Low-Power, RRIO, 1MHz Operational Amplifier for Cost-Sensitive Systems

General Description

ET85002 is a dual low-voltage (1.8 V to 5.5 V) operational amplifier with rail-to-rail input and output swing capabilities. ET85002 provides a cost-effective solution for space-constrained applications such as smoke detectors, wearable electronics, and small appliances where low-voltage operation and high capacitive-load drive are required. The capacitive-load drive is 500 pF and the resistive open−loop output impedance makes stabilization easier with much higher capacitive-loads. ET85002 features unity-gain stability, an integrated RFI and EMI rejection filter, and no-phase reversal in overdrive conditions.

ET85002 is specified for the extended industrial / automotive temperature range (-40°C to +125°C). ET85002 is available in SOP8 / MSOP8 / DFN8 packages.

Features

- Dual CMOS amplifier for low-cost applications
- Rail-to-rail input and output
- Low input offset voltage: ±0.4 mV
- Unity-gain bandwidth: 1 MHz
- Low broadband noise: 27 nV/$\sqrt{Hz}$
- Low input bias current: 5 pA
- Low quiescent current: 60 μA/Ch
- Unity-gain stable
- Internal RFI and EMI filter
- Operational at supply voltages as low as 1.8 V
- Easier to stabilize with higher capacitive load
- Extended temperature range: -40°C to 125°C

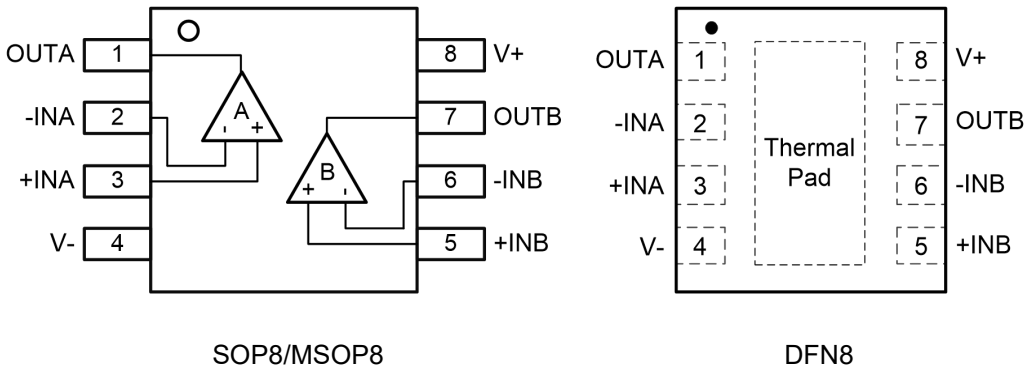
Applications

- Temperature sensors
- Sensor signal conditioning
- Power modules
- Active filters
- Low-side current sensing

Device information

Part No.	Package	MSL
ET85002M	SOP8	3
ET85002U	MSOP8	3
ET85002Y	DFN8(2×2)	1

Pin Configuration



SOP8/MSOP8 DFN8

Top View

Pin Function

Pin Number ET85002M/U/Y	Symbol	Descriptions
1,7	OUT	Output
4	V-	Negative supply
3,5	+IN	Non-inverting input
2,6	-IN	Inverting input
8	V+	Positive supply

Functional Description

Operating Voltage

ET85002 is for operation from 1.8 V to 5.5 V. In addition, many specifications such as input offset voltage, quiescent current, offset current, and short circuit current apply from -40°C to 125°C.

Rail-to-Rail Input

The input common-mode voltage range extends 100 mV beyond the supply rails for the full supply voltage range of 1.8 V to 5.5 V. This performance is achieved with a complementary input stage.

Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the ET85002 delivers a robust output drive capability. A class-AB output stage with common-source transistors achieves full rail-to-rail output swing

capability. For resistive loads of 10 kΩ, the output swings to within 20 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

Device Functional Modes

ET85002 has a single functional mode. The devices are powered on as long as the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are only stress ratings, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Parameter	Rating	Unit
Supply Voltage(1) (V+) - (V-)	6.0	V
Input Voltage	(V-)-0.3V to (V+)+0.3	V
Differential Input Voltage	(V+) - (V-)+0.2	V
ESD (Human Body Model)	±2000	V
Storage Temperature Range	-65 to +150	°C
Junction Temperature Range	-65 to +150	°C
Lead Temperature Range (Soldering, 60 sec)	300	°C
Operating Temperature Range	-40 to +125	°C

Note1: All voltage values, except differential voltage are with respect to network terminal.

Recommended Operating Conditions

Parameter	Min	Max	Unit
Supply Voltage (V_S)	1.8	5.5	V
Operating Temperature (T_A)	-40	125	°C

Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
$R_{\theta JA}$	SOP8	Thermal Characteristics, Thermal Resistance, Junction-to-Air	160	°C/W
	MSOP8		200	°C/W
	DFN8(2×2)		160	°C/W

Electrical Characteristics

V_S = (V+) – (V-) = 1.8 V to 5.5 V (± 0.9 V to ± 2.75 V), T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{CM} = V_{OUT} = V_S/2 (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±0.4	±2	mV
		V_S = 5 V, T_A = -40°C to 125°C			±2.5	
dV_{OS}/dT	V_{OS} vs temperature	T_A = -40°C to 125°C		±0.6		µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 to 5.5 V, V_{CM} = (V-)	80	105		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	No phase reversal, rail-to-rail input	(V-)-0.1		(V+)+0.1	V
CMRR	Common-mode rejection ratio	V_S = 1.8 V, (V-) - 0.1 V < V_{CM} < (V+) - 1.4 V, T_A = –40°C to 125°C		86		dB
		V_S = 5.5 V, (V-) - 0.1 V < V_{CM} < (V+) - 1.4 V, T_A = -40°C to 125°C		95		
		V_S = 5.5 V, (V-) -0.1 V < V_{CM} < (V+) + 0.1 V, T_A = -40°C to 125°C		77		
		V_S = 1.8 V, (V-) - 0.1 V < V_{CM} < (V+) + 0.1 V, T_A = -40°C to 125°C		68		
INPUT BIAS CURRENT						
I_B	Input bias current	V_S = 5 V		±5		pA
I_{OS}	Input offset current			±2		pA
NOISE						
E_n	Input voltage noise (peak to peak)	f = 0.1 Hz to 10 Hz, V_S = 5 V		4.7		μV_{PP}
e_n	Input voltage noise density	f = 1 kHz, V_S = 5 V		30		nV/√Hz
		f = 10 kHz, V_S = 5 V		27		
i_n	Input current noise density (2)	f = 1 kHz, V_S = 5 V		23		fA/√Hz
INPUT CAPACITANCE (2)						
C_{ID}	Differential			1.5		pF
C_{IC}	Common-mode			5		pF

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OPEN-LOOP GAIN						
A_{VO}	Open-loop voltage gain	V_S = 5.5 V, R_L = 10 kΩ (V-) + 0.05 V < V_O < (V+) - 0.05 V	104	117		dB
		V_S = 1.8 V, R_L = 10 kΩ (V-) + 0.04 V < V_O < (V+) - 0.04 V		100		
		V_S = 1.8 V, R_L = 2 kΩ (V-) + 0.1 V < V_O < (V+) - 0.1 V		115		
		V_S = 5.5 V, R_L = 2 kΩ (V-) + 0.15 V < V_O < (V+) – 0.15 V		130		
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	V_S = 5 V		1		MHz
φ_m	Phase margin	V_S = 5 V, G = 1		78		°
SR	Slew rate	V_S = 5 V		2		V/μs
t_S	Settling time (2)	To 0.1%, V_S = 5 V, 2V step, G = +1, C_L = 100 pF		2.5		μs
		To 0.01%, V_S = 5 V, 2V step, G = +1, C_L = 100 pF		3		
t_{OR}	Overload recovery time	V_S = 5 V, V_{IN} × gain > V_S		0.85		μs
THD+N	Total harmonic distortion + noise	V_S = 5.5 V, V_{CM} = 2.5 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz,		0.004		%
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 5.5 V, R_L = 10 kΩ		10	20	mV
		V_S = 5.5 V, R_L = 2 kΩ		35	55	
I_{SC}	Short-circuit current	V_S = 5.5 V		±40		mA
Z_O	Open-loop output impedance (2)	V_S = 5 V, f = 1 MHz		1200		Ω
POWER SUPPLY						
V_S	Specified voltage range		1.8 (±0.9)		5.5 (±2.75)	V
I_Q	Quiescent current per amplifier	I_O = 0 mA, V_S = 5.5 V		60	85	μA
		I_O = 0 mA, V_S = 5.5 V, T_A = -40°C to 125°C			90	

Note2: Guaranteed by design.

Application Notes

Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

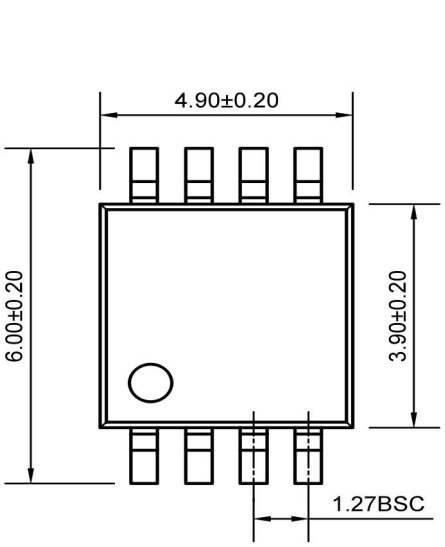
Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.

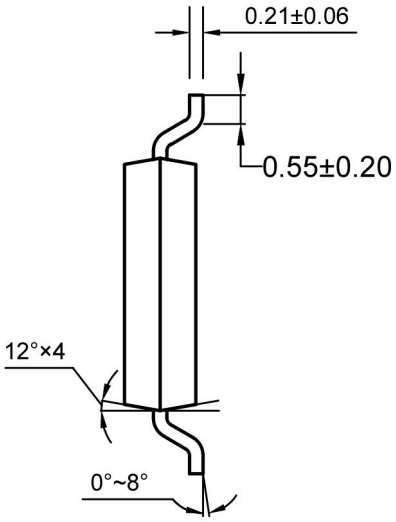
To reduce parasitic coupling, run the input traces as far away from the supply lines and digital signal as possible.Low-ESR, 0.1μF ceramic bypass capacitors must be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single supply applications.

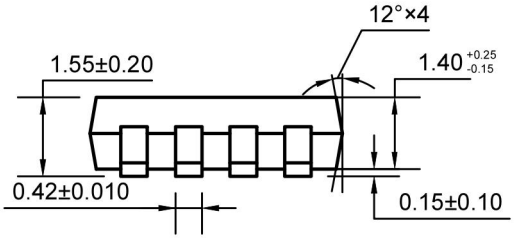
Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

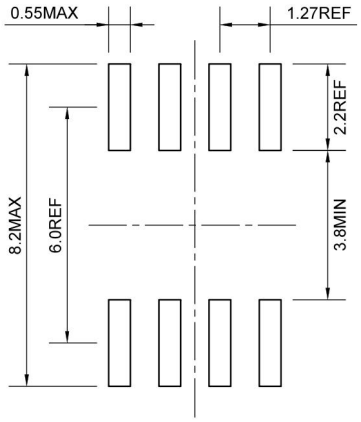
Package Dimension

SOP8



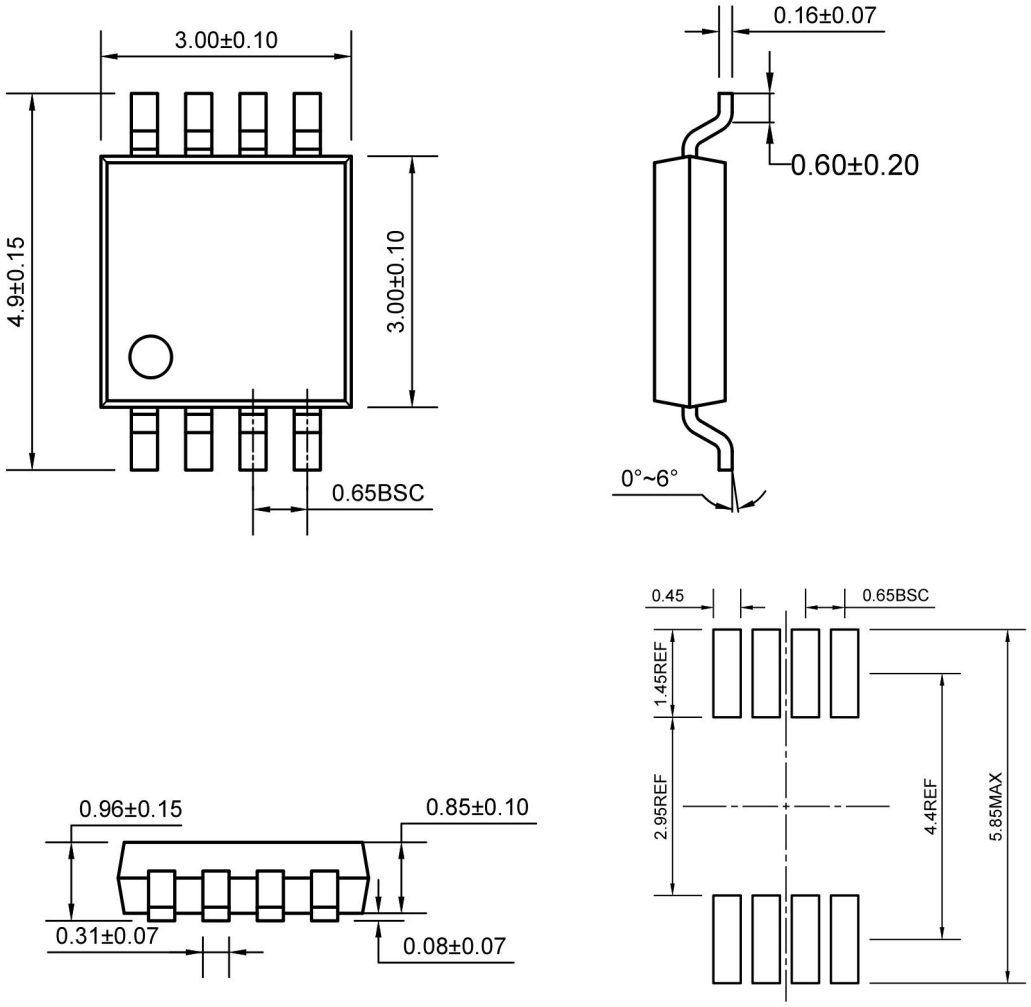






Recommended Land Pattern

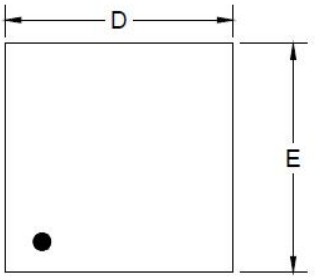
MSOP8



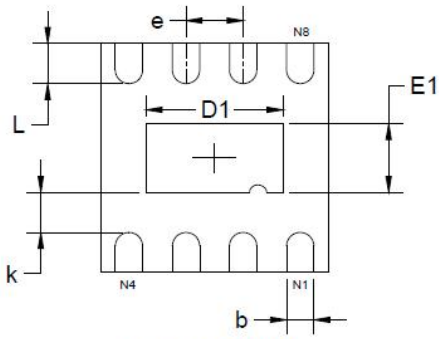
Recommended Land Pattern

Unit: mm

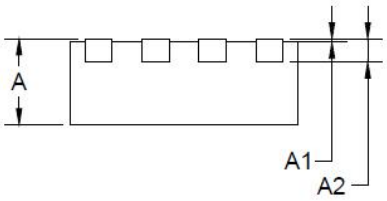
DFN8-2×2



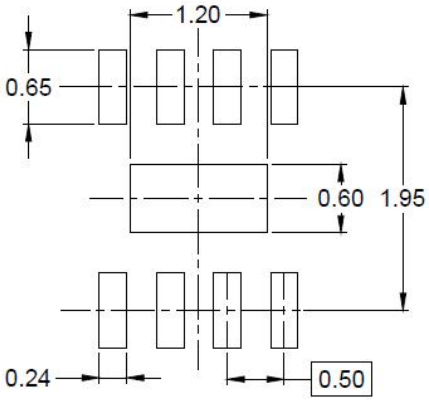
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
D1	1.100	1.300	0.043	0.051
E	1.900	2.100	0.075	0.083
E1	0.500	0.700	0.020	0.028
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.250	0.450	0.010	0.018

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2022-9-21	Preliminary Version	Shibo	Wanggp	Liujy
1.0	2023-9-27	Original Version	Huyt	Chenh	Liujy
1.1	2024-11-27	IQ max changed 82uA	Shibo	Wanggp	Liujy
1.2	2025-3-24	Update VOS max and IQ max	Huyt	Chenh,Tangyx	Liujy
1.3	2025-4-11	Update MSL Grade	Huyt	Chenh,Tangyx	Liujy