**Octal Buffers/Drivers With 3-State Outputs**

###### General Description

The ETQ74HCT541V octal buffers/drivers is ideal for driving bus lines or buffer memory address registers. The device feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable

(or) input is high, all corresponding outputs are in the high-impedance state. The outputs provide non-inverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down,should be tied to VCC through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

###### Features

* Designed for 4.5 to 5.5V VCC Operation
* Inputs are TTL Voltage Compatible
* Latch-up Performance Exceeds 200mA per JESD78, Class II
* Multiple Package Options Automotive AEC-Q100 Grade 1 Qualified
* ESD Protection Exceeds JESD22

4000V Human-Body Model (A114-A)

2000V Charged-Device Model (C101)

* Part No. and package

|  |  |  |
| --- | --- | --- |
| Part No. | Package | MSL |
| ETQ74HCT541V | TSSOP20 (6.5mm×4.4mm) | 1 |

###### Applications

* Fully Compliant with Standards for Automotive Applications
* Combine Normal Power Signals from Multiple Power Rails

###### Pin Configuration



TSSOP20

Figure 1. Top View

###### Pin Function

|  |  |  |
| --- | --- | --- |
| Pin No. | Name | Description |
| 1 | 1 | Output Enable 1 |
| 2 | A1 | Input A1 |
| 3 | A2 | Input A2 |
| 4 | A3 | Input A3 |
| 5 | A4 | Input A4 |
| 6 | A5 | Input A5 |
| 7 | A6 | Input A6 |
| 8 | A7 | Input A7 |
| 9 | A8 | Input A8 |
| 10 | GND | Ground |
| 11 | Y8 | Output Y8 |
| 12 | Y7 | Output Y7 |
| 13 | Y6 | Output Y6 |
| 14 | Y5 | Output Y5 |
| 15 | Y4 | Output Y4 |
| 16 | Y3 | Output Y3 |
| 17 | Y2 | Output Y2 |
| 18 | Y1 | Output Y1 |
| 19 | 2 | Output Enable 2 |
| 20 | VCC | Power |

###### Block Diagram

 

Figure 2. Logic Diagram

###### Functional Description

Function Table**(1)**

|  |  |
| --- | --- |
| Inputs | Output  |
| 1 | 2 | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

***Note1***: H = High voltage level ,

L = Low voltage level ,

X = Don’t care ,

Z = High-impedance off-state.

###### Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

|  |  |  |  |
| --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Value** | **Unit** |
| VCC | Supply voltage range  | -0.5 to 7.0 | V |
| VI | Input voltage range **(2)** | -0.5 to 7.0 | V |
| VO | Output voltage range**(2)**  | -0.5 to VCC + 0.5 | V |
| IIK | Input clamp current, VI < GND | -20 | mA |
| IOK | Output clamp Current ,VO < GND, VO > VCC | ±20 | mA |
| IO | Continuous output current, IO(VO = 0 to VCC) | ±25 | mA |
| ICC | Continuous current through VCC | ±75 | mA |
| IGND | Continuous current through GND | ±75 | mA |
| TJMAX | Maximum Junction Temperature | 150 | °C |
| PD | Max Power Dissipation (TSSOP20) | 400 | mW |
| TSTG | Storage Temperature Range | -65 to 150 | °C |
| VESD | Human Body Model ESD (JESD22-A114-A) | ±4000 | V |
| Charged Device Model ESD (JESD22-C101) | ±2000 |
| ILU | Latch up Current Maximum Rating (JESD78E) | ±200 | mA |

 ***Note2***. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

###### Recommended Operating Conditions

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Symbol | Parameter | Min | Max | Unit |
| VCC | Supply voltage | 4.5 | 5.5 | V |
| VIH | High-level input voltage | 2 | VCC | V |
| VIL | Low-level input voltage | 0 | 0.8 | V |
| VI | Input Voltage | 0 | 5.5 | V |
| VO | Output Voltage | 0 | VCC | V |
| IOH | High-level output current |  | -8 | mA |
| IOL | Low-level output current |  | 8 | mA |
| TA | Operating Temperature Range | -40 | 125 | °C |
| ∆t/∆V | Input Transition Rise or Fall Rate  |  | 20 | ns/V |

###### Electrical Characteristics

###### DC Electrical Characteristics

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Condition** | **VCC(V)** | **TA=25°C** | **−40°C≤TA≤125°C** | **Unit** |
| **Min** | **Typ** | **Max** | **Min** | **Max** |
| VOH | High−Level Output Voltage | IOH = -50μA | 4.5 | 4.4 | 4.5 |  | 4.4 |  | V |
| IOH = -8mA | 3.94 | 4.3 |  | 3.8 |  |
| VOL | Low−Level Output Voltage | IOL = 50μA | 4.5 |  | 0.001 | 0.1 |  | 0.1 | V |
| IOL = 8mA |  | 0.17 | 0.26 |  | 0.33 |
| II | Input Leakage Current | VI = 5.5V or GND | 0 to 5.5 |  |  | ±0.1 |  | ±1 | μA |
| IOZ | Output Leakage Current | Vo = VCC or GND | 5.5 |  |  | ±0.25 |  | ±2.5 |
| ICC | Quiescent Supply Current | VI = VCC or GND | 5.5 |  |  | 4 |  | 40 | μA |
| ΔICC**(3)** | One Input at 0.5V or 2.4V or 3.4V,Other Inputs at VCC or GND | 5.5 |  | 1.35 | 1.4 |  | 1.5 | mA |
| CI | VI=VCC or GND | 5.0 |  | 2 | 10 |  | 10 | pF |
| CO | VO=VCC or GND | 5.0 |  | 4 |  |  | 10 |

***Note3:*** This is the increase in supply current for each input at one of the specified TTL voltage levels,rather than 0V or VCC

###### Switching Characteristics (4)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Symbol | Condition | VCC | TA=25°C | −40°C≤TA≤125°C | Unit |
| Min | Typ | Max | Min | Max |
| tpd | From A to Y, CL=15pF | 4.5 V |  | 4.1 | 6 | 1 | 6.5 | ns |
| 5.5 V |  | 4.1 | 6 | 1 | 9.5 |
| ten | From /OE to Y, CL=15pF | 4.5 V |  | 5 | 7 | 1 | 8 |
| 5.5 V |  | 5 | 7 | 1 | 8 |
| tdis | From /OE to Y, CL=15pF | 4.5 V |  | 4.5 | 7 | 1 | 8 |
| 5.5 V |  | 4.5 | 7 | 1 | 8 |
| tpd | From A to Y, CL=50pF | 4.5 V |  | 6.2 | 8.5 | 1 | 9.5 |
| 5.5 V |  | 6.2 | 8.5 | 1 | 9.5 |
| ten | From /OE to Y, CL=50pF | 4.5 V |  | 7.5 | 10 | 1 | 12 |
| 5.5 V |  | 7.5 | 10 | 1 | 12 |
| tdis | From /OE to Y, CL=50pF | 4.5 V |  | 7 | 10 | 1 | 12 |
| 5.5 V |  | 7 | 10 | 1 | 12 |
| tt | CL=50pF | 4.5 V |  | 8 | 12 |  | 15 |
| 5.5 V |  | 7 | 11 |  | 14 |
| tpd | From A to Y, CL=150pF | 4.5 V |  | 20 | 33 | 1 | 42 |
| 5.5 V |  | 19 | 30 | 1 | 38 |
| ten | From /OE to Y, CL=150pF | 4.5 V |  | 26 | 40 | 1 | 50 |
| 5.5 V |  | 25 | 36 | 1 | 45 |
| tt | CL=150pF | 4.5 V |  | 17 | 42 |  | 53 |
| 5.5 V |  | 14 | 38 |  | 48 |

***Note4.*** Guaranteed by design and characterization. not a FT item.

**Capacitance Characteristics**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Symbol | Parameter | Condition | Typ | Unit |
| CPD**(5)** | Power Dissipation Capacitance  | 10MHz,VCC= 5.0 V, TA=25°C,No load | 12 | pF |

***Note5.*** CPD is used to determine the dynamic power dissipation (PD in μW).

PD = CPD × VCC 2 × fi × N + Σ(CL × VCC 2 × fo) where:

fi = Input Frequency in MHz;

fo = Output Frequency in MHz;

CL = Output Load capacitance in pF;

VCC = Supply Voltage in V;

N = Number of Inputs Switching;

Σ(CL × VCC 2 × fo) = Sum of Outputs.

**AC Characteristics Test Waveform**

|  |
| --- |
| Figure 3. Load circuit for pole outputs & Load circuit for 3-state and open-drain outputsFigure 5. Voltage waveform propagation delay times inverting and noninverting outputs(left)Figure 6. Voltage waveforms enable and disable times low-and high-level enabling(right)*Note A:* CL includes probe and jig capacitance.***Note B:*** Figure 5 is for an output with internal conditions such that the output is low except when disable by the output control. Figure 6 is for an output with internal conditions such that the output is high except when disable by the output control. |

###### Package Dimension

TSSOP20 (6.5mm×4.4mm)



###### Revision History and Checking Table

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Version** | **Date** | **Revision Item** | **Modifier** | **Function & Spec Checking** | **Package & Tape****Checking** |
| 0.0 | 2025-04-28 | Preliminary version | Lizh | Yangxx | Liujy |