4.5V to 38V Input, 3A Synchronous Step-Down Regulator

General Description

The ETQ8134M is a highly integrated, wide input voltage, 3A output synchronous buck convertor. The device is optimized to operate with minimum external component counts and also optimized to achieve low standby current.

This convertor adopts adaptive constant-on-time (ACOT) structure, and provides a fast transient response. It also supports both low-equivalent series resistance (ESR) output capacitors and ultra-low ESR ceramic capacitors with no external compensation components. During light load operation, ETQ8134M operates in pulse frequency modulation (PFM) mode, which maintains high efficiency.

ETQ8134M is available in a ESOP8 package.

Features

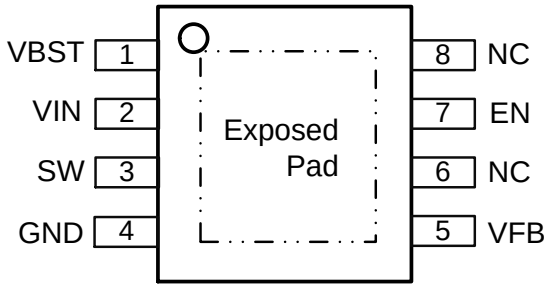
- 3A Converters Integrated 130mΩ and 100mΩ FET
- ACOT mode control with fast transient response
- Input Voltage Range: 4.5V to 38V
- Output Voltage Range:V_{FBTH} to 12V
- FB voltage is 0.923V (TYP)
- PFM mode during light load operation
- 600KHz Switching Frequency
- Low Shutdown Current Less than 5 μA
- Start-up from Pre-Biased Output Voltage
- Cycle-by-Cycle Over-current Limit
- Hiccup-mode Over-current Protection
- Non-Latch UVP and TSD Protections
- Fixed Soft Start: 1.0ms
- Automotive AEC-Q100 Grade 2 Qualified
- Part No. and Package

Part No.	Package	MSL
ETQ8134M	ESOP8	3

Application

- Digital TV Power Supply and Surveillance
- Disc Players
- Networking Home Terminal
- Digital Set Top Box

Pin Configuration



Top View

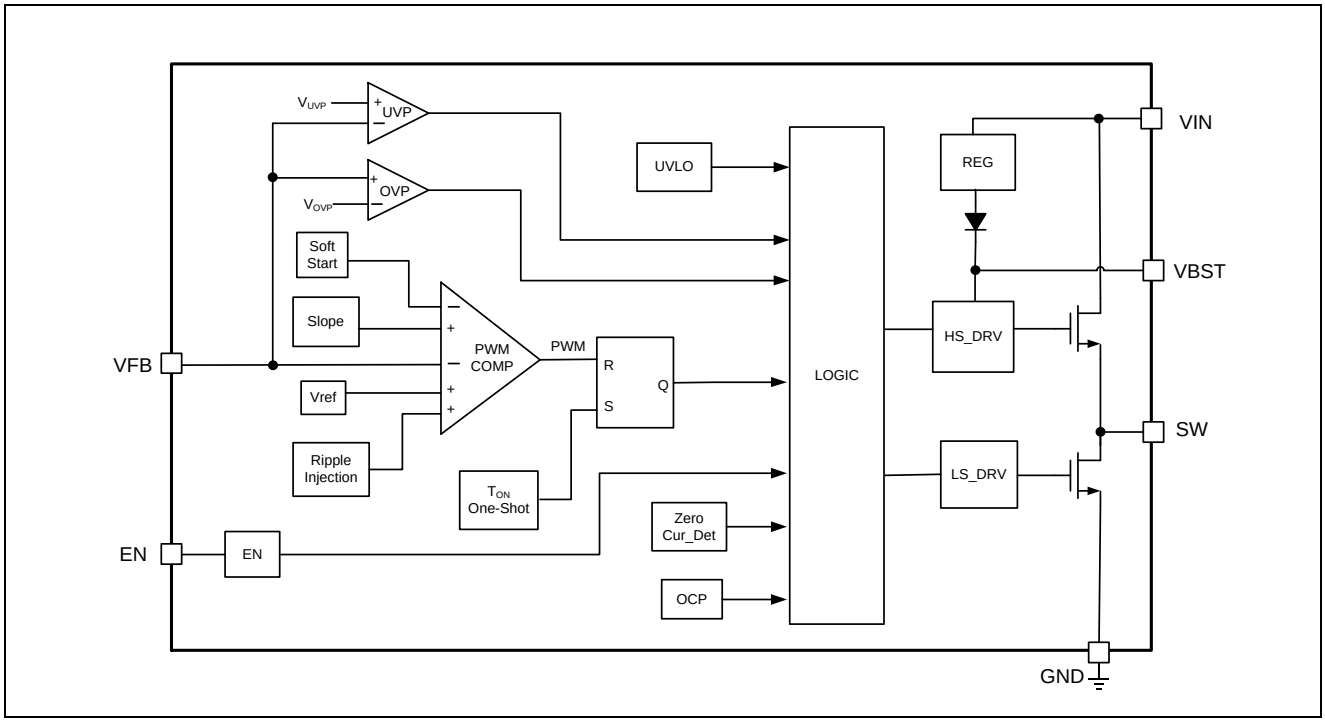
Note: The Exposed Pad must be connect with GND on Printed Circuit Board.

Pin Function

Pin Name	Pin No.	I/O	Description
VBST	1	O	Power supply of high-side NFET control circuit. Connect 0.1μF capacitor between VBST and SW pins.
VIN	2	I	Input voltage supply pin, also the drain terminal of high-side power NFET.
SW	3	O	Switch node connection between low-side NFET and high-side NFET.
GND	4		Ground pin of controller circuit, as well as source terminal of low-side power NFET. Connect sensitive VFB to this GND at a single point.
VFB	5	I	Output voltage feedback pin. Connect to output voltage with feedback resistor divider.
NC	6		No connect
EN	7	I	Enable pin. Must be pulled up to enable the device.
NC	8		No connect
EP	/		Exposed Pad for heat dissipating, it is recommended to connect GND

Note: The Exposed Pad must be connect with GND on Printed Circuit Board.

Block Diagram



Functional Description

Overview

The ETQ8134M is highly integrated, 3A synchronous Buck convertor. It employs adaptive constant on time (ACOT) mode, and supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of this device can reduce the output capacitance.

Adaptive On-Time Control and PWM Operation

The main control mode of ETQ8134M is pulse width modulation (PWM) with ACOT structure. This control mode control can achieve pseudo-fixed frequency and stable operation with both low-ESR and ceramic output capacitors.

The high-side MOSFET is turned on at the beginning of each cycle. When one shot timer expires, the high-side power FET is turned off. This one shot duration is set proportional to input voltage, V_{IN}, and inversely proportional to the output voltage, V_O, to achieve pseudo-fixed frequency over the input voltage range, hence it is called adaptive constant on-time control. The one-shot timer is reset and the high-side power FET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is generated to emulate output ripple, eliminating the need for ESR of output capacitor.

Pulse Frequency Modulation

The ETQ8134M is designed with pulse frequency modulation mode to achieve high efficiency during light load condition. As the output current decreases from heavy load condition, the inductor current also deceases and eventually comes to zero, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side power FET is turned off when the zero inductor current is detected. As the load current

further decreases the convertor enters into discontinuous conduction mode. The on-time is almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps efficiency high in light load condition. The transition point to the light load operation IOUT(LL) current can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{sw}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

In PFM mode, each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the VFB voltage falls below the threshold voltage. As the output current decreases, the sleep time between switching pulses increases.

Soft Start and Pre-Biased Soft Start

The ETQ8134M is designed with an internal 1ms soft-start. When the VIN is plugged in and the EN pin becomes high, the reference voltage of PWM comparator begins to rise from zero.

If the output capacitor is pre-biased at start-up, the device begins to switch and start ramping up only after the internal reference voltage becomes greater than the feedback voltage VFB. This scheme ensures that the convertors ramp up smoothly into regulation point.

Current Protection

The over-current limit (OCL) is implemented by using cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET drain to source voltage during its on-state. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-state of high-side FET, the switch current increases at a linear rate determined by VIN, VOUT, and the inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current IOUT. If the monitored current is above the OCL level, the convertor keeps low-side FET on and prevents the creation of a new set pulse, even the voltage feedback loop requires one, until the current level decreases to OCL level or lower. In next switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the load current is higher than the current available from the convertor. This may cause the output voltage to fall. When the VFB voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device will shut down after the UVP delay time and re-start after the hiccup time (typically 6ms).When the over current condition is removed, the output voltage returns to the regulated value.

Under-voltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When input voltage increases up to the upper threshold of UVLO, it begins to switch.

Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 170°C), the device is shut off. When the temperature falls to about 140oC or below, the convertor begins to switch.

Standby Operation

When the ETQ8134M is operating in either normal CCM or PFM, they may be placed in standby by pulling the EN pin to low.

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameters	Min	Max	Unit
V_I	VIN Voltage Range	-0.3	40	V
	EN Voltage Range	-0.3	40	V
	VBST Voltage Range	-0.3	44	V
	VBST(10ns transient) Voltage Range	-0.3	46	V
	VBST(VS SW) Voltage Range	-0.3	6.5	V
	VFB Voltage Range	-0.3	6.5	V
	SW Voltage Range	-2	40	V
	SW (10ns transient)	-3.5	42	V
V_{ESD}	Human Body Model (JEDEC JS-001)		±2000	V
	Charged Device Model (JESD22-C101)		±1000	V
T_J	Junction Temperature	-40	+150	°C
T_{STG}	Storage Temperature	-65	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameters	Min	Typ	Max	Unit
V_{IN}	Supply Input Voltage Range (VIN)	4.5		38	V
V_{OUT}	Output Voltage Range	0.923		12	V
I_{OUT}	Output current Range			3	A
T_J	Operating Junction Temperature	-40		125	°C
T_A	Ambient Temperature	-40		105	°C

Thermal Properties

Symbol	Parameters	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	52	°C/W

Electrical Characteristics

V_{IN} = 12V, T_A = -40°C to 85°C, (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Current						
I_{IN}	Operating–non-switching Supply Current	V_{IN} current, EN = 5V,V_{FB} = 1.0V		300		μA
I_{IN_OFF}	Shutdown supply current	V_{IN} current, EN = 0V		1.6	5	
Logic Threshold						
V_{ENH}	EN High-level Input Voltage		1.6			V
V_{ENL}	EN Low-level Input Voltage				0.8	
R_{EN}	EN Pin Resistance to GND	V_{EN} = 12V	200	320	600	kΩ
V_{FB} Voltage and Discharge Resistance						
V_{FBTH}	V_{FB} Threshold Voltage	V_O = 1.05V, I_O = 10mA, PFM operation		930		mV
	V_{FB} Threshold Voltage	V_O = 1.05V, Continuous mode operation	900	923	946	mV
I_{FB}	V_{FB} Input Current	V_{FB} = 1.0V			0.1	μA
MOSFET						
$R_{DS(ON)H}$	High-side Switch Resistance	T_A = 25°C, V_{BST} – V_{SW} = 5V		130		mΩ
$R_{DS(ON)L}$	Low-side Switch Resistance	T_A = 25°C		100		mΩ
Current Limit						
I_{OCL}	Current Limit	DC current, V_{OUT} = 1.05V, L_1 = 2.2μH	3.5	4.2	5.5	A
Thermal Shutdown						
T_{SDN}	Thermal Shutdown Threshold(1)	Shutdown temperature		170		°C
T_{SDN_HYS}		Hysteresis		30		
ON-Time Timer Control						
$t_{OFF(MIN)}$	Minimum off Time	V_{FB} = 0.5V		150		ns
Soft Start						
T_{SS}	Soft Start Time	Internal soft-start time		1.0		ms
Frequency						
F_{SW}	Switching Frequency	CCM mode		600		KHz
Output Under-voltage Protection						
V_{UVP}	Output UVP Threshold	Hiccup detect (H > L)		60		%
UVLO						
V_{UVLO}	UVLO Threshold	Wake up V_{IN} voltage		3.9	4.3	V
		Shutdown V_{IN} voltage	3.5	3.7		
		Hysteresis V_{IN} voltage		0.2		

Note1: Not production tested, design assurance.

Application and Implementation

Note

Information in the following applications sections is not part of the ETEK component specification. ETEK does not warrant its accuracy or completeness and Customers should be responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

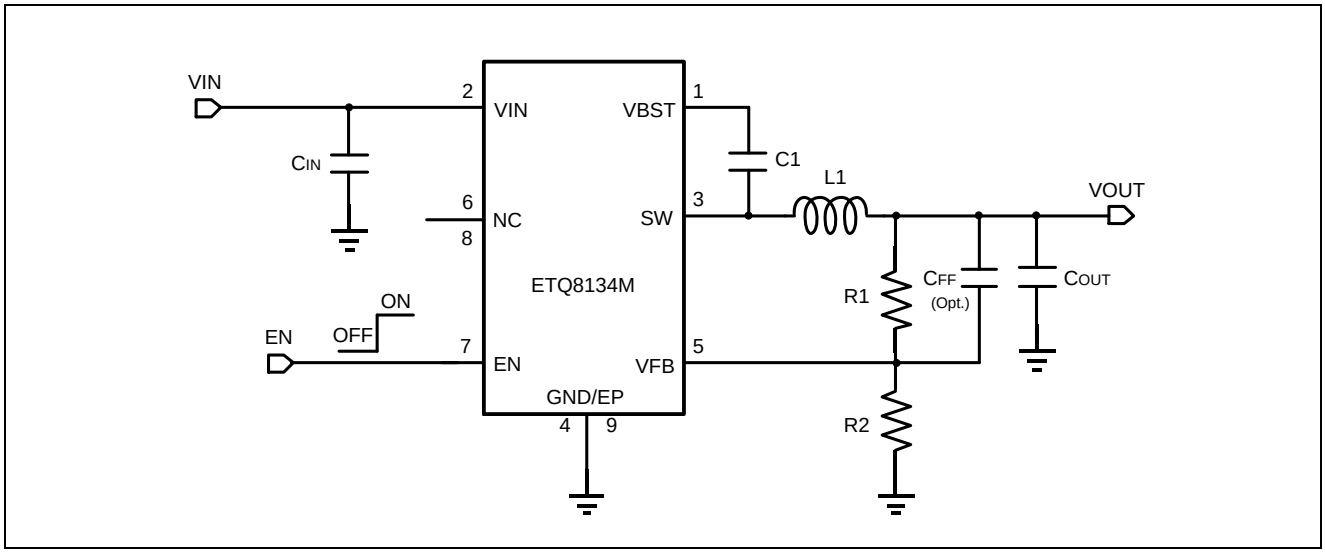
Application Information

ETQ8134M is typical step-down DC-DC converter. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 3A. The following design procedure can be used to select component values for the ETQ8134M.

Typical Application

The application schematic below was developed to meet the previous requirements. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

The figure shows ETQ8134M converter schematics.



OUT=X.XV / 3A Reference Design

Design Requirements

This table below shows the design parameters for this application.

Parameter	Example Value
Input voltage range	4.5 to 38V
Output voltage	1.05V
Transient response, 1.5A load step	ΔV_{OUT} = ±2.5 %
Input ripple voltage	400mV
Output ripple voltage	30mV
Output current rating	3A
Operating frequency	600KHz

Detailed Design Procedure

Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. ETEK recommends using 1% tolerance or better divider resistors. Start by using Equation 2 to calculate VOUT.

If customers want to improve efficiency at very light loads,we recommend using larger value resistors. High value of resistor will be more susceptible to noise and voltage errors from the V_{FB} input current will be more noticeable.

$$V_{OUT} = 0.923 \times (1 + \frac{R1}{R2}) \quad (2)$$

Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_p = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

The overall loop gain is set by the output set-point resistor divider network and the internal gain of the device at low frequencies. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a -40dB per decade rate and the phase drops rapidly. The inductor and capacitor for the output filter should be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 1.

V_{OUT}(V)	R1(KΩ)	R2(KΩ)	L1(μH)	C1(nF)	C_{IN}(μF)	C_{OUT}(μF)	C_{FF} (pF) Opt.
1.0	0.83	10	2.2	100	22	22×2	CFF Chapter
1.2	3	10	2.2	100	22	22×2	CFF Chapter
1.5	6.25	10	2.2	100	22	22×2	CFF Chapter
1.8	9.5	10	2.2	100	22	22×2	CFF Chapter
2.5	17.1	10	2.2	100	22	22×2	CFF Chapter
3.3	25.7	10	3.3	100	22	22×2	CFF Chapter
5.0	44.2	10	4.7	100	22	22×2	CFF Chapter
12.0	120	10	4.7	100	22	22×3	CFF Chapter

Table 1. Recommended Component Values

The inductor peak to peak ripple current, peak current and RMS current are calculated using Equation 4,Equation 5, and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$IL_{p\text{-}p} = \frac{V_{OUT}}{V_{IN}(MAX)} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{sw}} \quad (4)$$

$$IL_{peak} = I_O + \frac{IL_{p\text{-}p}}{2} \quad (5)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} IL_{P\text{-}P}^2} \quad (6)$$

For this design example, the calculated peak current is 3.5A and the calculated RMS current is 3.01A.

The inductor should be used with a peak current rating of 13A and an RMS current rating of 9A.

The capacitor value and ESR determines the amount of output voltage ripple. The ETQ8134M is intended for use with ceramic or other low ESR capacitors. We recommend using values range from 20μF to 68μF. Equation 7 determines the required RMS current rating for the output capacitor

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{sw}} \quad (7)$$

Two 22μF output capacitors are used for this design. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286A and each output capacitor is rated for 4A.

Input Capacitor Selection

The ETQ8134M requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. We recommend a ceramic capacitor over 10μF for the decoupling capacitor. An additional 0.1μF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current. Larger values of ripple current can restrict the maximum output current, before current limit is reached. Smaller values of ripple current reduce the SNR of the current mode controller and can lead to increased jitter in the duty cycle. Both the inductor and switching frequency tolerance have an impact on the selection of ripple current, and, therefore, inductor value. Use the maximum device current when calculating the ripple current for applications with much smaller maximum load than the maximum available from the device. The ratio of inductor ripple current over maximum output current is designated as K in the following equations. Equation 8 can be used to determine the value of inductance.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \times K \times I_{OUTmax}} \times \frac{V_{OUT}}{V_{IN}} \quad (8)$$

Ideally, the saturation current rating of the inductor is at least as large as the high-side switch current limit, I_{SC} .This ensures that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, I_{LIMIT}, is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly. This can lead to component damage. Do not allow the inductor to saturate. Inductors with a ferrite core material have very hard saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a soft saturation, allowing some relaxation in the current rating of the inductor. In any case, the inductor saturation current must not be less than the maximum peak inductor current at full load.

Bootstrap Capacitor Selection

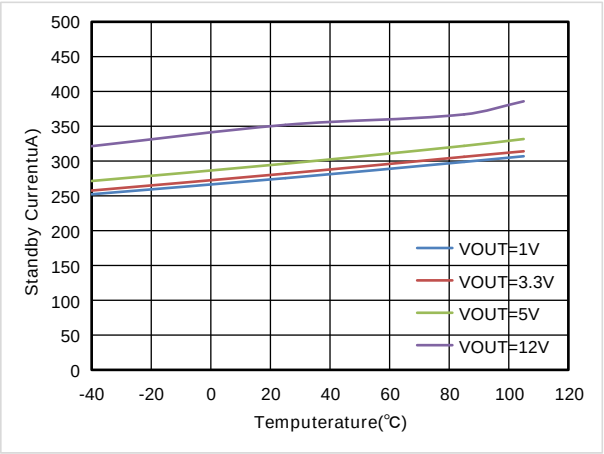
A 0.1uF ceramic capacitor must be connected between the VBST to SW pin for proper operation. We recommend using a ceramic capacitor.

Power Supply Recommendations

ETQ8134M is designed to operate from input supply voltage in the range of 4.5V to 38V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 75%. Using that criteria, the minimum recommended input voltage is V_O/0.75.

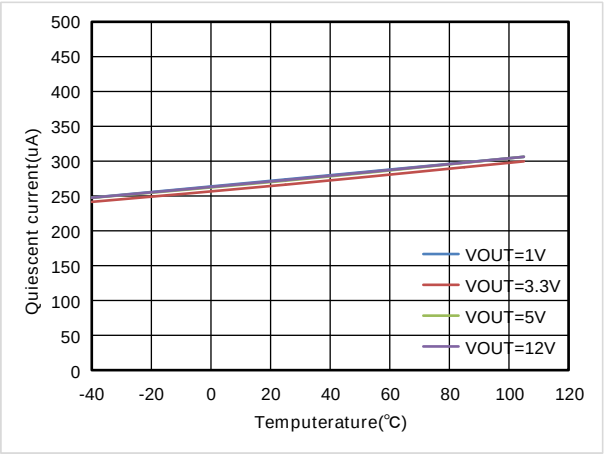
Application Curves

V_{IN} = 12V (unless otherwise noted)



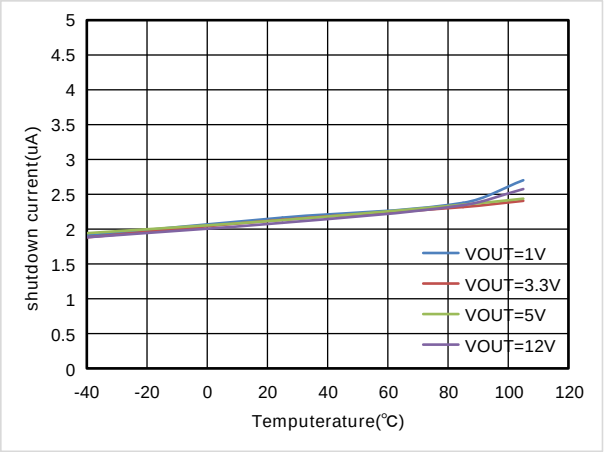
V_{IN}=24.0V

Figure1. Standby Current vs Temperature



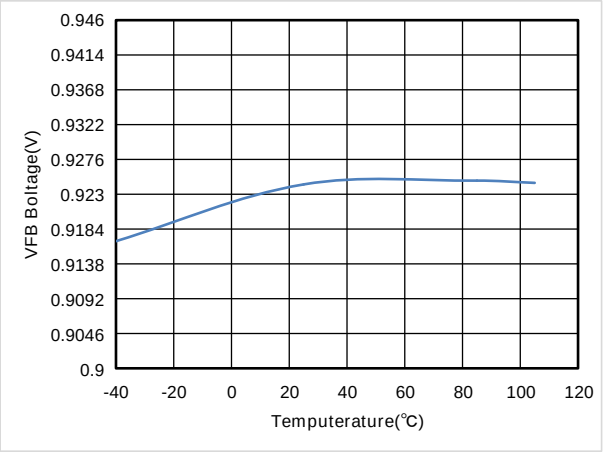
V_{IN}=24.0V

Figure2. Quiescent Current vs Temperature



V_{IN}=24.0V

Figure3. Shutdown Current vs Temperature



IOUT=2A

Figure4. VFB Voltage vs Temperature

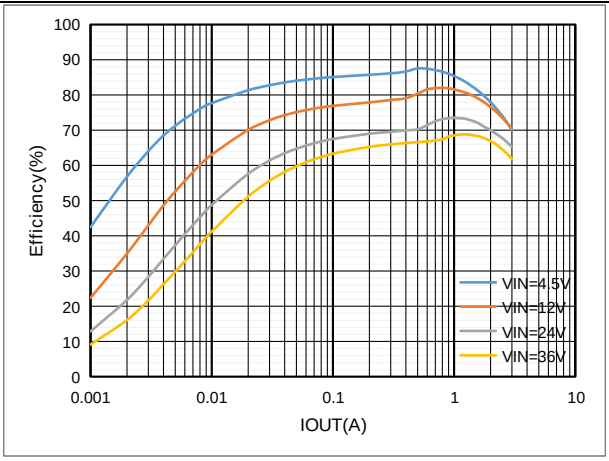


Figure5. Efficiency , VOUT=1.0V

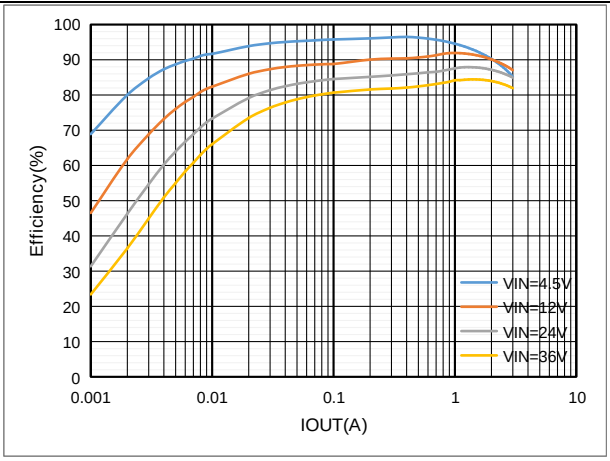


Figure6. Efficiency , VOUT=3.3V

Application Curves(Continued)

V_{IN} = 12V (unless otherwise noted)

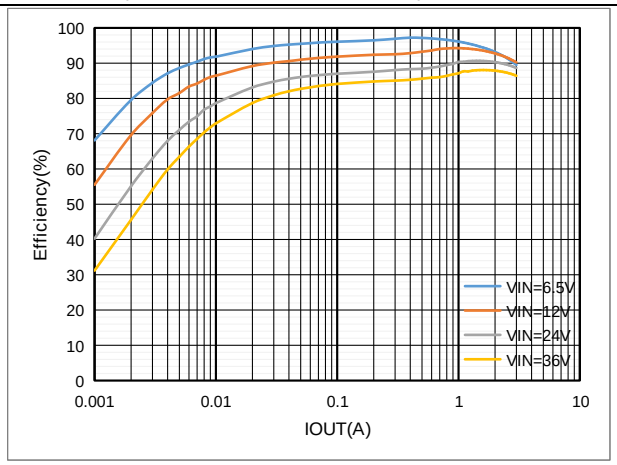


Figure7. Efficiency , VOUT=5.0V

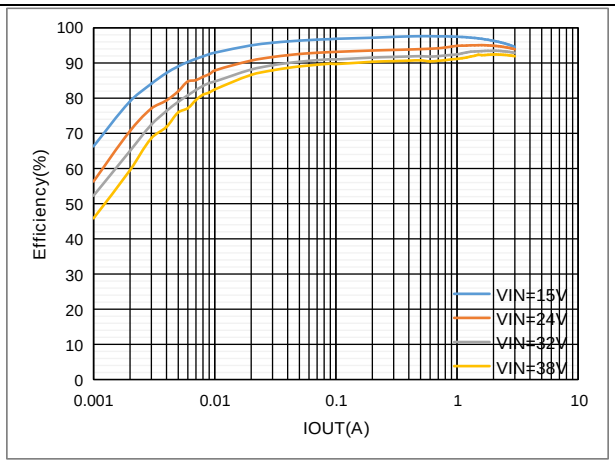


Figure8. Efficiency , VOUT=12.0V

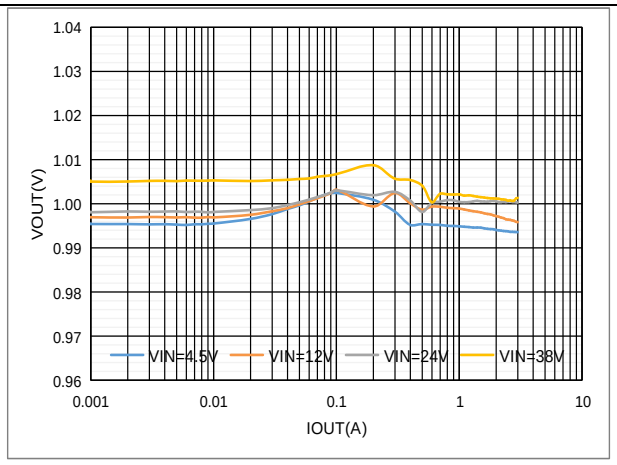


Figure9. Load Regulation , V_{OUT}=1.0V

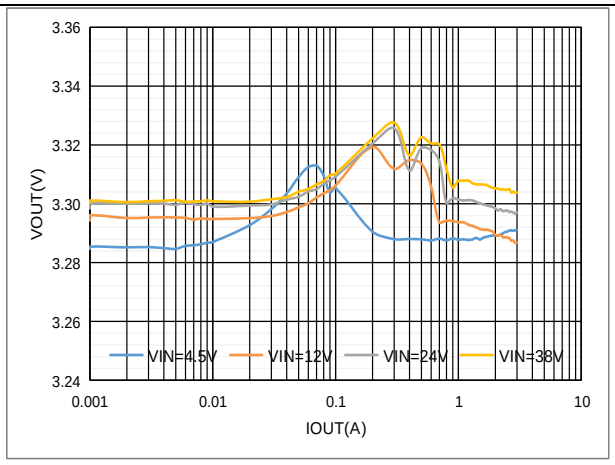


Figure10. Load Regulation , V_{OUT}=3.3V

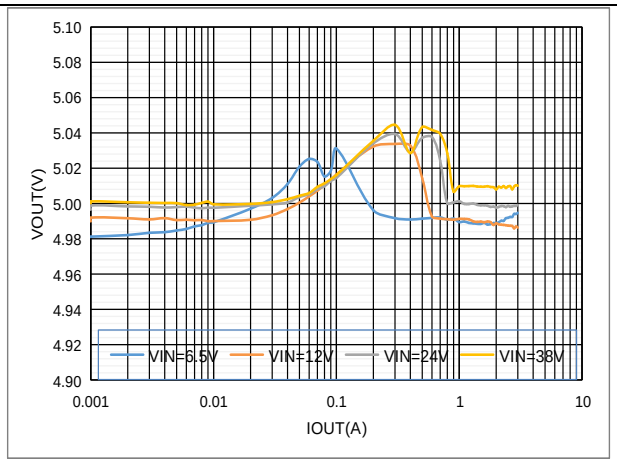


Figure11. Load Regulation , V_{OUT}=5.0V

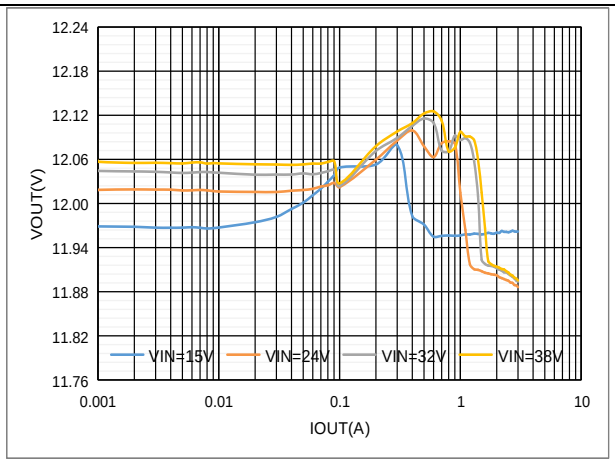


Figure12. Load Regulation , V_{OUT}=12.0V

Application Curves(Continued)

V_{IN} = 12V (unless otherwise noted)

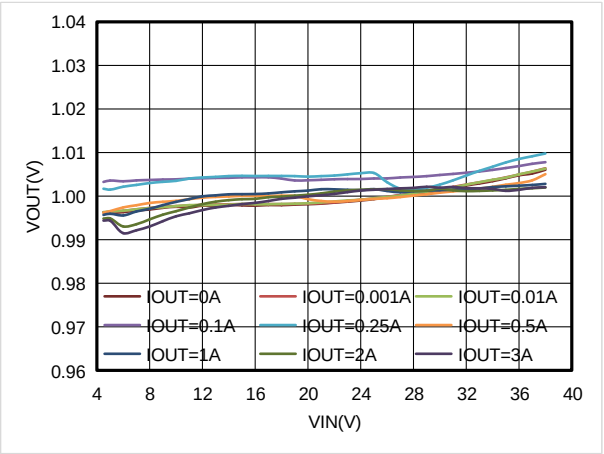


Figure13. Line Regulation,V_{OUT}=1.0V

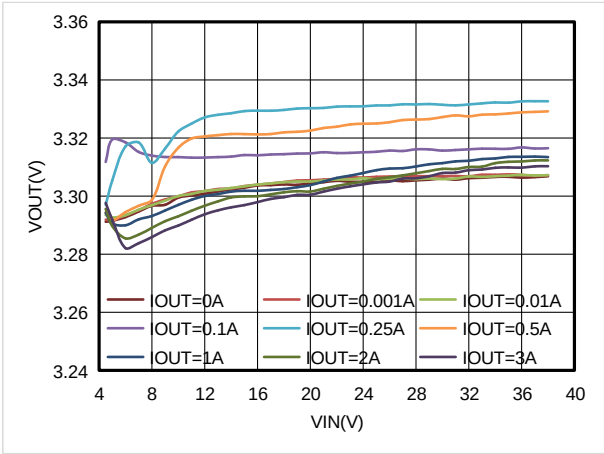


Figure14. Line Regulation, V_{OUT}=3.3V

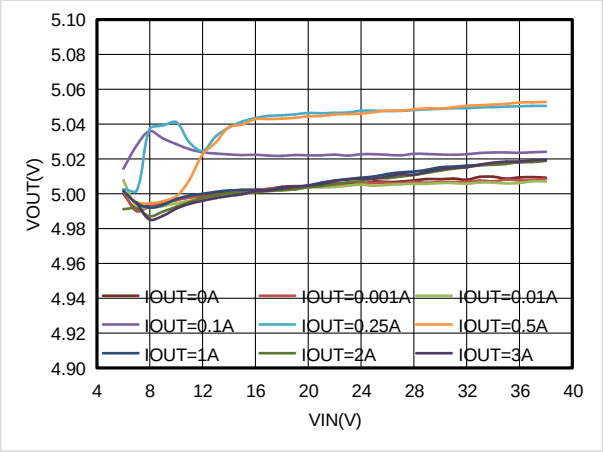


Figure15. Line Regulation, V_{OUT}=5.0V

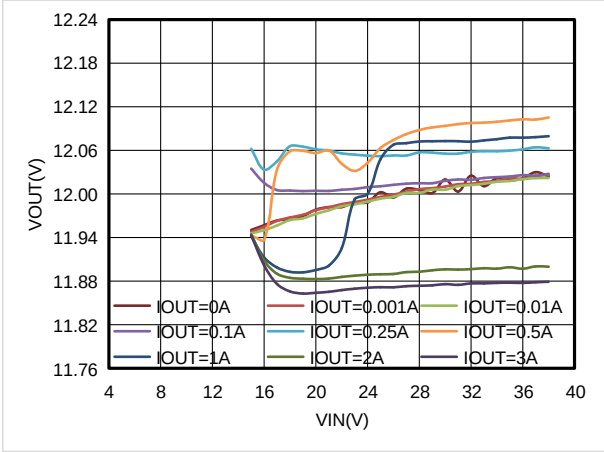
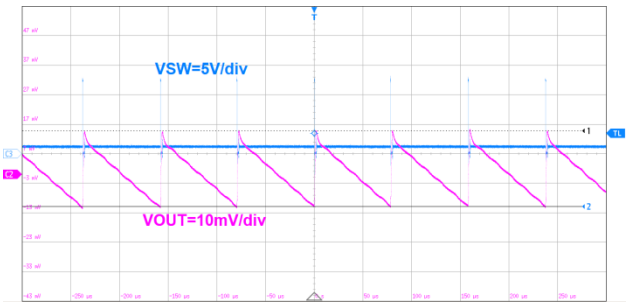
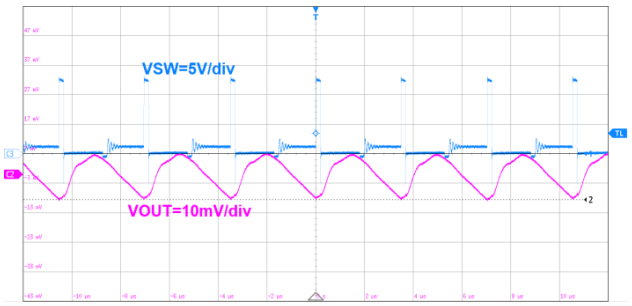


Figure16. Line Regulation, V_{OUT}=12.0V



50us/div V_{OUT}=1.0V I_{OUT}=0.01A

Figure17. Output Ripple

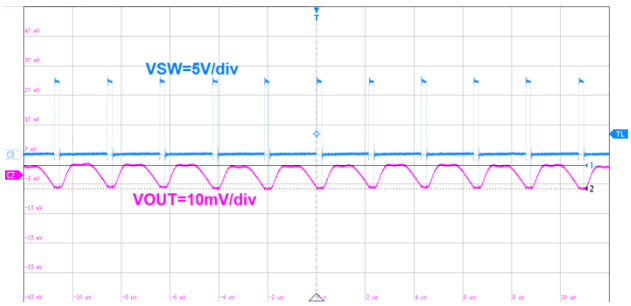


2us/div V_{OUT}=1.0V I_{OUT}=0.25A

Figure18. Output Ripple

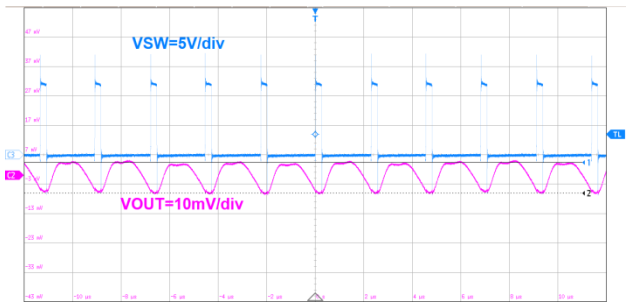
Application Curves(Continued)

V_{IN} = 12V (unless otherwise noted)



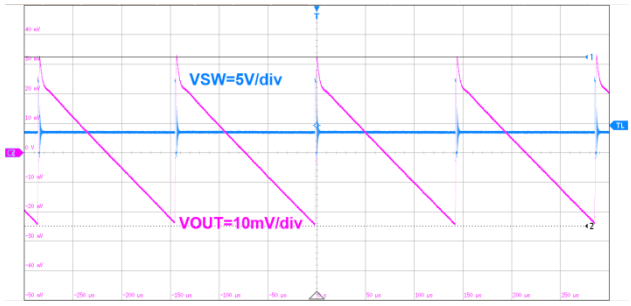
2us/div V_{OUT}=1.0V I_{OUT}=1.0A

Figure19. Output Ripple



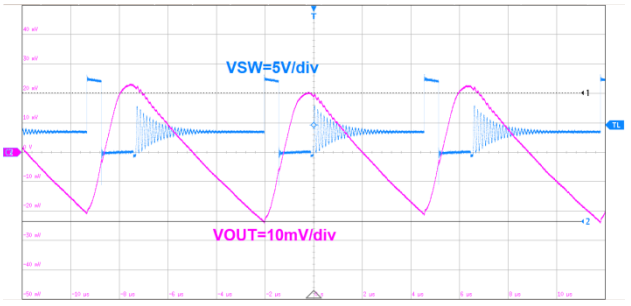
2us/div V_{OUT}=1.0V I_{OUT}=3.0A

Figure20. Output Ripple



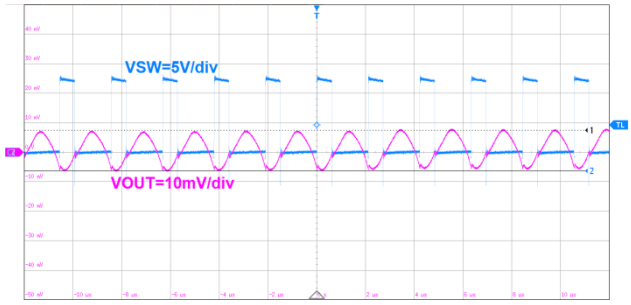
50us/div V_{OUT}=3.3V I_{OUT}=0.01A

Figure21. Output Ripple



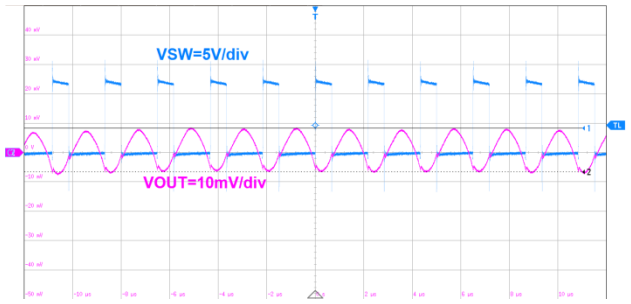
2us/div V_{OUT}=3.3V I_{OUT}=0.25A

Figure22. Output Ripple



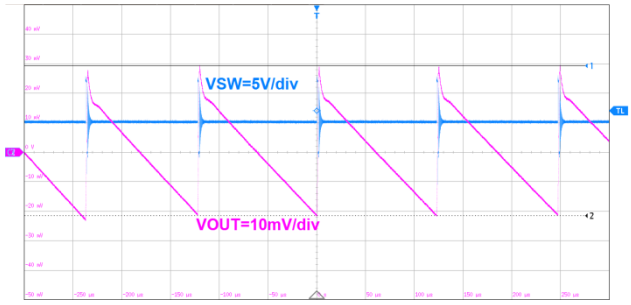
2us/div V_{OUT}=3.3V I_{OUT}=1.0A

Figure23. Output Ripple



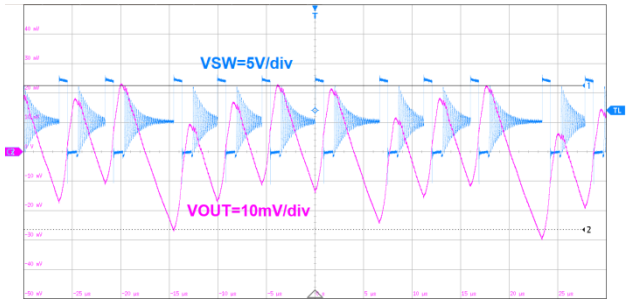
2us/div V_{OUT}=3.3V I_{OUT}=3.0A

Figure24. Output Ripple



50us/div V_{OUT}=5.0V I_{OUT}=0.01A

Figure25. Output Ripple

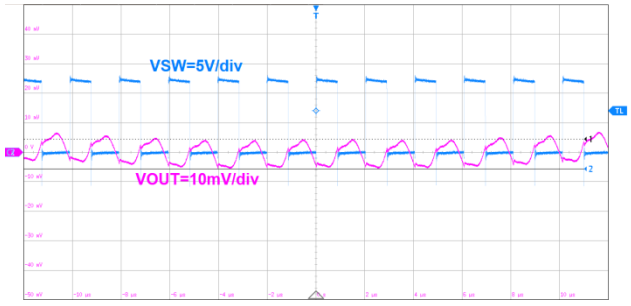


5us/div V_{OUT}=5.0V I_{OUT}=0.25A

Figure26. Output Ripple

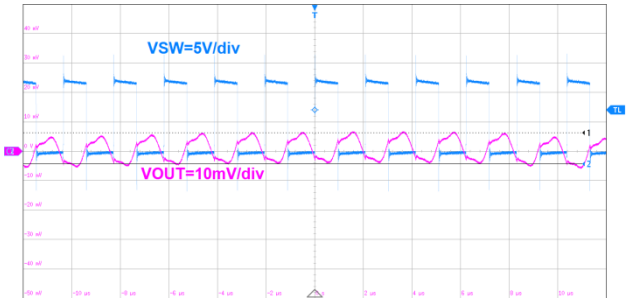
Application Curves(Continued)

V_{IN} = 12V (unless otherwise noted)



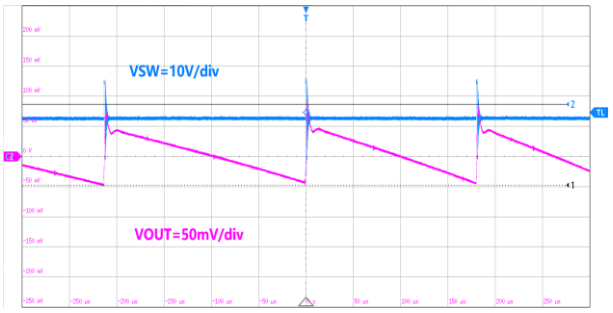
2us/div V_{OUT}=5.0V I_{OUT}=1.0A

Figure27. Output Ripple



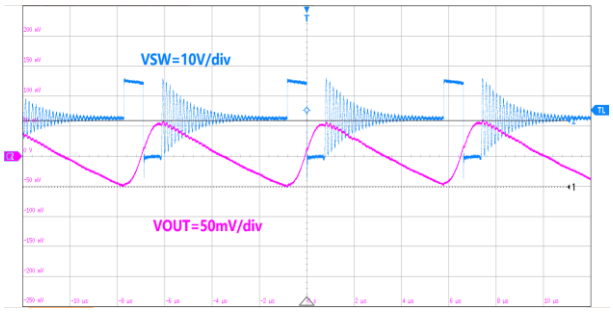
2us/div V_{OUT}=5.0V I_{OUT}=3.0A

Figure28. Output Ripple



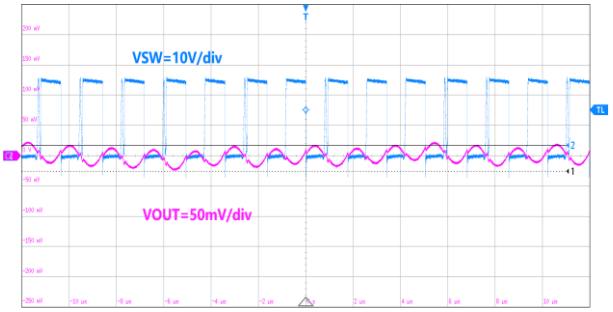
50us/div V_{OUT}=12.0V I_{OUT}=0.01A V_{IN}=24.0V

Figure29. Output Ripple



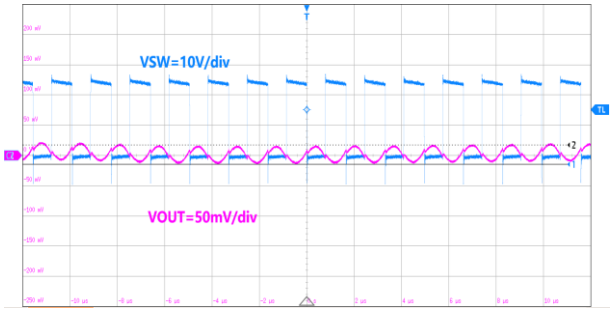
50us/div V_{OUT}=12.0V I_{OUT}=0.25A V_{IN}=24.0V

Figure30. Output Ripple



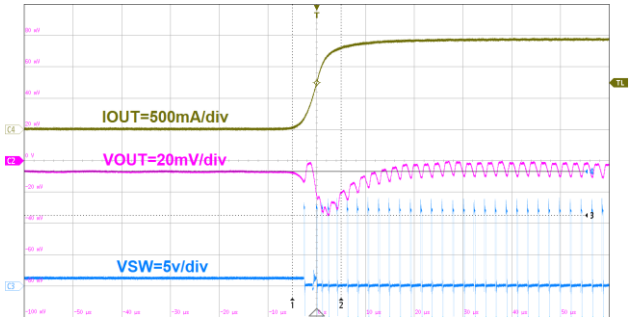
50us/div V_{OUT}=12.0V I_{OUT}=1.0A V_{IN}=24.0V

Figure31. Output Ripple



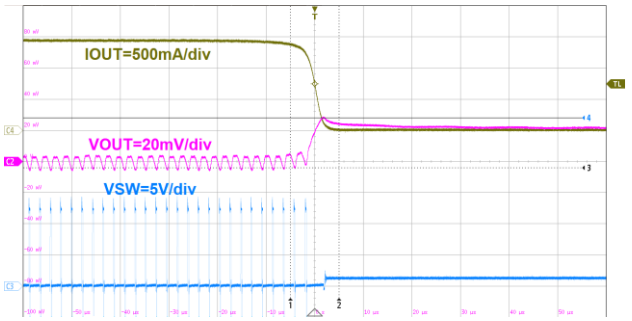
50us/div V_{OUT}=12.0V I_{OUT}=3.0A V_{IN}=24.0V

Figure32. Output Ripple



10us/div V_{OUT}=1.0V I_{OUT} =0A to 1.5A

Figure33. Load Transient

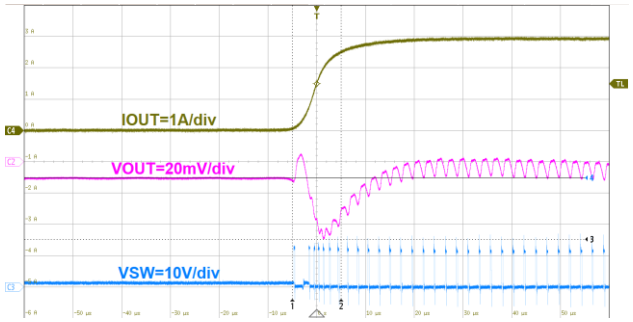


10us/div V_{OUT}=1.0V I_{OUT} =1.5A to 0A

Figure34. Load Transient

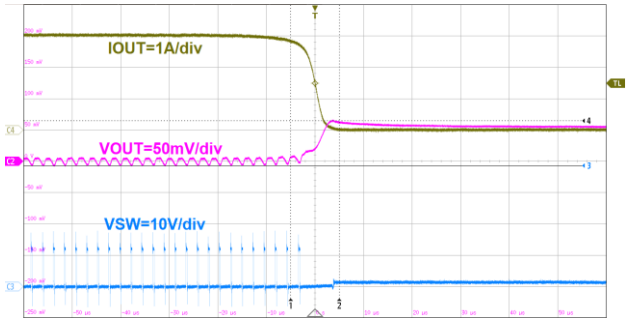
Application Curves(Continued)

V_{IN} = 12V (unless otherwise noted)



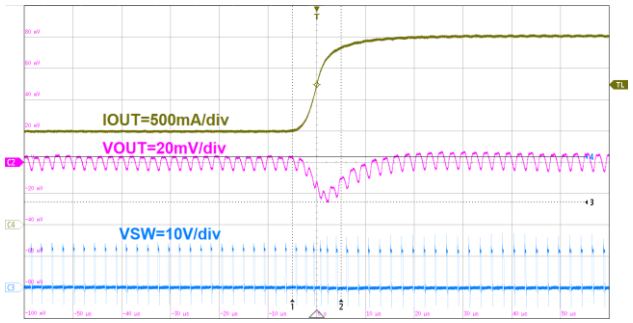
10us/div V_{OUT}=1.0V I_{OUT} =0A to 3A

Figure35. Load Transient



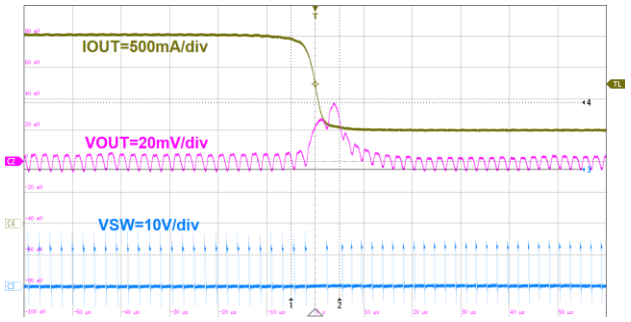
10us/div V_{OUT}=1.0V I_{OUT} =3A to 0A

Figure36. Load Transient



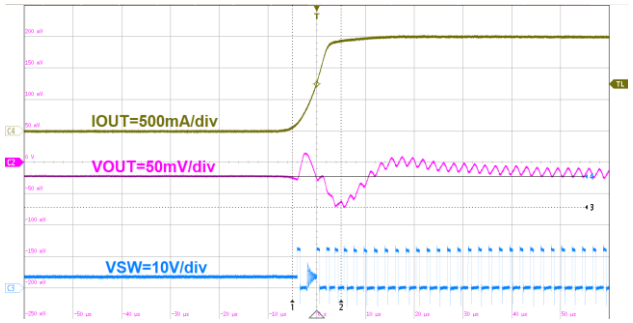
10us/div V_{OUT}=1.0V I_{OUT} =1.5A to 3A

Figure37. Load Transient



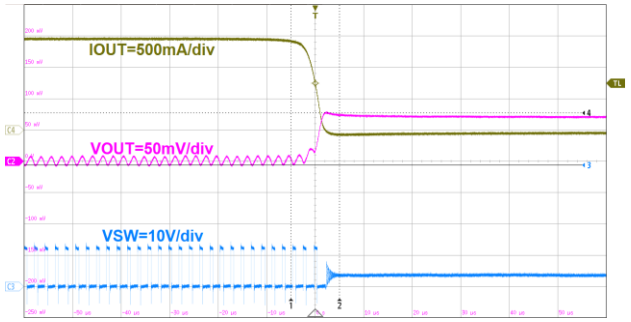
10us/div V_{OUT}=1.0V I_{OUT} =3A to 1.5A

Figure38. Load Transient



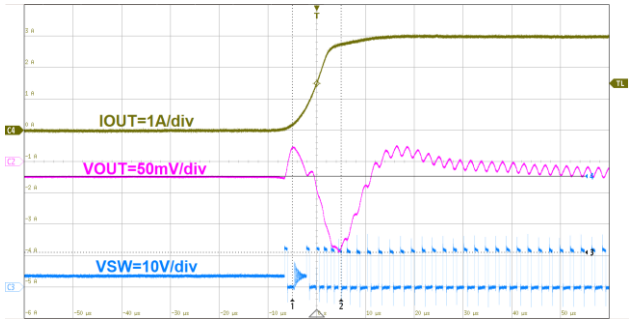
10us/div V_{OUT}=3.3V I_{OUT} =0A to 1.5A

Figure39. Load Transient



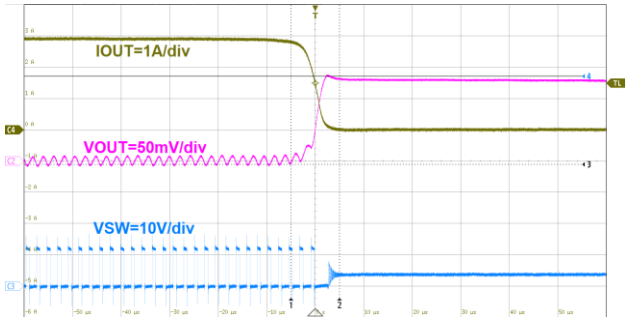
10us/div V_{OUT}=3.3V I_{OUT} =1.5A to 0A

Figure40. Load Transient



10us/div V_{OUT}=3.3V I_{OUT} =0A to 3A

Figure41. Load Transient

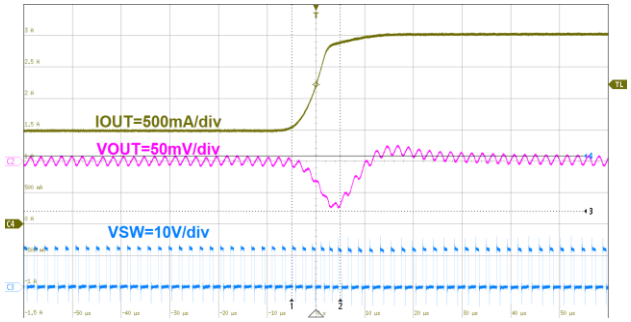


10us/div V_{OUT}=3.3V I_{OUT} =3A to 0A

Figure42. Load Transient

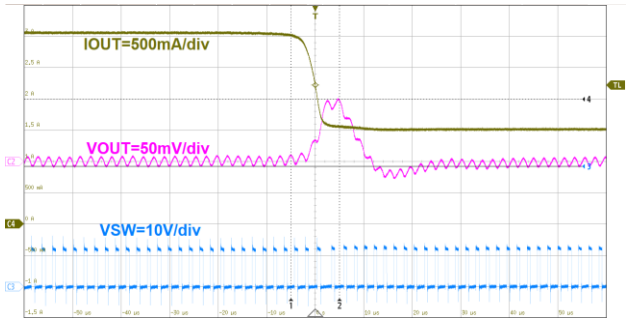
Application Curves(Continued)

V_{IN} = 12V (unless otherwise noted)



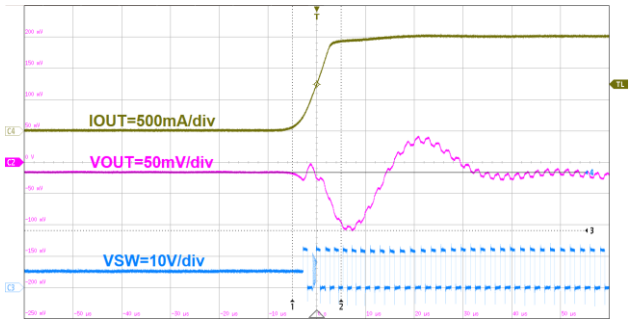
10us/div V_{OUT}=3.3V I_{OUT} =1.5A to 3A

Figure43. Load Transient



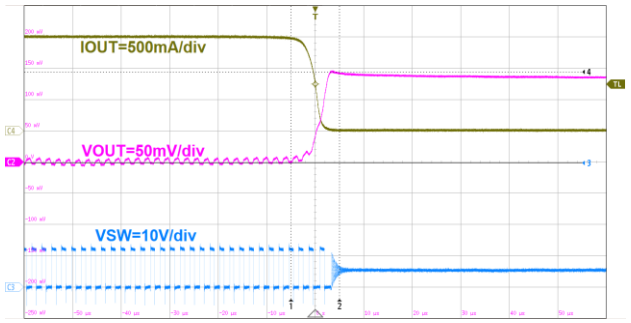
10us/div V_{OUT}=3.3V I_{OUT} =3A to 1.5A

Figure44. Load Transient



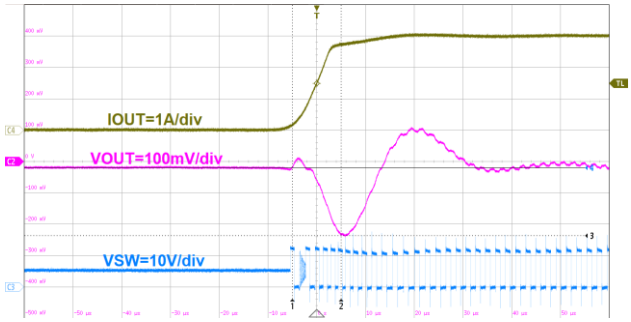
10us/div V_{OUT}=5.0V I_{OUT} =0A to 1.5A

Figure45. Load Transient



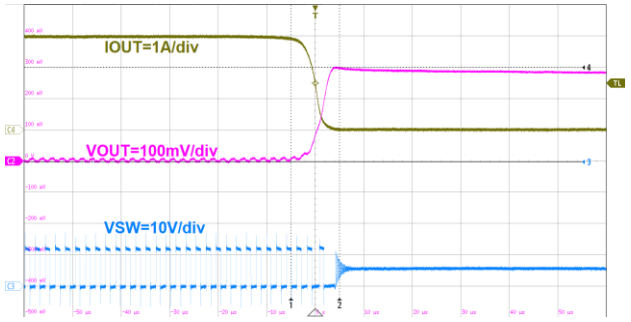
10us/div V_{OUT}=5.0V I_{OUT} =1.5A to 0A

Figure46. Load Transient



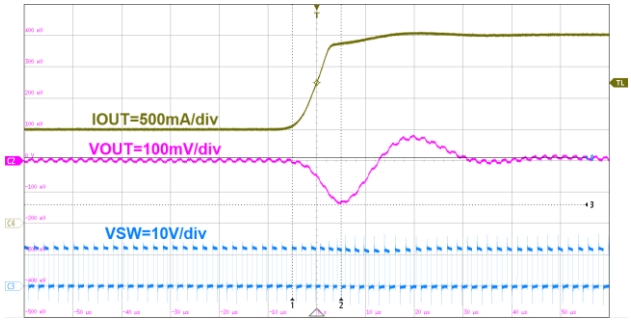
10us/div V_{OUT}=5.0V I_{OUT} =0A to 3A

Figure47. Load Transient



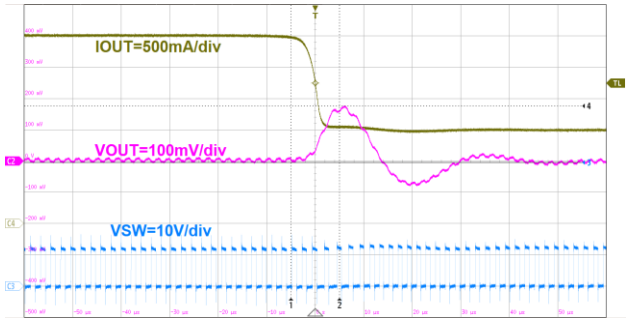
10us/div V_{OUT}=5.0V I_{OUT} =3A to 0A

Figure48. Load Transient



10us/div V_{OUT}=5.0V I_{OUT} =1.5A to 3A

Figure49. Load Transient

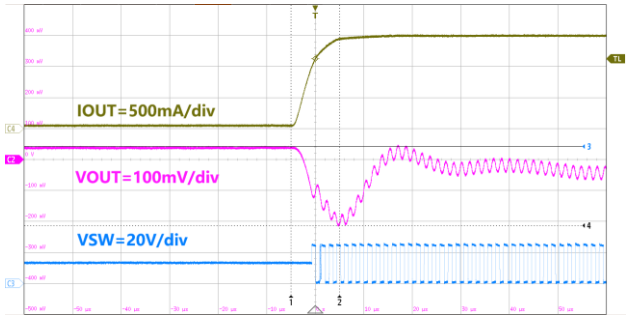


10us/div V_{OUT}=5.0V I_{OUT} =3A to 1.5A

Figure50. Load Transient

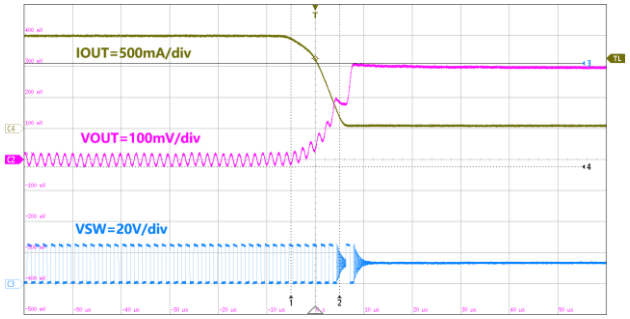
Application Curves(Continued)

V_{IN} = 12V (unless otherwise noted)



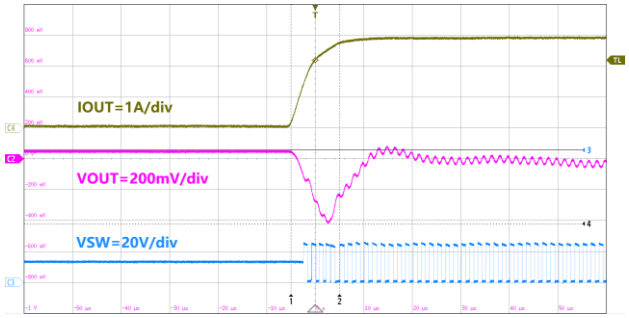
10us/div V_{OUT}=12.0V I_{OUT} =0A to 1.5A V_{IN}=24.0V

Figure51. Load Transient



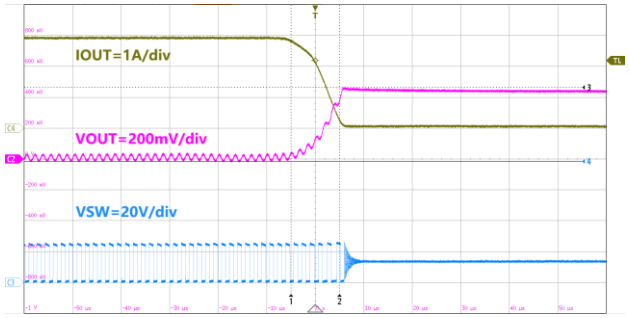
10us/div V_{OUT}=12.0V I_{OUT} =1.5A to 0A V_{IN}=24.0V

Figure52. Load Transient



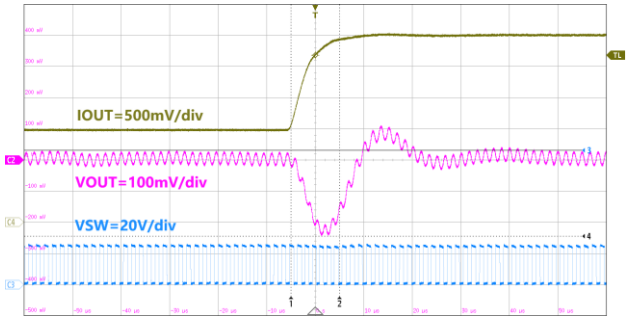
10us/div V_{OUT}=12.0V I_{OUT} =0A to 3A V_{IN}=24.0V

Figure53. Load Transient



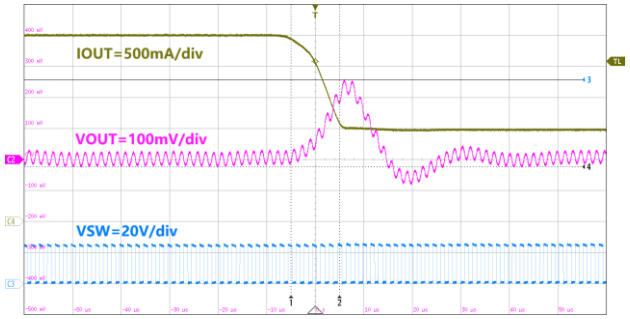
10us/div V_{OUT}=12.0V I_{OUT} =3A to 0A V_{IN}=24.0V

Figure54. Load Transient



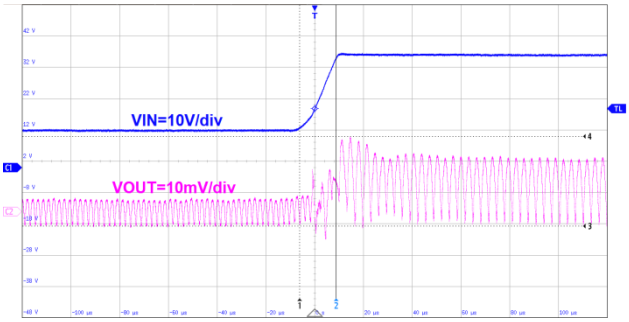
10us/div V_{OUT}=12.0V I_{OUT} =1.5A to 3A V_{IN}=24.0V

Figure55. Load Transient



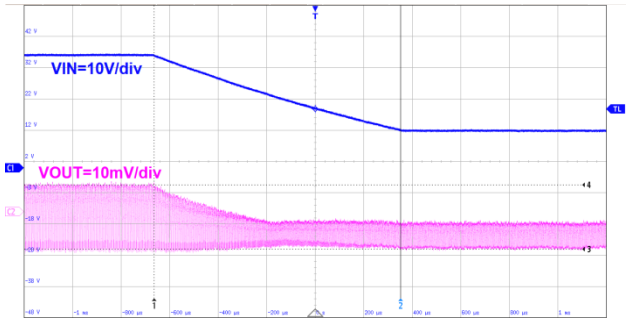
10us/div V_{OUT}=12.0V I_{OUT} =3A to 1.5A V_{IN}=24.0V

Figure56. Load Transient



20us/div V_{IN}=12V to 36V V_{OUT}=1.0V I_{OUT}=1.5A

Figure57. Line Transient

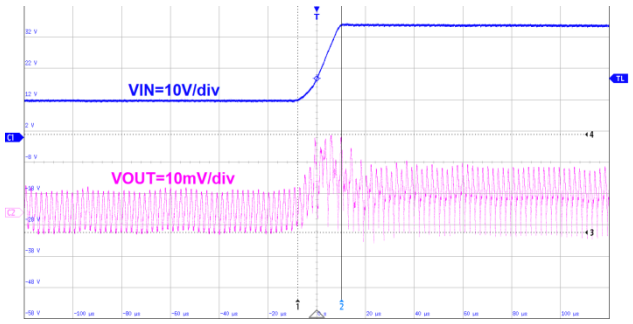


200us/div V_{IN}=36V to 12V V_{OUT}=1.0V I_{OUT}=1.5A

Figure58. Line Transient

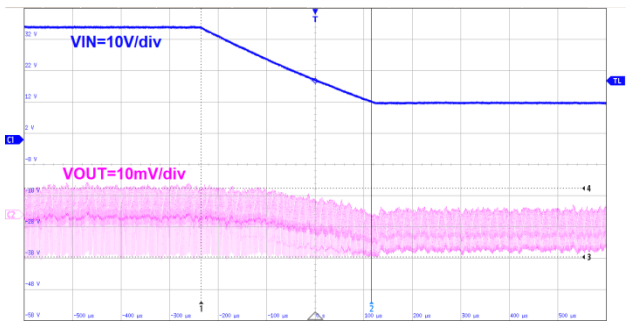
Application Curves(Continued)

V_{IN} = 12V (unless otherwise noted)



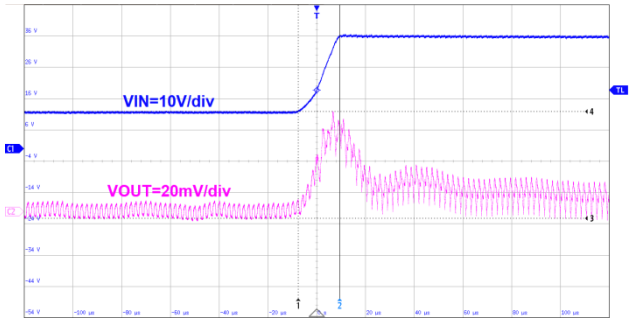
20us/div V_{IN}=12V to 36V V_{OUT}=3.3V I_{OUT}=1.5A

Figure59. Line Transient



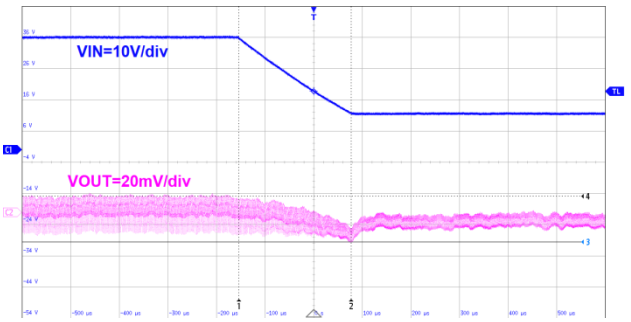
100us/div V_{IN}=36V to 12V V_{OUT}=3.3V I_{OUT}=1.5A

Figure60. Line Transient



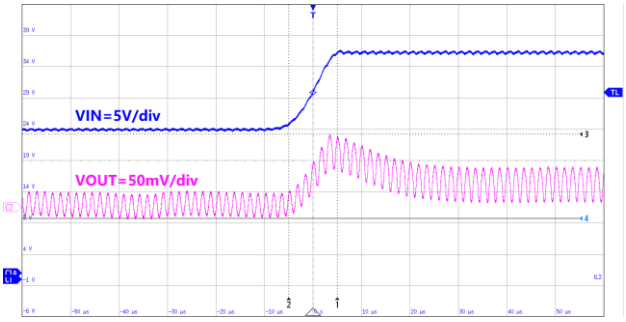
20us/div V_{IN}=12V to 36V V_{OUT}=5.0V I_{OUT}=1.5A

Figure61. Line Transient



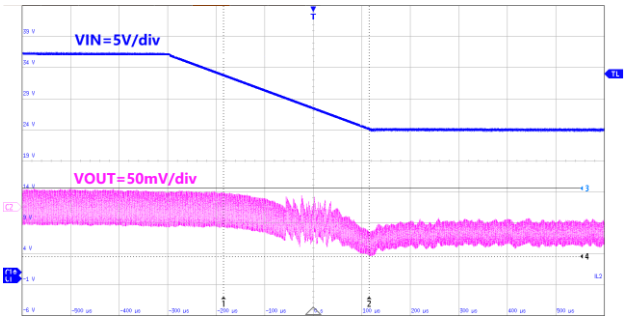
100us/div V_{IN}=36V to 12V V_{OUT}=5.0V I_{OUT}=1.5A

Figure62. Line Transient



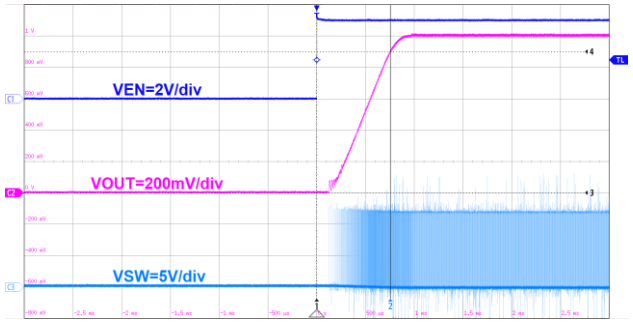
20us/div V_{IN}=24V to 36V V_{OUT}=12.0V I_{OUT}=1.5A

Figure63. Line Transient



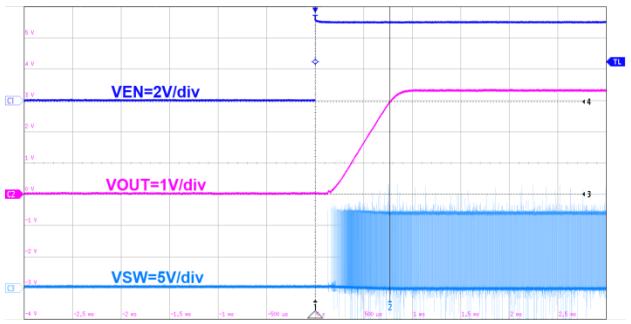
100us/div V_{IN}=24V to 36V V_{OUT}=12.0V I_{OUT}=1.5A

Figure64. Line Transient



500us/div V_{OUT}=1.0V I_{OUT}=3A

Figure65. Start-up by EN

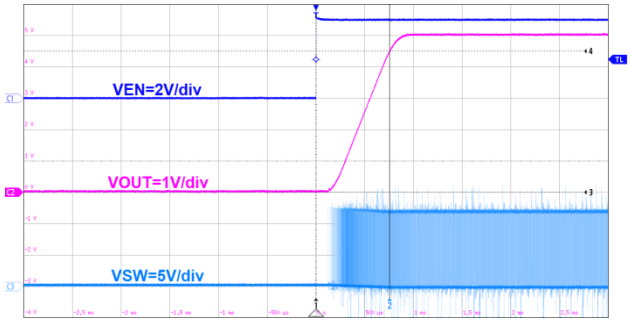


500us/div V_{OUT}=3.3V I_{OUT}=3A

Figure66. Start-up by EN

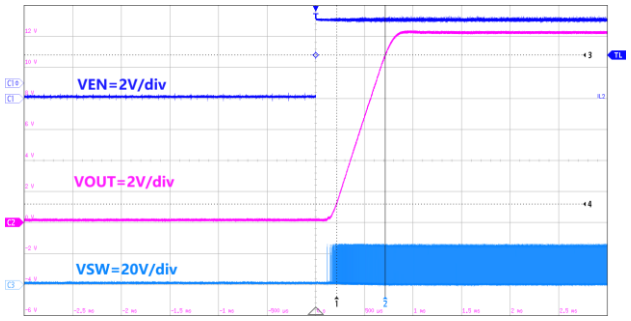
Application Curves(Continued)

V_{IN} = 12V (unless otherwise noted)



500us/div V_{OUT}=5.0V I_{OUT}=3A

Figure67. Start-up by EN

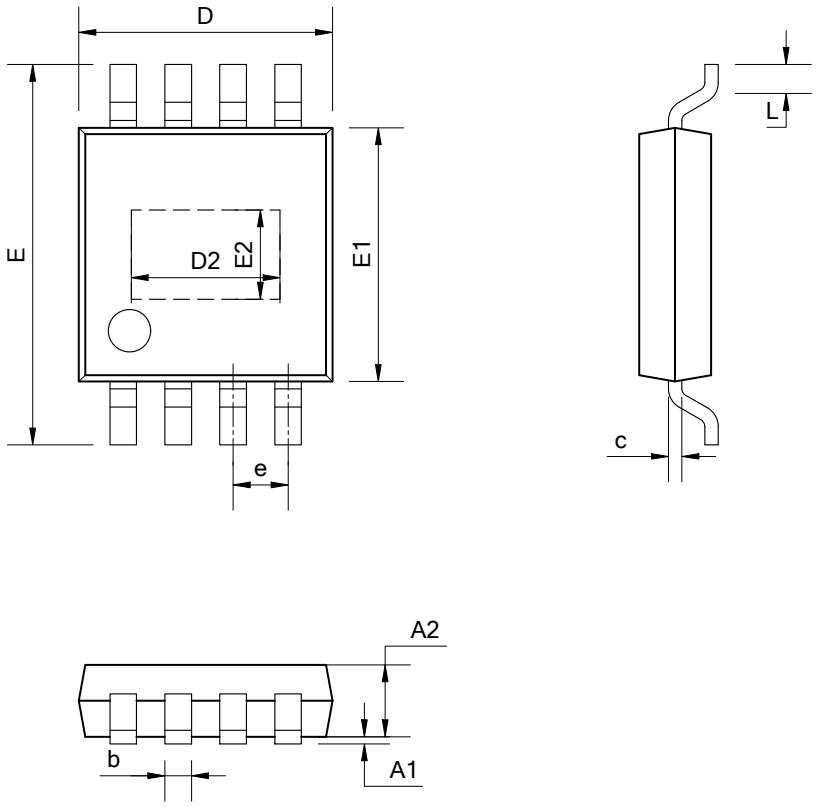


500us/div V_{OUT}=12.0V I_{OUT}=3A V_{IN}=24.0V

Figure68. Start-up by EN

Package Dimension

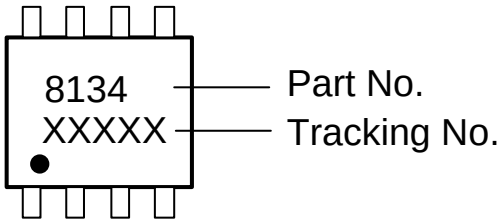
ESOP8



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A1	0.00	-	0.15
A2	1.35	1.40	1.50
b	0.38	-	0.47
c	0.17	-	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
D2	3.02	3.17	3.32
E1	3.80	3.90	4.00
E2	2.13	2.28	2.43
e	1.17	1.27	1.37
L	0.45	0.60	0.80

Marking



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.1	2022.6.17	Preliminary Version	Xie Lin Han	Xie Lin Han	Liu Jia Yin
0.2	2022.11.7	Update Typeset	Shibo	Xie Lin Han	Liu Jia Yin
0.3	2023.4.27	Update Fsw and Modified error	Shibo	Xie Lin Han	Liu Jia Yin
1.0	2023.7.23	Official Version	LiuCong	Xie Lin Han	Xie Lin Han
1.1	2024.04.14	Update Electrical Characteristics	LiuCong	Xie Lin Han	Xie Lin Han
1.2	2025.1.16	Add Thermal Properties	LiuCong	Xie Lin Han	Xie Lin Han
1.3	2025.2.13	Update Hiccup time and UVLO_Hys	Wuhs	Xie Lin Han	Xie Lin Han
1.4	2025.3.22	Update 12V output voltage parameters	LiuCong	Xie Lin Han	Xie Lin Han
1.5	2025.05.09	Add Inductor Selection	CaoJiachen	Xie Lin Han	Liu Jia Yin