Single D-type Flip-Flop with Set and Reset; Positive Edge Trigger

General Description

The ET74LVC1G74 is a single positive edge triggered D-type flip-flop with individual data (D), clock (CP), set ($\overline{SD}$) and reset ($\overline{RD}$) inputs, and complementary Q and $\overline{Q}$ outputs. Data at the D-input that meets the set-up and hold time requirements on the Low-to-High clock transition will be stored in the flip-flop and appear at the Q output. Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in mixed 3.3V and 5V environments.

Schmitt trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging back-flow current through the device when it is powered down.

Features

- Wide Supply Voltage Range from 1.65V to 5.5V
- Over Voltage Tolerant Inputs to 5.5V
- High Noise Immunity
- ±24mA Output Drive (V_{CC} = 3.0V)
- CMOS Low Power Consumption
- Direct Interface with TTL Levels
- I_{OFF} Circuitry Provides Partial Power-down Mode Operation
- ESD Protection Exceeds JESD22
  - 4000V Human-Body Model (A114-A)
  - 1500V Charged-Device Model (C101)
- Latch-up Performance Exceeds 200mA per JESD78, Class II

Applications

- Server
- LED Display Screen
- Network Switches
- Telecommunications Infrastructure
- Motor Driver
- I/O Extender

Ordering Information

Part No.	Package	Packing Option	MSL
ET74LVC1G74V	TSSOP8	Tape and Reel, 4K	3

Pin Configuration

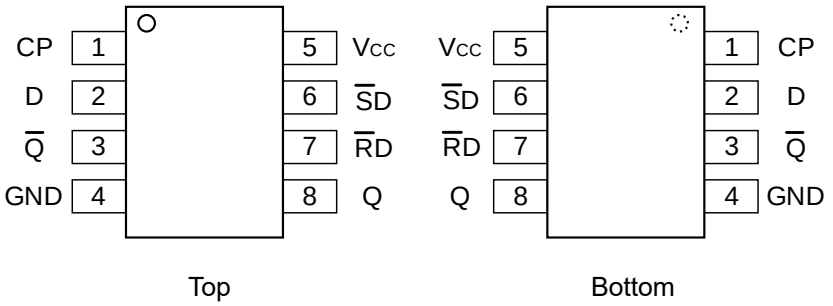


Fig 1. Top View & Bottom View

Pin Function

Pin No.	Pin Name	Pin Function
1	CP	Clock Input (Low-to-High, Edge-Triggered)
2	D	Data Input
3	$\overline{Q}$	Complement Output
4	GND	Ground
5	Q	True Output
6	$\overline{RD}$	Asynchronous Reset-direct Input (Active Low)
7	$\overline{SD}$	Asynchronous Set-direct Input (Active Low)
8	V_{CC}	Supply Voltage

Functional Diagram

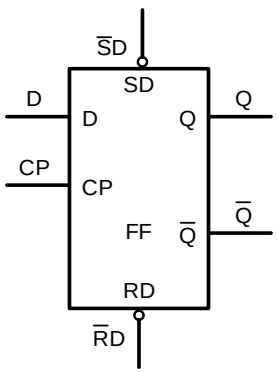


Fig 2. Logic Symbol

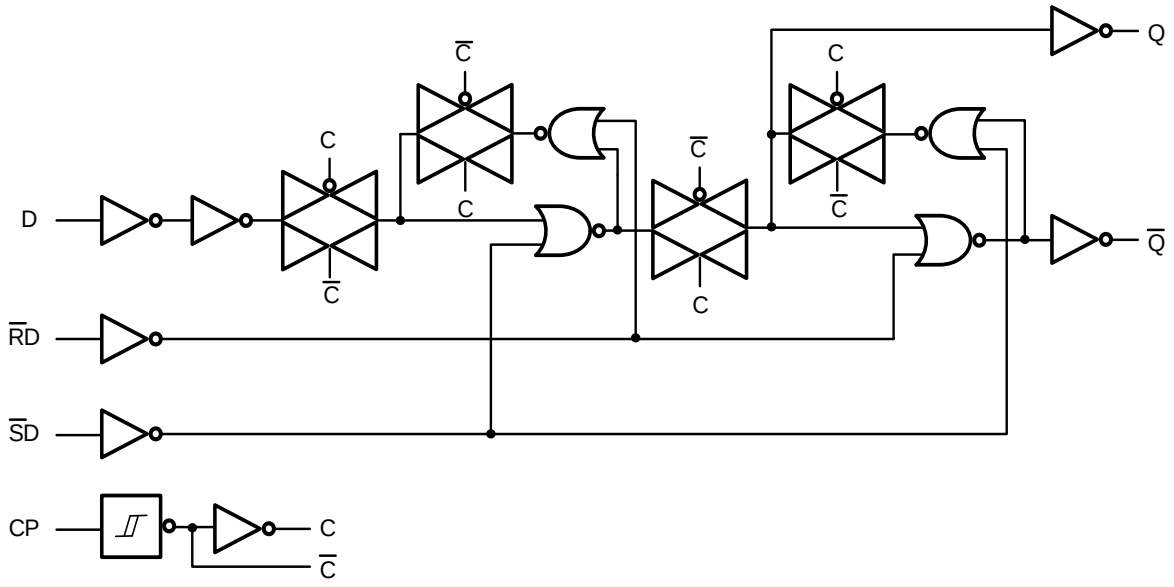


Fig 3. Logic Diagram

Functional Description

Table 1. Function Table for Asynchronous Operation

H = High voltage level; L = Low voltage level; X = Don't care.

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

Table 2. Function Table for Synchronous Operation

H = High voltage level; L = Low voltage level; ↑ = Low-to-High CP transition;

Q_{n+1} = state after the next Low-to-High CP transition.

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage		-0.5~+6.5	V
I_{IK}	Input Clamping Current	V_I < 0V	-50	mA
V_I	Input Voltage (1)		-0.5~+6.5	V
I_{OK}	Output Clamping Current	V_O > 0V or V_O < 0V	±50	mA
V_O	Output Voltage	Active Mode (1)	-0.5~V_{CC}+0.5	V
		Power-Down Mode V_{CC}=0V (1)	-0.5~+6.5	V
I_O	Output Current	V_O = 0V to V_{CC}	±50	mA
I_{CC}	Supply Current		+100	mA
I_{GND}	Ground Current		-100	mA
T_J	Operating Junction Range		-40 to +150	°C
T_{STG}	Storage Temperature		-65 to +150	°C
V_{ESD}	Human Body Mode (2)		±4000	V
	Charged Device Mode (3)		±1500	V
I_{LU}	Latch-up Current (4)		±200	mA

Note1:I_O absolute maximum rating must be observed.

Note2: HBM tested per EIA/JESD22-A114−A;

Note3: CDM tested per EIA/JESD22-C101;

Note4: Latch-up Current Maximum Rating tested per EIA/JESD78E;

Recommended Operating Conditions

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage		1.65~5.5	V
V_I	Input Voltage		0~5.5	V
V_O	Output Voltage	Active Mode	0~V_{CC}	V
		Power-Down Mode V_{CC}=0V	0~5.5	V
T_A	Ambient Temperature		-40 to +125	°C
Δt/ΔV	Input Transition Rise and Fall Rate	V_{CC} = 1.65V to 2.7V	<20	ns/V
		V_{CC} = 2.7V to 5.5V	<10	ns/V

Electrical Characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0V).

Symbol	Parameter	Conditions	−40°C ≤ T_A ≤ +85°C			−40°C ≤ T_A ≤ +125°C		Unit
			Min	Typ [5]	Max	Min	Max	
V_{IH}	High−Level Input Voltage	V_{CC} = 1.65V to 1.95V	0.65V_{CC}			0.65V_{CC}		V
		V_{CC} = 2.3V to 2.7V	1.7			1.7		
		V_{CC} = 2.7V to 3.6V	2.0			2.0		
		V_{cc} = 4.5V to 5.5V	0.7V_{CC}			0.7V_{CC}		
V_{IL}	Low−Level Input Voltage	V_{CC} = 1.65V to 1.95V			0.35V_{CC}		0.35V_{CC}	V
		V_{CC} = 2.3V to 2.7V			0.7		0.7	
		V_{CC} = 2.7V to 3.6V			0.8		0.8	
		V_{cc} = 4.5V to 5.5V			0.3V_{CC}		0.3V_{CC}	
V_{OH}	High-Level Output Voltage	V_I = V_{IH} or V_{IL}						V
		I_O = -100μA; V_{CC} = 1.65V to 5.5V	V_{CC} - 0.1			V_{CC} - 0.1		
		I_O = -4mA; V_{CC} = 1.65V	1.2	1.54		0.95		
		I_O = -8mA; V_{CC} = 2.3V	1.9	2.15		1.7		
		I_O = -12mA; V_{CC} = 2.7V	2.2	2.5		1.9		
		I_O = -24mA; V_{CC} = 3.0V	2.3	2.62		2.0		
		I_O = -32mA; V_{CC} = 4.5V	3.8	4.11		3.4		
V_{OL}	Low-Level Output Voltage	V_I = V_{IH} or V_{IL}						V
		I_O = -100μA; V_{CC} = 1.65V to 5.5V			0.10		0.10	
		I_O = 4mA; V_{CC} = 1.65V		0.07	0.45		0.70	
		I_O = 8mA; V_{CC} = 2.3V		0.09	0.30		0.45	
		I_O = 12mA; V_{CC} = 2.7V		0.16	0.40		0.60	
		I_O = 24mA; V_{CC} = 3.0V		0.17	0.55		0.80	
		I_O = 32mA; V_{CC} = 4.5V		0.18	0.55		0.80	
I_I	Input Leakage Current	V_I = 5.5V or GND; V_{CC} = 0V to 5.5V		±0.1	±5		±20	uA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V; V_{CC} = 0V		±0.1	±10		±20	uA
I_{CC}	Supply Current	V_I = 5.5V or GND; V_{CC} = 1.65V to 5.5V; I_O = 0A		0.1	10		40	uA
ΔI_{CC}	Additional Supply Current	Per pin; V_I = V_{CC} - 0.6V; I_O = 0A; V_{CC} =2.3V to 5.5V		5.0	500		500	uA
C_I	Input Capacitance			4.5				pF

Dynamic Characteristics

Voltages are referenced to GND (ground = 0V); for test circuit see Fig.6.

Symbol	Parameter	Conditions	−40°C ≤ T_A ≤ +85°C			−40°C ≤ T_A ≤ +125°C		Unit
			Min	Typ[5]	Max	Min	Max	
t_{pd}	Propagation Delay	CP to Q,$\overline{Q}$; See Fig.4						ns
		V_{CC} = 1.65V to 1.95V	1.5	8.1	13.4	1.5	17	
		V_{CC} = 2.3V to 2.7V	1.0	4.5	7.1	1.0	9.0	
		V_{CC} = 2.7V	1.0	4.4	7.1	1.0	9.0	
		V_{CC} = 3.0V to 3.6V	1.0	4.3	5.9	1.0	7.5	
		V_{CC} = 4.5V to 5.5V	1.0	2.5	4.1	1.0	5.5	
		$\overline{SD}$ to Q,$\overline{Q}$; See Fig.5						
		V_{CC} = 1.65V to 1.95V	1.5	7.8	12.9	1.5	17	
		V_{CC} = 2.3V to 2.7V	1.0	4.5	7.0	1.0	9.0	
		V_{CC} = 2.7V	1.0	4.1	7.0	1.0	9.0	
		V_{CC} = 3.0V to 3.6V	1.0	3.9	5.9	1.0	7.5	
		V_{CC} = 4.5V to 5.5V	1.0	2.4	4.1	1.0	5.5	
		$\overline{RD}$ to Q,$\overline{Q}$; See Fig.5						
		V_{CC} = 1.65V to 1.95V	1.5	7.0	12.9	1.5	17	
		V_{CC} = 2.3V to 2.7V	1.0	3.7	7.0	1.0	9.0	
		V_{CC} = 2.7V	1.0	3.6	7.0	1.0	9.0	
		V_{CC} = 3.0V to 3.6V	1.0	3.5	5.9	1.0	7.5	
		V_{CC} = 4.5V to 5.5V	1.0	2.0	4.1	1.0	5.5	
t_W	Pulse Width	CP High or Low; See Fig.4						ns
		V_{CC} = 1.65V to 1.95V	6.2			6.2		
		V_{CC} = 2.3V to 2.7V	2.7			2.7		
		V_{CC} = 2.7V	2.7			2.7		
		V_{CC} = 3.0V to 3.6V	2.7			2.7		
		V_{CC} = 4.5V to 5.5V	2.0			2.0		
		$\overline{SD}$ and $\overline{RD}$ Low; See Fig.5						
		V_{CC} = 1.65V to 1.95V	6.2			6.2		
		V_{CC} = 2.3V to 2.7V	2.7			2.7		
		V_{CC} = 2.7V	2.7			2.7		
		V_{CC} = 3.0V to 3.6V	2.7			2.7		
		V_{CC} = 4.5V to 5.5V	2.0			2.0		
t_{rec}	Recovery Time	$\overline{SD}$ and $\overline{RD}$; See Fig.5						ns
		V_{CC} = 1.65V to 1.95V	1.9			1.9		
		V_{CC} = 2.3V to 2.7V	1.4			1.4		
		V_{CC} = 2.7V	1.3			1.3		
		V_{CC} = 3.0V to 3.6V	1.2			1.2		
		V_{CC} = 4.5V to 5.5V	1.0			1.0		

Dynamic Characteristics (Continued)

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig.6; for wave forms see Fig.4 and Fig.5.

Symbol	Parameter	Conditions	−40°C ≤ T_A ≤ +85°C			−40°C ≤ T_A ≤ +125°C		Unit
			Min	Typ[5]	Max	Min	Max	
t_{su}	Set-up Time	D to CP; See Fig.4						ns
		V_{CC} = 1.65V to 1.95V	2.9			2.9		
		V_{CC} = 2.3V to 2.7V	1.7			1.7		
		V_{CC} = 2.7V	1.7			1.7		
		V_{CC} = 3.0V to 3.6V	1.3			1.3		
		V_{CC} = 4.5V to 5.5V	1.1			1.1		
t_h	Hold time	D to CP; See Fig.4						ns
		V_{CC} = 1.65V to 1.95V	1.5			1.5		
		V_{CC} = 2.3V to 2.7V	1.0			1.0		
		V_{CC} = 2.7V	1.0			1.0		
		V_{CC} = 3.0V to 3.6V	1.0			1.0		
		V_{CC} = 4.5V to 5.5V	1.0			1.0		
f_{max}	Maximum Frequency	CP; See Fig.4						MHz
		V_{CC} = 1.65V to 1.95V	80			80		
		V_{CC} = 2.3V to 2.7V	175			175		
		V_{CC} = 2.7V	175			175		
		V_{CC} = 3.0V to 3.6V	175			175		
		V_{CC} = 4.5V to 5.5V	200			200		
C_{PD} [6]	Power Dissipation Capacitance	V_I = GND to V_{CC}; V_{CC} = 3.3V		37				pF

Note5: All typical values are measured at T_A = 25°C and V_{CC} = 3.3V.

Note6: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = Input Frequency in MHz;

f_o = Output Frequency in MHz;

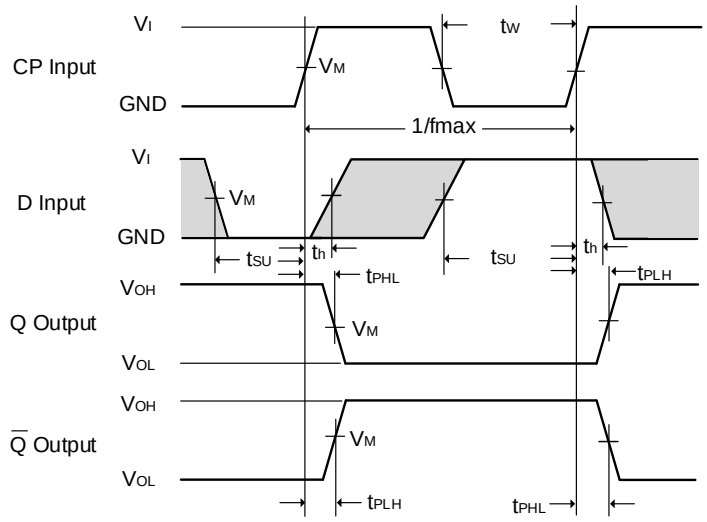
C_L = Output Load capacitance in pF;

V_{CC} = Supply Voltage in V;

N = Number of Inputs Switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of Outputs.

Test Circuit

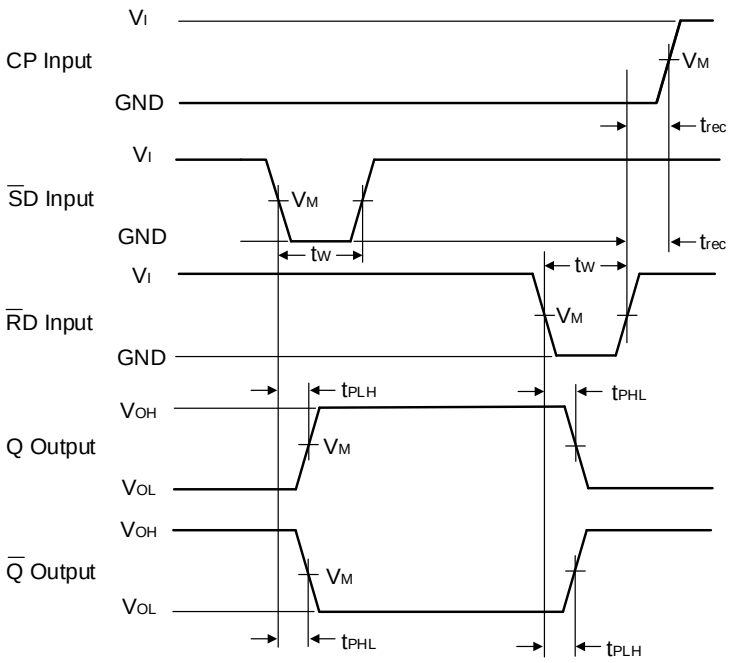


Measurement points are given in Table 3.

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig.4 The clock input (CP) to output (Q, $\overline{Q}$) propagation delays and pulse width, D to CP set-up, CP to D hold times and the maximum frequency



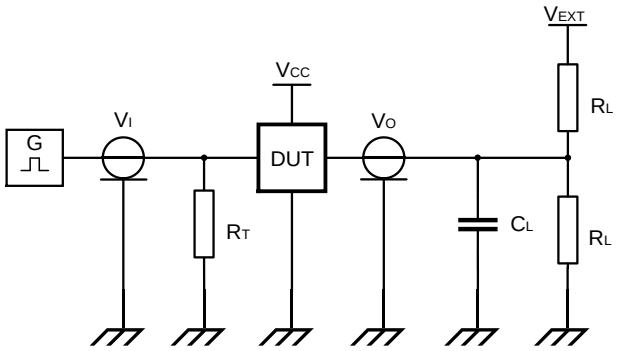
Measurement points are given in Table 3.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig.5 The set ($\overline{SD}$) and reset ($\overline{RD}$) input to output (Q, $\overline{Q}$) propagation delays, pulse widths and the $\overline{RD}$ to CP recovery time

Table 3.Measurement Points

Supply Voltage	Input	Output
V_{CC}	V_M	V_M
1.65V to 1.95V	0.5 × V_{CC}	0.5 × V_{CC}
2.3V to 2.7V	0.5 × V_{CC}	0.5 × V_{CC}
2.7V	1.5V	1.5V
3.0V to 3.6V	1.5V	1.5V
4.5V to 5.5V	0.5 × V_{CC}	0.5 × V_{CC}



Measurement points are given in Table 4.

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

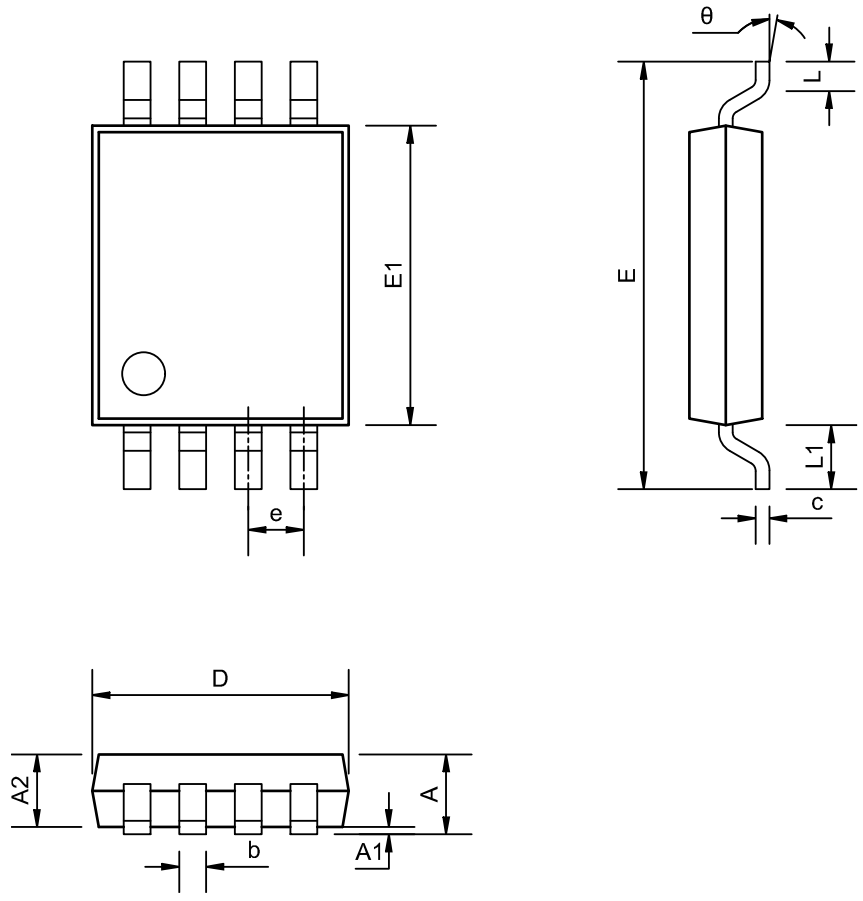
Fig.6 Test circuit for measuring switching times

Table 4. Test Data

Supply Voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r,t_f	C_L	R_L	t_{PLH} , t_{PHL}	t_{PZH} , t_{PHZ}	t_{PZL} , t_{PLZ}
1.65V to 1.95V	V_{CC}	≤ 2.0ns	30pF	1kΩ	Open	GND	2 × V_{CC}
2.3V to 2.7V	V_{CC}	≤ 2.0ns	30pF	500Ω	Open	GND	2 × V_{CC}
2.7V	2.7V	≤ 2.5ns	50pF	500Ω	Open	GND	6V
3.0V to 3.6V	2.7V	≤ 2.5ns	50pF	500Ω	Open	GND	6V
4.5V to 5.5V	V_{CC}	≤ 2.5ns	50pF	500Ω	Open	GND	2 × V_{CC}

Package Dimension

TSSOP8



COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.0	1.05	1.1
A1	0.00	0.07	0.15
A2	0.75	0.85	0.95
b	0.22	0.30	0.38
c	0.08	0.10	0.18
D	2.9	3.0	3.1
E	3.9	4.0	4.1
E1	2.9	3.0	3.1
e	0.65BSC		
L	0.33	0.40	0.47
L1	0.5REF		
θ	0°	4°	8°

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2024-02-06	Preliminary Version	Zhangzw	Tugz	Liujy
1.0	2025-03-29	Official Version	Wangar	Yangxx	Liujy
1.1	2025-05-27	Add Packing Option	Yang xiaoxu	Yang xiaoxu	Liu jiaying