

Single D-type Flip-flop Positive-edge Trigger

General Description

The ET74LVC1G80 is a single positive-edge triggered D-type flip-flop. Data at the D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and its complement will appear at the Q output.

Schmitt trigger action at all inputs makes the circuit tolerant of slower input rise and fall time.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging back-flow current through the device when it is powered down.

Features

- Wide Supply Voltage Range from 1.65V to 5.5V
- Over Voltage Tolerant Inputs to 5.5V
- High Noise Immunity
- $\pm 24\text{mA}$ Output Drive ($V_{CC} = 3.0\text{V}$)
- CMOS Low Power Consumption
- Direct Interface with TTL Levels
- I_{OFF} Circuitry Provides Partial Power-down Mode Operation
- ESD Protection Exceeds JESD22
 - 4000V Human-Body Model (A114-A)
 - 1500V Charged-Device Model (C101)
- Latch-up Performance Exceeds 200mA per JESD78, Class II

Applications

- Server
- LED Display Screen
- Network Switches
- Telecommunications Infrastructure
- Motor Driver
- I/O Extender

Ordering Information

Part No.	Package	Packing Option	MSL
ET74LVC1G80	SC70-5	Tape and Reel, 3K	1

ET74LVC1G80

Pin Configuration

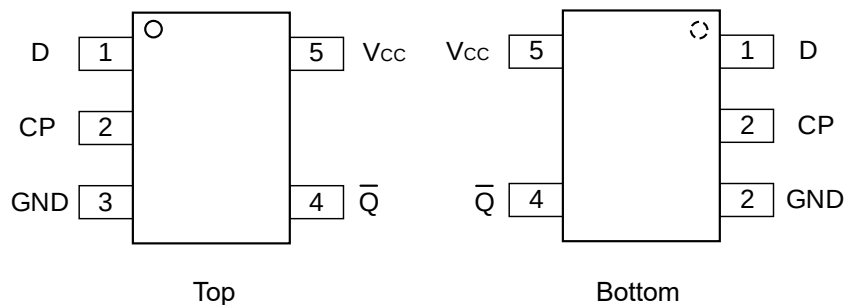


Fig 1. Top View & Bottom View

Pin Function

Pin No.	Function	Function
1	D	Data Input
2	CP	Ground
3	GND	Data Input
4	$\bar{Q}$	Data Output
5	VCC	Supply Voltage

Block Diagram

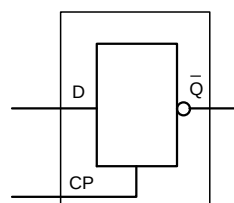


Fig 2. Logic Symbol

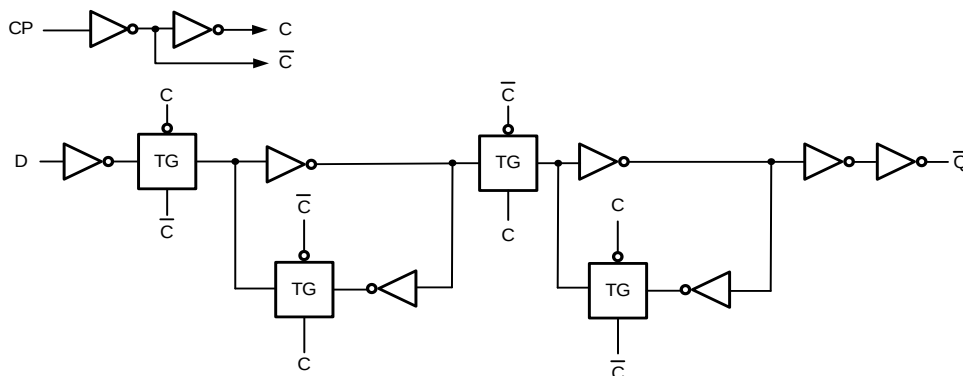


Fig 3. Logic Diagram

ET74LVC1G80

Function Table

H = High voltage level; L = Low voltage level; ↑ = Low-to-High CP transition; X = don't care;
 $\bar{q}$ = lower case letter indicates the state of referenced input, one set-up time prior to the LOW-to-HIGH CP transition.

Input		Output
CP	D	$\bar{Q}$
↑	L	H
↑	H	L
L	X	$\bar{q}$

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage		-0.5~+6.5	V
I_{IK}	Input Clamping Current	$V_I < 0V$	-50	mA
V_I	Input Voltage ⁽¹⁾		-0.5~+6.5	V
I_{OK}	Output Clamping Current	$V_O > 0V$ or $V_O < 0V$	±50	mA
V_O	Output Voltage	Active Mode ⁽¹⁾	-0.5~ $V_{CC}+0.5$	V
		Power-Down Mode $V_{CC}=0V$ ⁽¹⁾	-0.5~+6.5	V
I_O	Output Current	$V_O = 0V$ to V_{CC}	±50	mA
I_{CC}	Supply Current		+100	mA
I_{GND}	Ground Current		-100	mA
T_J	Operating Junction Range		-40 to +150	°C
T_{STG}	Storage Temperature		-65 to +150	°C
V_{ESD}	Human Body Mode ⁽²⁾		±4000	V
	Charged Device Mode ⁽³⁾		±1500	V
I_{LU}	Latch-up Current ⁽⁴⁾		±200	mA

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per EIA/JESD22-A114-A;

Note3: CDM tested per EIA/JESD22-C101;

Note4: Latch-up Current Maximum Rating tested per EIA/JESD78E;

Recommended Operating Conditions

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage		1.65~5.5	V
V_I	Input Voltage		0~5.5	V
V_O	Output Voltage	Active Mode	0~ V_{CC}	V
		Power-Down Mode $V_{CC}=0V$	0~5.5	V
T_A	Ambient Temperature		-40 to +125	°C
$\Delta t/\Delta V$	Input Transition Rise and Fall Rate	$V_{CC} = 1.65V$ to $2.7V$	<20	ns/V
		$V_{CC} = 2.7V$ to $5.5V$	<10	ns/V

ET74LVC1G80

Electrical Characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Sym bol	Parameter	Conditions	-40°C ≤ T _A ≤ +85°C			-40°C ≤ T _A ≤ +125°C		Unit
			Min	Typ ⁽⁵⁾	Max	Min	Max	
V _{IH}	High-Level Input Voltage	V _{CC} = 1.65V to 1.95V	0.65V _{CC}			0.65V _{CC}		V
		V _{CC} = 2.3V to 2.7V	1.7			1.7		
		V _{CC} = 2.7V to 3.6V	2.0			2.0		
		V _{CC} = 4.5V to 5.5V	0.7V _{CC}			0.7V _{CC}		
V _{IL}	Low-Level Input Voltage	V _{CC} = 1.65V to 1.95V			0.35V _{CC}		0.35V _{CC}	V
		V _{CC} = 2.3V to 2.7V			0.7		0.7	
		V _{CC} = 2.7V to 3.6V			0.8		0.8	
		V _{CC} = 4.5V to 5.5V			0.3V _{CC}		0.3V _{CC}	
V _{OH}	High-Level Output Voltage	V _I = V _{IH} or V _{IL}						V
		I _O = -100μA; V _{CC} = 1.65V to 5.5V	V _{CC} - 0.1			V _{CC} - 0.1		
		I _O = -4mA; V _{CC} = 1.65V	1.2	1.54		0.95		
		I _O = -8mA; V _{CC} = 2.3V	1.9	2.15		1.7		
		I _O = -12mA; V _{CC} = 2.7V	2.2	2.5		1.9		
		I _O = -24mA; V _{CC} = 3.0V	2.3	2.62		2.0		
		I _O = -32mA; V _{CC} = 4.5V	3.8	4.11		3.4		
V _{OL}	Low-Level Output Voltage	V _I = V _{IH} or V _{IL}						V
		I _O = -100μA; V _{CC} = 1.65V to 5.5V			0.10		0.10	
		I _O = 4mA; V _{CC} = 1.65V		0.07	0.45		0.70	
		I _O = 8mA; V _{CC} = 2.3V		0.09	0.30		0.45	
		I _O = 12mA; V _{CC} = 2.7V		0.16	0.40		0.60	
		I _O = 24mA; V _{CC} = 3.0V		0.17	0.55		0.80	
		I _O = 32mA; V _{CC} = 4.5V		0.18	0.55		0.80	
I _I	Input Leakage Current	V _I = 5.5V or GND; V _{CC} = 0V to 5.5V		±0.1	±5		±20	μA
I _{OFF}	Power-Off Leakage Current	V _I or V _O = 5.5V; V _{CC} = 0V		±0.1	±10		±20	μA
I _{CC}	Supply Current	V _I = 5.5V or GND; V _{CC} = 1.65V to 5.5V; I _O = 0A		0.1	10		40	μA
ΔI _{CC}	Additional Supply Current	V _I = V _{CC} - 0.6V; I _O = 0A; V _{CC} = 2.3V to 5.5V		5.0	500		500	μA
C _I	Input Capacitance			5.0				pF

ET74LVC1G80

Dynamic Characteristics

Voltages are referenced to GND (ground = 0V); for test circuit see Fig.6.

Symbol	Parameter	Conditions	-40°C ≤ T _A ≤ +85°C			-40°C ≤ T _A ≤ +125°C		Unit
			Min	Typ ⁽⁵⁾	Max	Min	Max	
t _{pd}	Propagation Delay	CP to $\overline{Q}$; See Fig.4						ns
		V _{CC} = 1.65V to 1.95V	1.5	8.6	13.4	1.5	17	
		V _{CC} = 2.3V to 2.7V	1.0	5.0	7.1	1.0	9.0	
		V _{CC} = 2.7V	1.0	4.5	7.1	1.0	9.0	
		V _{CC} = 3.0V to 3.6V	1.0	4.4	5.7	1.0	7.5	
		V _{CC} = 4.5V to 5.5V	1.0	3.0	4.0	1.0	5.5	
t _w	Pulse Width	CP High or Low; See Fig.4						ns
		V _{CC} = 1.65V to 1.95V	3			3.0		
		V _{CC} = 2.3V to 2.7V	2.5			2.5		
		V _{CC} = 2.7V	2.5			2.5		
		V _{CC} = 3.0V to 3.6V	2.5			2.5		
		V _{CC} = 4.5V to 5.5V	2.0			2.0		
t _{su}	Set-up Time	D to CP; See Fig.4						ns
		V _{CC} = 1.65V to 1.95V	2.5			2.5		
		V _{CC} = 2.3V to 2.7V	1.7			1.7		
		V _{CC} = 2.7V	1.7			1.7		
		V _{CC} = 3.0V to 3.6V	1.3			1.2		
		V _{CC} = 4.5V to 5.5V	1.2			1.2		
t _h	Hold time	D to CP; See Fig.4						ns
		V _{CC} = 1.65V to 1.95V	0			0		
		V _{CC} = 2.3V to 2.7V	0			0		
		V _{CC} = 2.7V	0.5			0.5		
		V _{CC} = 3.0V to 3.6V	0.5			0.5		
		V _{CC} = 4.5V to 5.5V	0.5			0.5		
f _{max}	Maximum Frequency	CP; See Fig.4						MHz
		V _{CC} = 1.65V to 1.95V	160			160		
		V _{CC} = 2.3V to 2.7V	160			160		
		V _{CC} = 2.7V	160			160		
		V _{CC} = 3.0V to 3.6V	160			160		
		V _{CC} = 4.5V to 5.5V	200			200		
C _{PD} ⁽⁵⁾	Power Dissipation Capacitance	V _I = GND to V _{CC} ; V _{CC} = 3.3V		25				pF

Note5: All typical values are measured at T_A = 25°C and V_{CC} = 3.3V.

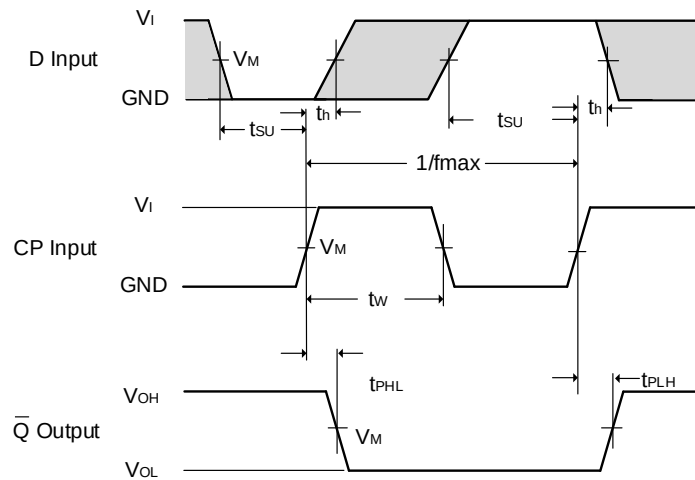
Note6: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

ET74LVC1G80

f_i = Input Frequency in MHz;
 f_o = Output Frequency in MHz;
 C_L = Output Load capacitance in pF;
 V_{CC} = Supply Voltage in V;
 N = Number of Inputs Switching;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of Outputs.

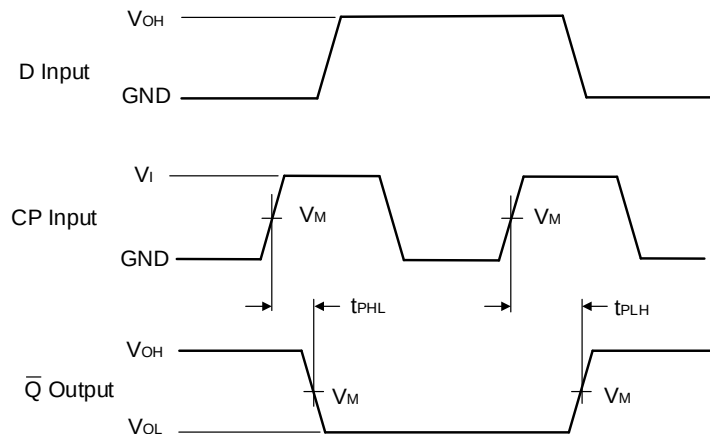
Test Circuit



Measurement points are given in [Table 1](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output.

Fig.4 Clock (CP) to output ($\bar{Q}$) propagation delay times, clock pulse width, D to CP set-up times, CP to D hold times and maximum clock pulse frequency



Measurement points are given in [Table 1](#).

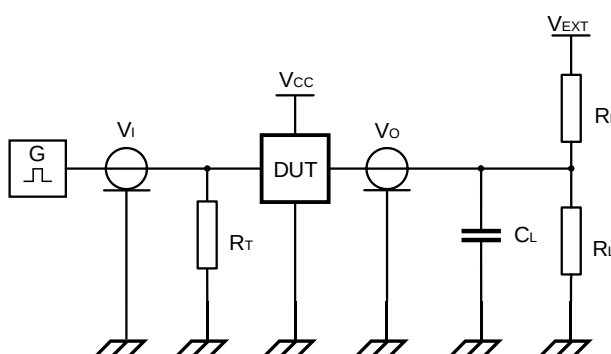
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig.5 Clock (CP) to output ($\bar{Q}$) propagation delay times

ET74LVC1G80

Table 1. Measurement Points

Supply Voltage	Input	Output
V_{CC}	V_M	V_M
1.65V to 1.95V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3V to 2.7V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7V	1.5V	1.5V
3.0V to 3.6V	1.5V	1.5V
4.5V to 5.5V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Measurement points are given in [Table 2](#).

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Fig.6 Test circuit for measuring switching times

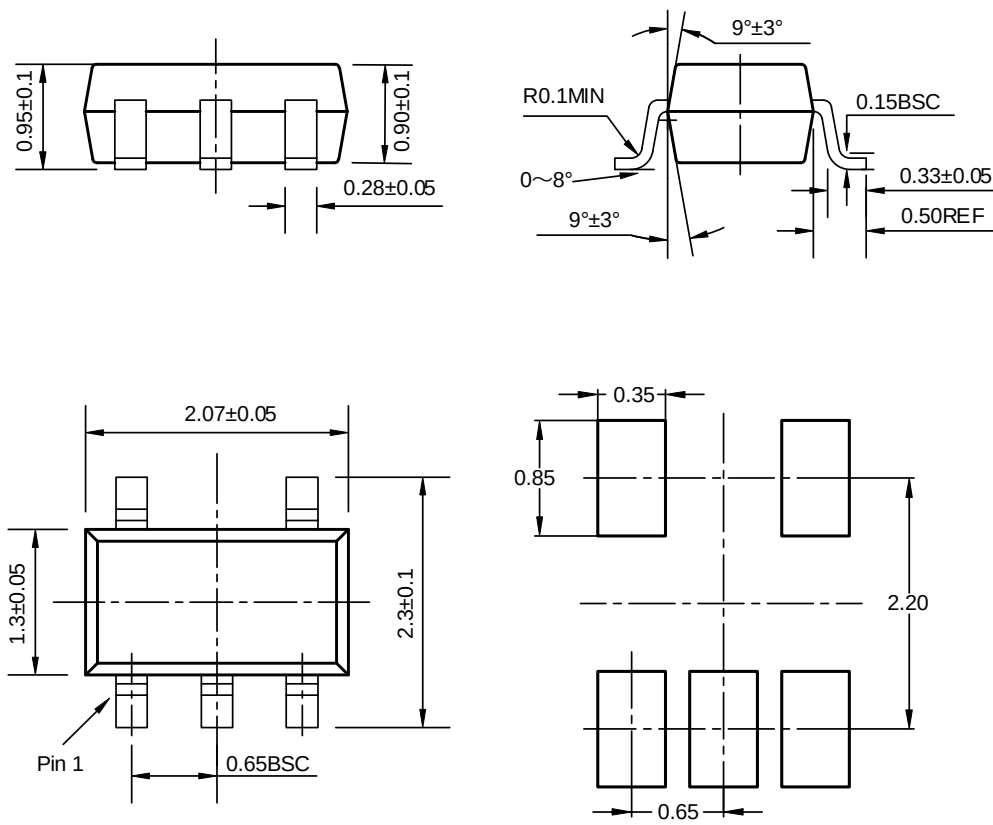
Table 2. Test Data

Supply Voltage	Input		Load		V_{EXT}
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}
1.65V to 1.95V	V_{CC}	$\leq 2.0ns$	30pF	1k Ω	Open
2.3V to 2.7V	V_{CC}	$\leq 2.0ns$	30pF	500 Ω	Open
2.7V	2.7V	$\leq 2.5ns$	50pF	500 Ω	Open
3.0V to 3.6V	2.7V	$\leq 2.5ns$	50pF	500 Ω	Open
4.5V to 5.5V	V_{CC}	$\leq 2.5ns$	50pF	500 Ω	Open

ET74LVC1G80

Package Dimension

SC70-5



Recommended Land Pattern

Unit: mm

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2024.7.4	Preliminary Version	Maruijie	Luhao	Liujiaying
1.0	2025-03-29	Official Version	Wangar	Yangxx	Liuji
1.1	2025-05-30	Add Packing Option	Yang xiaoxu	Yang xiaoxu	Liu jiaying