

High-Speed USB 2.0(480Mbps) Switch

General Description

The ET7222 is a 2CH single-pole/double-throw (SPDT) switches. Their wide bandwidth and low bit-to-bit skew allow them to pass high-speed differential signals with good signal integrity.

Each switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. Industry-leading advantages include a propagation delay of less than 250 ps, resulting from its low channel resistance and low I/O capacitance. Their high channel-to-channel crosstalk rejection results in minimal noise interference. Their bandwidth is wide enough to pass High-Speed USB 2.0 differential signals (480 Mb/s).

ET7222 is offered in a QFN10L and MSOP10 package.

Features

- R_{ON} is typically $6.0\ \Omega$ @ $V_{CC} = 3.3\ V$
- Low Bit-to-Bit skew is typically 50 ps
- Low crosstalk is typical -37 dB @ 250 MHz
- Low current consumption is 1.0 μA typical
- Near-zero propagation delay is typical 250 ps
- Channel on-capacitance is 8.0 pF typical
- V_{CC} Operating Range from 1.65 V to 4.7 V
- $\geq 750\ MHz$ bandwidth (or data frequency)
- Part No. and package

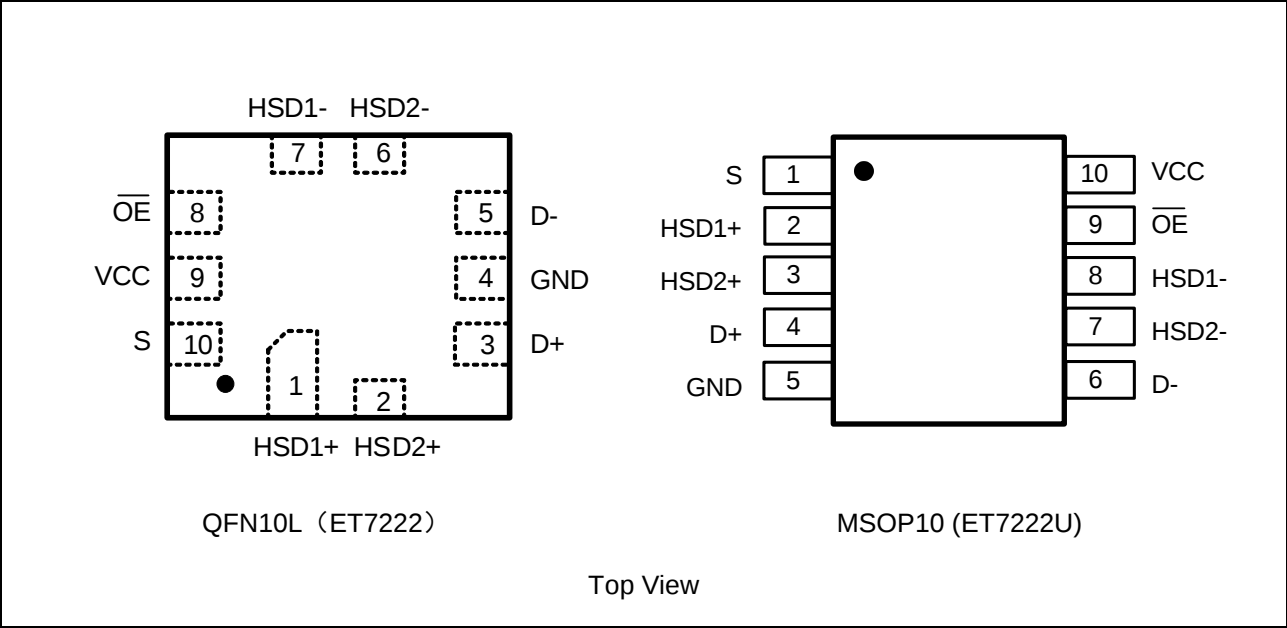
Part No.	Package	MSL
ET7222	QFN10L(1.8 mm×1.4 mm)	Level 1
ET7222U	MSOP10(4.9 mm×3.0 mm)	Level 1

Applications

- Differential Signal Data Routing
- USB 2.0 Signal Routing

ET7222

Pin Configuration



Pin Function

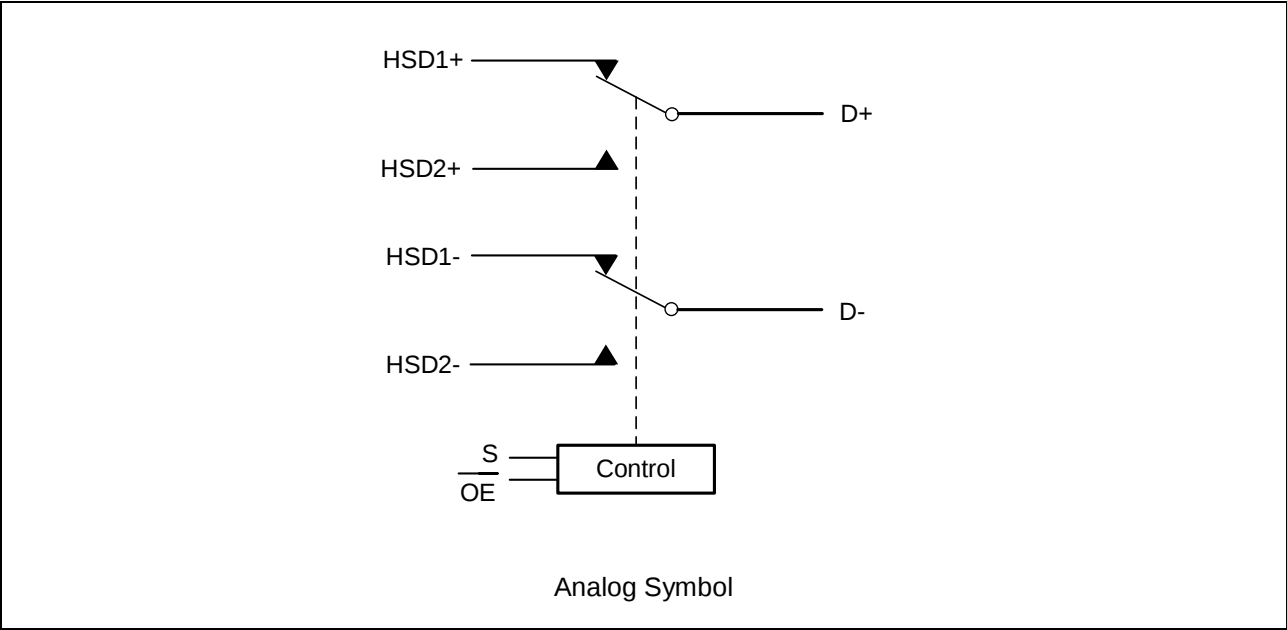
Pin NO.		Pin Name	Pin Function
ET7222 QFN10L	ET7222U MSOP10		
1	2	HSD1+	Data Ports
2	3	HSD2+	Data Ports
3	4	D+	Data Ports
4	5	GND	Ground
5	6	D-	Data Ports
6	7	HSD2-	Data Ports
7	8	HSD1	Data Ports
8	9	$\overline{OE}$	Output Enable
9	10	VCC	Power supply
10	1	S	Select Input

ET7222

Truth Table

OE	S	HSD1+ to D+, HSD1- to D-	HSD2+ to D+, HSD2- to D-
1	X	OFF	OFF
0	0	ON	OFF
0	1	OFF	ON

Analog Symbol



ET7222

Absolute Maximum Ratings

Symbol	Pins	Parameters	Value	Unit
V _{CC}	V _{CC}	Positive DC Supply Voltage	-0.5 to +5.5	V
V _{IS}	HSD1+,HSD1-,HSD2+,HSD2-	Analog Signal Voltage	-0.5 to V _{CC} +0.3	V
	D+,D-		-0.5 to +5.5	
V _{IN}	$\overline{\text{OE}}$	Control Input Voltage	-0.5 to +5.5	V
I _{CC}	V _{CC}	Positive DC Supply Current	50	mA
I _{IS_CON}	HSD1+,HSD1-,HSD2+,HSD2- D+,D-	Analog Signal Continuous Current-Closed Switch	± 100	mA
I _{IS_PK}	HSD1+,HSD1-,HSD2+,HSD2- D+,D-	Analog Signal Continuous Current 10% Duty Cycle	± 150	mA
I _{IN}	$\overline{\text{OE}}$	Control Input Current	± 20	mA
T _J		Junction Temperature Range	-40 to +150	°C
T _{STG}		Storage Temperature	-65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Symbol	Pins	Parameter	Min	Max	Unit
V _{CC}		Positive DC Supply Voltage	1.65	4.7	V
V _{IS}	HSD1+,HSD1-,HSD2+,HSD2-	Analog Signal Voltage	GND	V _{CC}	V
	D+,D-		GND	4.7	
V _{IN}	$\overline{\text{OE}}$	Digital Select Input Voltage	GND	V _{CC}	V
T _A		Operating Temperature Range	-40	+85	°C

Minimum and maximum values are guaranteed through test or design across the Recommended Operating Conditions, where applicable. Typical values are listed for guidance only and are based on the particular conditions listed for section, where applicable. These conditions are valid for all values found in the characteristics tables unless otherwise specified in the test conditions.

ET7222

DC Electrical Characteristics

Control Input (Typical: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 3.3\text{ V}$)

Symbol	Pins	Parameter	Conditions	V_{CC} (V)	-40°C to +85°C			unit
					Min	Typ	Max	
V_{IH}	$\overline{OE}$	Control Input High Voltage ⁽¹⁾		2.7 3.3 4.2	1.3 1.4 1.6	-	-	V
V_{IL}	$\overline{OE}$	Control Input Low Voltage ⁽¹⁾		2.7 3.3 4.2	-	-	0.4 0.4 0.5	V
I_{IN}	$\overline{OE}$	Control Input Leakage Current	$0 \leq V_{IS} \leq V_{CC}$	1.65 ~ 4.7	-	-	± 1.0	μA

Note1: V_{IH} level is recommended to be consistent with V_{CC} and V_{IL} level is GND to reduce I_{CC} current.

Supply And Leakage Current (Typical: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 3.3\text{ V}$, $\overline{OE} = V_{CC}$ or GND, $S = V_{CC}$ or GND)

Symbol	Pins	Parameter	Conditions	V_{CC} (V)	-40°C to +85°C		unit
					Min	Max	
I_{CC}	V_{CC}	Quiescent Supply Current	$V_{IS} = V_{CC}$ or GND; $I_{OUT} = 0\text{ A}$	1.65 ~ 4.7		1.0	μA
I_{CCT}	V_{CC}	Increase in I_{CC} per Control Voltage	$V_{IN} = 2.6\text{ V}$	3.6		10	μA
I_{OZ}	HSD1+ HSD1- HSD2+ HSD2-	OFF Stage Leakage Current	$0 \leq V_{IS} \leq V_{CC}$	1.65 ~ 4.7		± 1.0	μA
I_{OFF}	D+, D-	Power OFF Leakage Current	$0 \leq V_{IS} \leq 4.7\text{ V}$	0		± 1.0	μA

High Speed On Resistance (Typical: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 3.3\text{ V}$)

Symbol	Pins	Parameter	Conditions	V_{CC} (V)	-40°C to +85°C			unit
					Min	Typ	Max	
R_{ON}		On-Resistance	$V_{IS} = 0.2\text{ V}$, 0.4 V $I_{ON} = 8\text{ mA}$	2.7 3.3 4.2	-	6.5 6.0 5.5	12 10 8	Ω
R_{FLAT}		On-Resistance Flatness		2.7 3.3 4.2	-	0.3 0.2 0.1	1.5 1 0.5	Ω
ΔR_{ON}		On-Resistance Matching		2.7 3.3 4.2	-	0.25 0.2 0.15	0.5 0.45 0.4	Ω

ET7222

Full Speed On Resistance (Typical: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 3.3\text{ V}$)

Symbol	Pins	Parameter	Conditions	V_{CC} (V)	-40°C to +85°C			unit
					Min	Typ	Max	
R_{ON}		On-Resistance	$V_{IS}=0.2V_{CC}$, 0.5 V_{CC} ,	2.7 3.3 4.2	-	9.0 7.5 6.0	12.5 10.5 8.5	Ω
ΔR_{ON}		On-Resistance Matching	0.8 V_{CC} , V_{CC} $I_{ON} = 8\text{ mA}$	2.7 3.3 4.2	-	0.5 0.4 0.3	0.8 0.7 0.6	Ω
R_{FLAT}		On-Resistance Flatness	$V_{IS}=0.2\text{V}$, 0.4V, 0.7V,1.0V $I_{ON} = 8\text{ mA}$	2.7 3.3 4.2	-	1.0 0.5 0.4	3 1.5 1.2	Ω

AC Electrical Characteristics

Timing / Frequency (Typical: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 3.3\text{ V}$, $R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$)

Symbol	Pins	Parameter	Conditions	V_{CC} (V)	-40°C to +85°C			unit
					Min	Typ	Max	
t_{ON}	Closed to Open	Turn-ON Time		2.7 ~ 4.7	-	14	30	ns
t_{OFF}	Open to Closed	Turn-OFF Time		2.7 ~ 4.7	-	22	30	ns
t_{BBM}		Break-Before-Make Delay	$V_{IS} = 0\text{ V}$ to V_{CC}	2.7 ~ 4.7	2	8	-	ns
BW		-3 dB Bandwidth	$C_L = 5\text{ pF}$	2.7 ~ 4.7	-	550	-	MHz
			$C_L = 0\text{ pF}$		-	750	-	

Isolation (Typical: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 3.3\text{ V}$, $R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$)

Symbol	Pins	Parameter	Conditions	V_{CC} (V)	-40°C to +85°C			unit
					Min	Typ	Max	
O_{IRR}	Open	OFF-Isolation	$f = 250\text{ MHz}$	1.65 ~ 4.7	-	-25	-	dB
X_{TALK}	HSD1+ to HSD1-	Non-Adjacent Channel Crosstalk	$f = 250\text{ MHz}$	1.65 ~ 4.7	-	-37	-	dB

Capacitance (Typical: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 3.3\text{ V}$, $f = 1\text{ MHz}$)

Symbol	Pins	Parameter	Conditions	V_{CC} (V)	-40°C to +85°C			unit
					Min	Typ	Max	
C_{IN}	$\overline{OE}$	Control Pin Input Capacitance		0		1.8		pF
C_{ON}	D+ to HSD1/2+	ON Capacitance	$V_{OE} = 0\text{ V}$	3.3		8.0		pF
C_{OFF}	HSD2+, HSD2-	OFF Capacitance	$V_{IS} = 3.3\text{ V}$ $V_{OE} = 3.3\text{ V}$	3.3		3.5		pF

Typical Characteristics

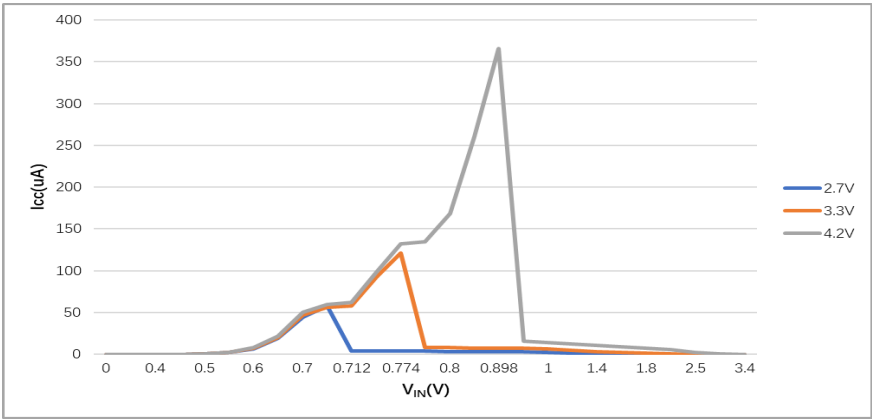
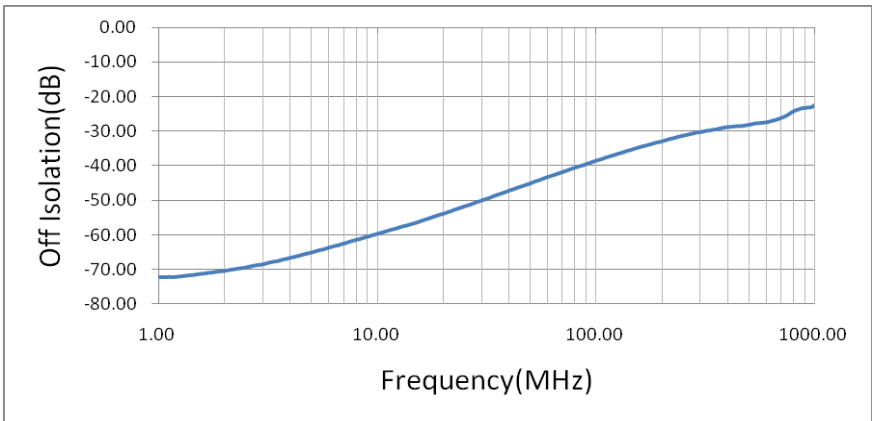
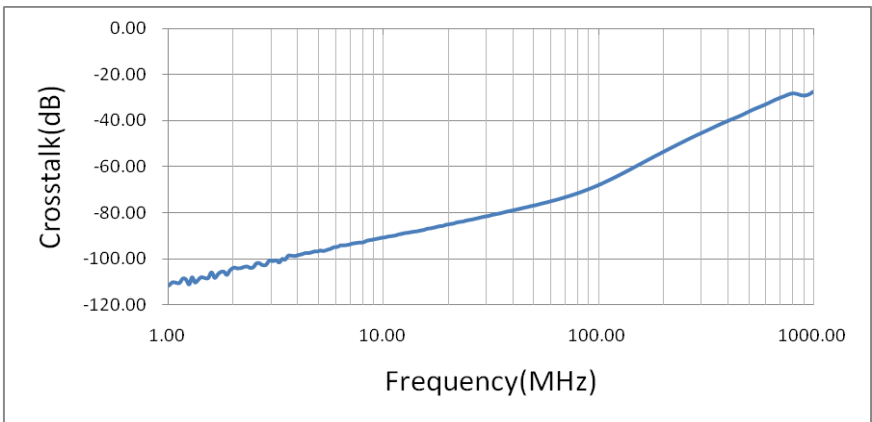


Figure1-a. I_{CC} vs. V_{IN}



OFF-ISOLATION

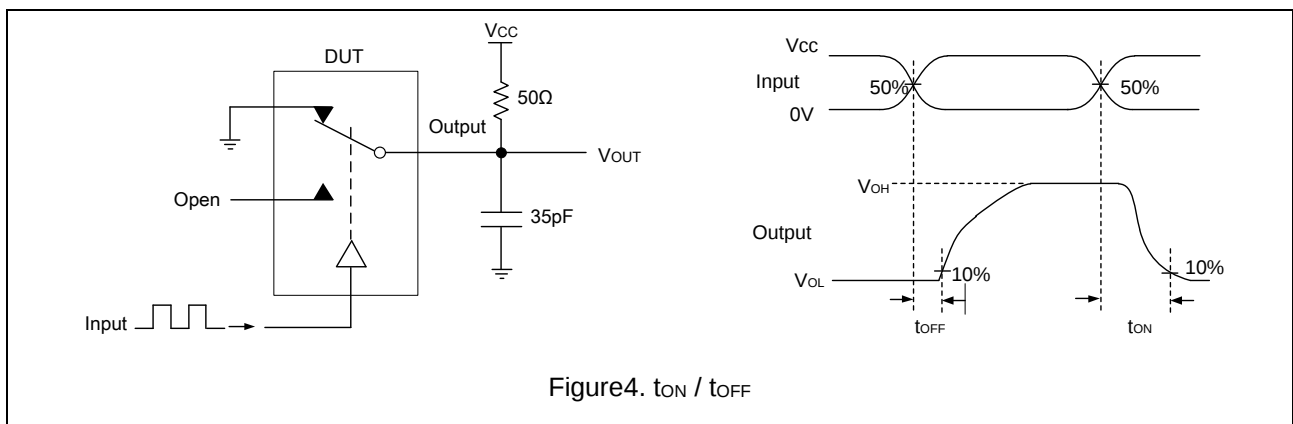
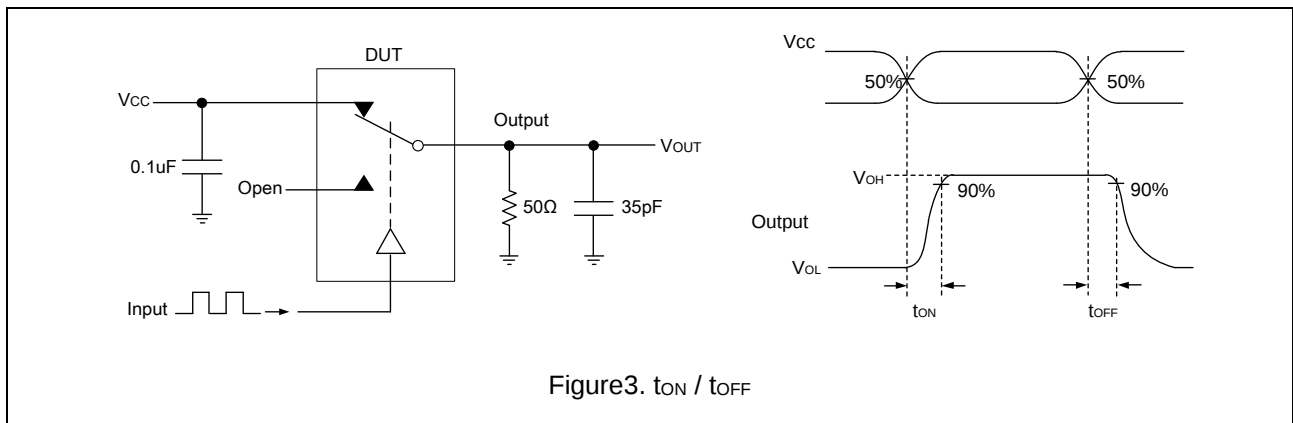
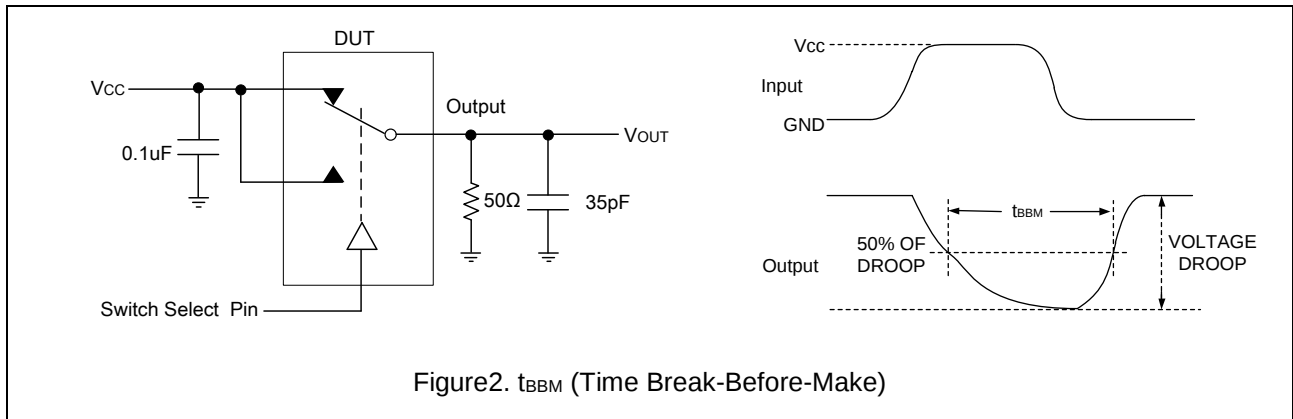
Figure1-b. Response vs. Frequency



CROSSTALK

Figure1-c. Response vs. Frequency

Test Circuit and Waveform



Test Circuit and Waveform(Continued)

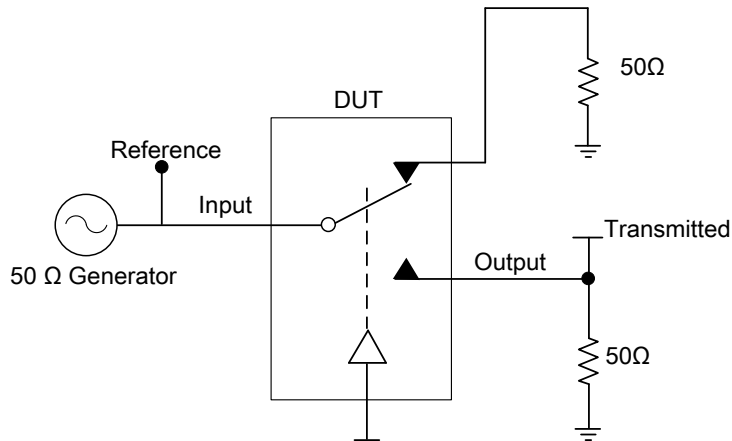


Figure5. Off Channel Isolation/On Channel Loss(BW)/Crosstalk
(On Channel to Off Channel)/ V_{ONL}

Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \log \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz.}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \log \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz.}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL} .

V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω.

Typical Performance Curves

$T_A = +25\text{ }^{\circ}\text{C}$, Unless Otherwise Specified

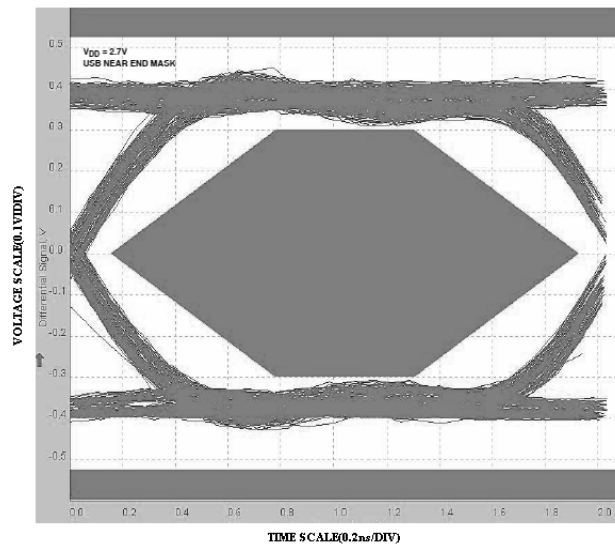


Figure6. Eye Pattern : 480 Mbps with USB Switches in the Signal Path (near end mask)

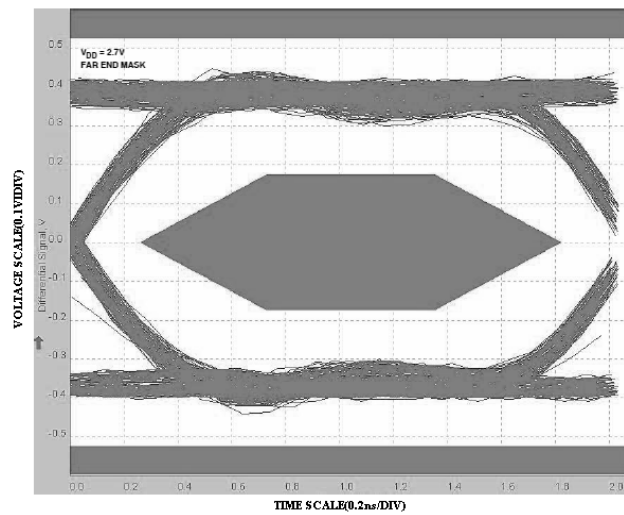
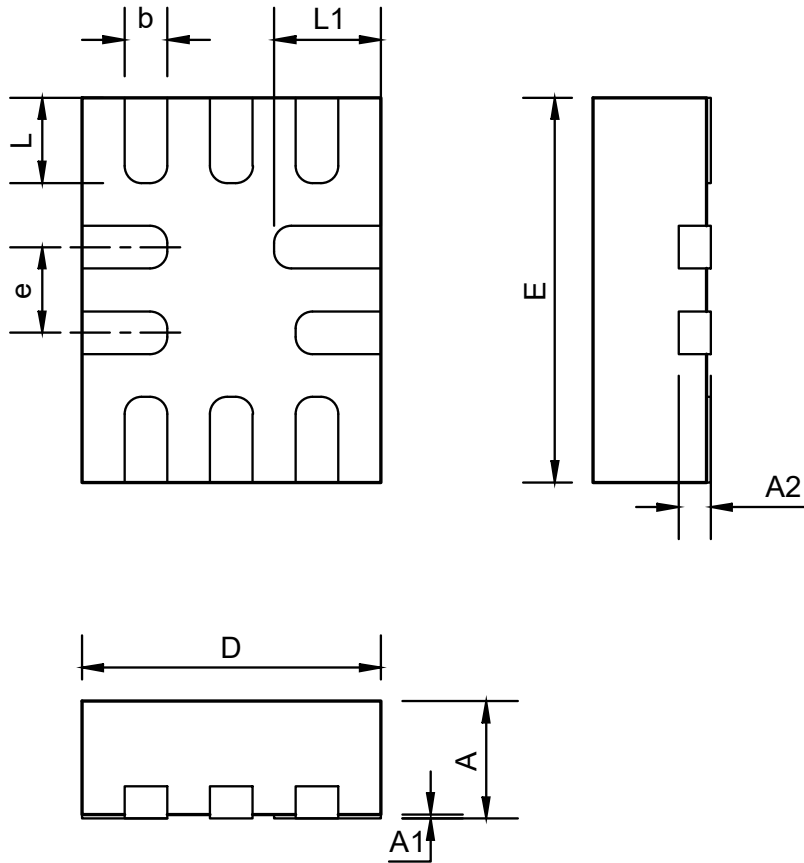


Figure7. Eye Pattern : 480 Mbps with USB Switches in the Signal Path (far end mask)

ET7222

Package Dimension

QFN10L

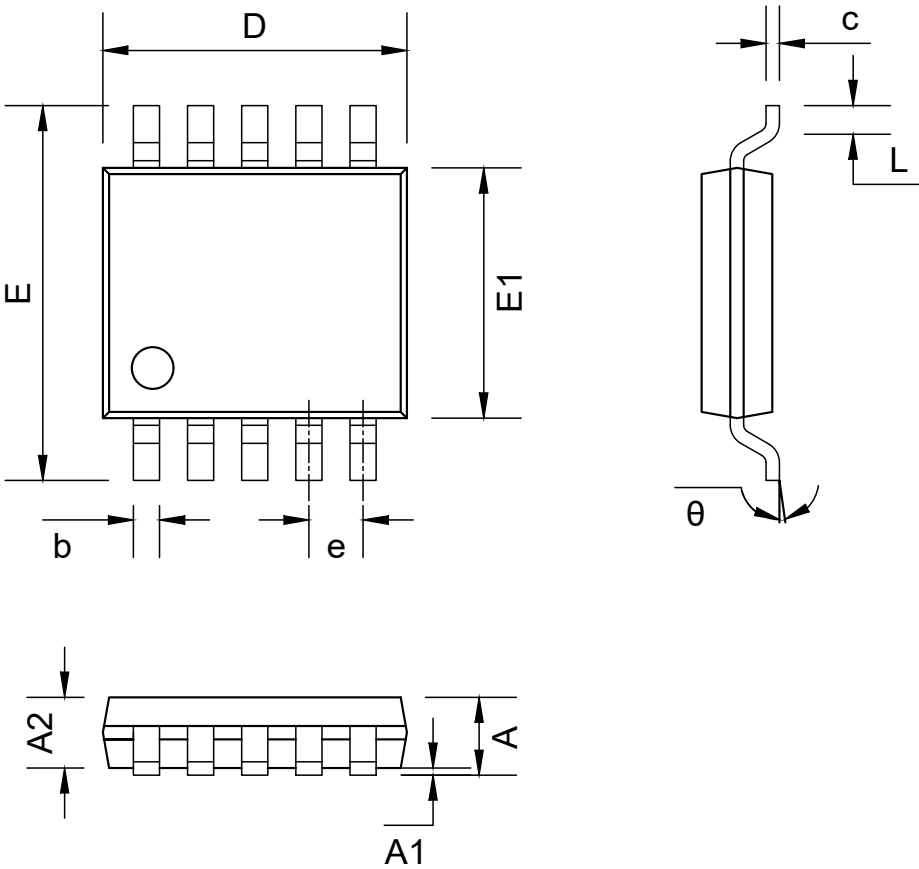


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.500		0.600
A1	0.000		0.050
A2	0.152 TYP		
b	0.150	0.200	0.250
D	1.350	1.400	1.450
E	1.750	1.800	1.850
e	0.400 TYP		
L	0.350	0.400	0.450
L1	0.450	0.500	0.550

ET7222

MSOP10



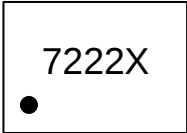
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.82	0.95	1.10
A1	0.02	0.07	0.15
A2	0.75	0.85	0.95
b	0.18	0.23	0.28
c	0.09	0.16	0.23
D	2.90	3.00	3.10
E	4.75	4.90	5.05
E1	2.90	3.00	3.10
e	0.50 TYP		
L	0.40		0.80
θ	0°		6°

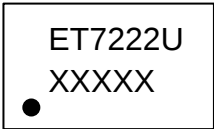
ET7222

Marking Information

ET7222(QFN10L)

7222 - Part Number X - Tracking Number, and is variable	
---	---

ET7222U(MSOP10)

ET7222U - Part Number XXXXX - Tracking Number, and is variable	
--	---

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2012-08-07	Preliminary Version	Liuxm	Liuxm	Zhujl
1.1	2016-02-01	Add some parameters	Liuxm	Liuxm	Zhujl
1.2	2017-03-10	Updated typo	Wuxj	Wuxj	Zhujl
1.3	2019-02-01	Update format	Liuxm	Liuxm	Liujoy
1.4	2019-04-12	According to the test results Update Typical Value of On-Resistance Flatness, On-Resistance Matching , Turn-OFF Time, OFF-Isolation, Non-Adjacent Channel Crosstalk	Liuxm	Liuxm	Liujoy
1.5	2019-06-25	Updated: 1.VIH,VIL Test Spec 2.RON,RFLAT,ΔRON Test Conditions 3. RFLAT Test Spec 4.Add max RON, RFLAT, ΔRON value 5.Add Min tBBM value 6. ICC vs. VIN, OFF-ISOLATION,CROSSTALK graph	Liuxm	Liuxm	Zhujl
1.6	2019-09-29	Update OFF-ISOLATION and CROSSTALK	Liuxm	Liuxm	Zhujl
1.7	2020-03-06	Documents check and formalize	Shib	Shib	Liujoy
1.8	2022-08-31	Update Typeset	Qinpl	Qinpl	Liujoy
1.9	2023-12-14	Update C _{ON} 、C _{OFF} spec according to measured data; Update Vcc range to 4.7V	Wangp	Luh	Liujoy
2.0	2024-03-07	Add Marking Information	Yinp	Luh	Liujoy