DPDT USB Switch With Over Voltage Protection

General Description

The ET74752 is a Hi-Speed USB 2.0(480Mbps) DPDT(Double Pole Double Throw) switch with integrated protection for USB D+ and D-, it can be configured as a dual 1:2 or 2:1 switch.

The ET74752 protection on the D+/D- pins can tolerate up to 24V DC, when D+ or D- voltage is greater than the OVP(Over-Voltage Protection) threshold, the switch will be automatically shutoff to protect downstream devices.

The device operates over 2.3V to 5.5V supply range with independent control bits for each switch pair and an on/off enable pin for shutdown mode.

Features

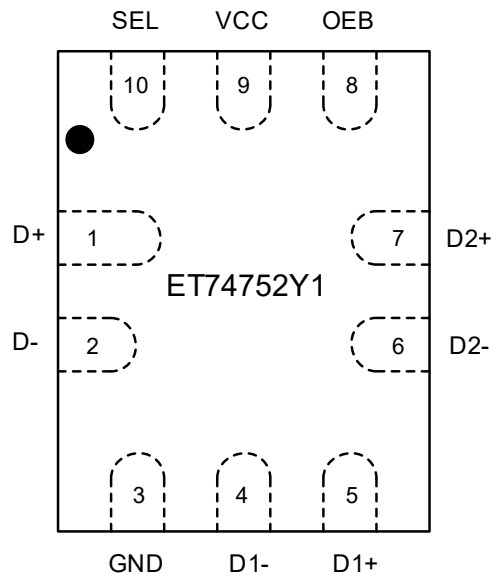
- USB 2.0 Hi-speed DPDT Switch
- Typical -3dB Bandwidth:
  - 1 GHz (Single-ended)
- Over Voltage Protection: 5.1V Typical
- 24V DC Protection on D+ and D- Ports
- +35V Surge Protection on D+ and D-
- Supply Voltage Range: 2.3V to 5.5V
- 7.6Ω Switch On-resistance
- C_{ON}: 6pF Typical
- I_{CC}: 32uA Typical
- Package Information:

Part No.	Package	MSL
ET74752Y1	QFN10L (1.8mm×1.4mm)	Level 1
ET74752Y2	QFN10L (2.0mm×1.5mm)	Level 1

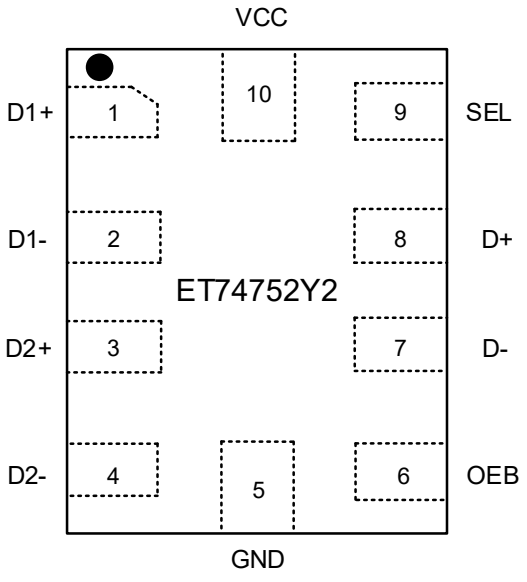
Application

- Smart Phones
- Tables
- USB Type-C
- PC/Notebook

Pin Configuration



Top View



Top View

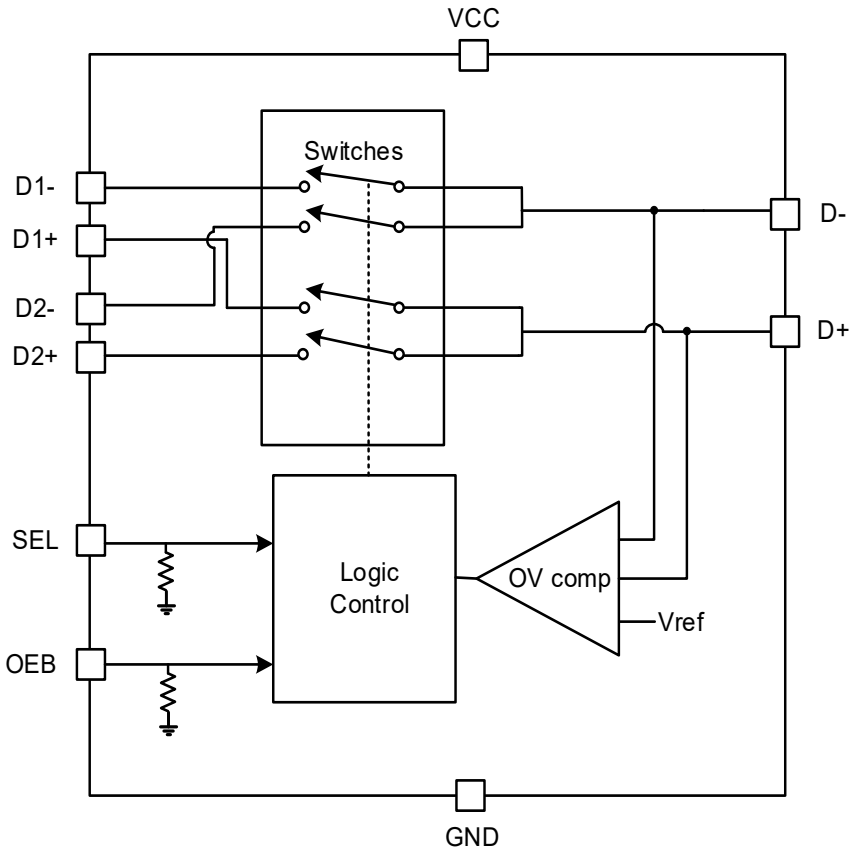
Pin Function

Pin No.	Pin Name	Description
1	D+	Common high speed data port, differential +
2	D-	Common high speed data port, differential -
3	GND	Ground
4	D1-	Multiplexed high speed data port1, differential -
5	D1+	Multiplexed high speed data port1, differential +
6	D2-	Multiplexed high speed data port2, differential -
7	D2+	Multiplexed high speed data port2, differential +
8	OEB	Output enable, active low
9	VCC	Supply voltage
10	SEL	Switch select

Truth Table

OEB	SEL	D- CONNECTION	D+ CONNECTION
H	X	High-Z	High-Z
L	L	D- to D1-	D+ to D1+
L	H	D- to D2-	D+ to D2+

Block Diagram



Block Diagram

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Supply Voltage Range		V_{CC}	-0.3～+6	V
Input/Output DC Voltage (D+, D-)		V_{IS}	-0.5～+24	V
Input/Output DC Voltage (D1+, D1-, D2+, D2-)		V_{IS}	-0.5～+6	V
Input Voltage (SEL, OEB)		V_{IN}	-0.3～+6	V
Storage Temperature Range		T_{STG}	-65 to 150	°C
Maximum Operating Junction Temperature		T_J	150	°C
ESD	Human Body Model (1)	HBM	±2000	V
	Charge-Device Model (1)	CDM	±1500	
Latch up Current Maximum Rating (1)		I_{LATCH}	±200	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

Note1. This device series incorporates ESD protection and is tested by the following methods:

ESD Human Body Model tested per ESDA/JEDEC JS-001-2017.

CDM tested per ESDA/JEDEC JS-002-2018.

Latch up Current Maximum Rating tested per JEDEC78.

Recommended Operating Conditions

Characteristic	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	2.3	5.5	V
Analog Input/Output Voltage (D±)	V_{IS}	0	20	V
Analog Input/Output Voltage (Dn±)		0	3.6	V
Digital Input Voltage (SEL, OEB)	V_{IN}	0	5.5	V
Operating Temperature Range	T_A	-40	+85	°C

Electrical Characteristics

V_{CC}=3.3V, T_A=25°C for typical values (unless otherwise noted).

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		2.3	3.3	5.5	V
I_{CC}	Active Supply Current	OEB=0V, SEL=0V 0V < $V_{D\pm}$ < 3.6V		32	50	uA
I_{CC_PD}	Standby Supply Current	OEB=V_{CC}, SEL=0V		0.1		uA
DC Characteristics						
R_{ON}	On-state Resistance	V_{IS}=0.4V, I_{SINK}=8mA		7.6	10	Ω
ΔR_{ON}	On-state Resistance Match between Channels	V_{IS}=0.4V, I_{SINK}=8mA		0.2	1	Ω
$R_{ON(FLAT)}$	On-state Resistance Flatness	V_{IS}=0V to 0.4V, I_{SINK}=8mA		0.01	1	Ω
I_{OFF}	I/O pin OFF Leakage Current on D+/D-	$V_{D\pm}$=0V or 3.6V $V_{D1\pm}$ or $V_{D2\pm}$=3.6V or 0V		0.4	5	uA
		$V_{D\pm}$=0V or 24V $V_{D1\pm}$ or $V_{D2\pm}$=0V		3.0	10	uA
I_{ON}	ON Leakage Current on D+/D-	$V_{D\pm}$=0V or 3.6V $V_{D1\pm}$ and $V_{D2\pm}$=high-Z		0.4	10	uA
Digital Characteristics						
V_{IH}	Input Logic High	V_{CC}=2.3V to 5.5V SEL, OEB	0.96			V
V_{IL}	Input Logic Low	V_{CC}=2.3V to 5.5V SEL, OEB			0.4	V
R_{OEB}	OEB Pull-down Resistor		6	8	12	MΩ
R_{SEL}	SEL Pull-down Resistor		1	2	3	MΩ
Protection						
V_{OVP_TH}	OVP Threshold	D+/D- rising	4.8	5.1	5.4	V
V_{OVP_HYST}	OVP Threshold Hysteresis			250		mV
V_{CLAMP_V}	Clamping Voltage on $D_{1\pm}$ and $D_{2\pm}$ Pins during Surge	8/20us surge test, OEB=0V, R_L=open			9	V
t_{CLAMP}	Clamp Time during OVP	V_{D+}/V_{D-}=0V to 35V surge, 8/20us surge test, OEB=0V, R_L=open		150		ns

Electrical Characteristics (Continued)

V_{CC}=3.3V, T_A=25°C for typical values (unless otherwise noted).

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Dynamic Characteristics						
C_{ON}	IO Pins ON Capacitance	$V_{D\pm}$=0V or 3.3V, f=240MHz, switch ON		6		pF
O_{ISO}	Differential Off Isolation	R_L=50Ω, C_L=5pF f=100kHz, switch OFF		-85		dB
		R_L=50Ω, C_L=5pF f=240MHz, switch OFF		-28		dB
X_{TALK}	Channel to Channel Crosstalk	R_L=50Ω, C_L=5pF f=100kHz, switch ON		-85		dB
BW	-3dB Bandwidth	R_L=50Ω, switch ON (Single-ended)	0.75	1		GHz
t_{switch}	Switching Time between Channels (SEL to output)	$V_{D\pm}$=0.8V R_L=50Ω C_L=5pF, V_{CC}=2.3V to 5.5V		3	10	us
t_{on}	Device Turn On Time (OEB to output)			32		us
t_{off}	Device Turn Off Time (OEB to output)			30		ns
t_{pd} (2)	Propagation Delay	$V_{D\pm}$=0.4V, R_L=50Ω, C_L=5pF, V_{CC}=2.3V to 5.5V		200		ps

Note2. This parameter is guaranteed by design and characterization.

Timing Diagram

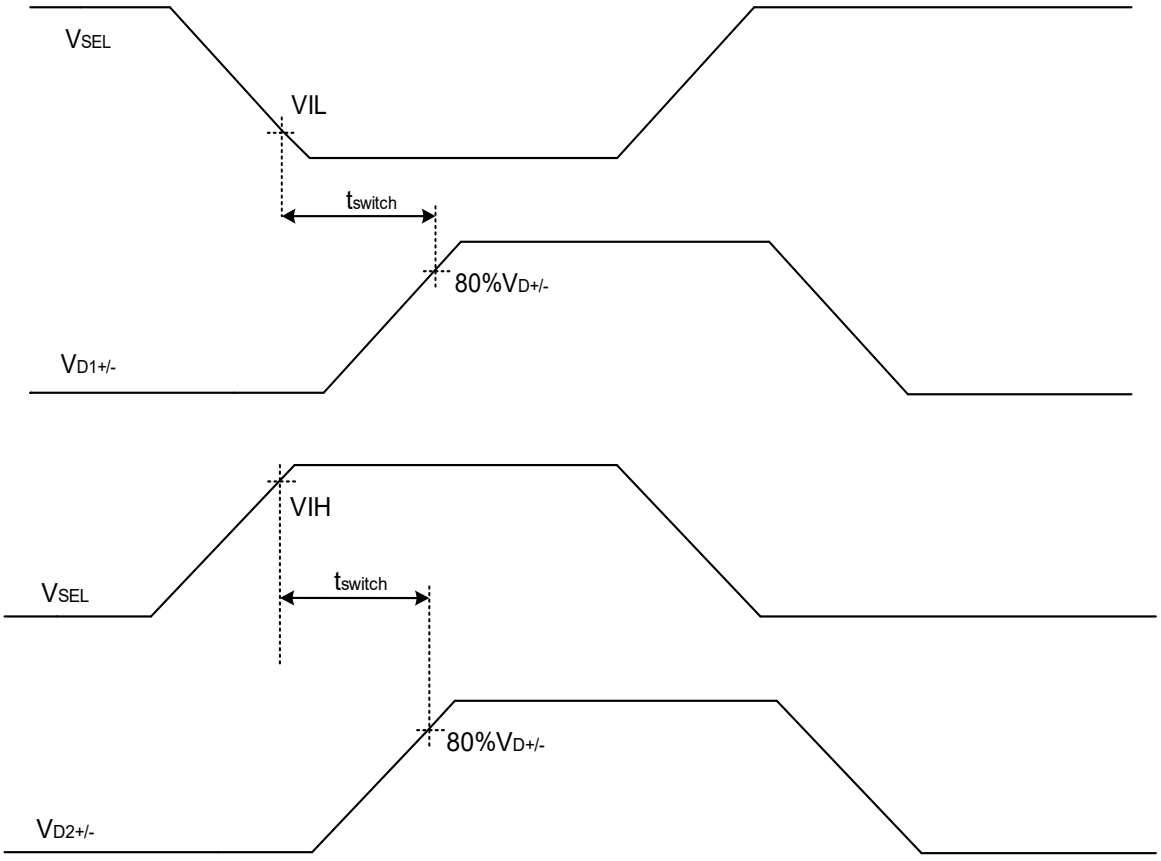


Figure 1. Switching Time Between Channels

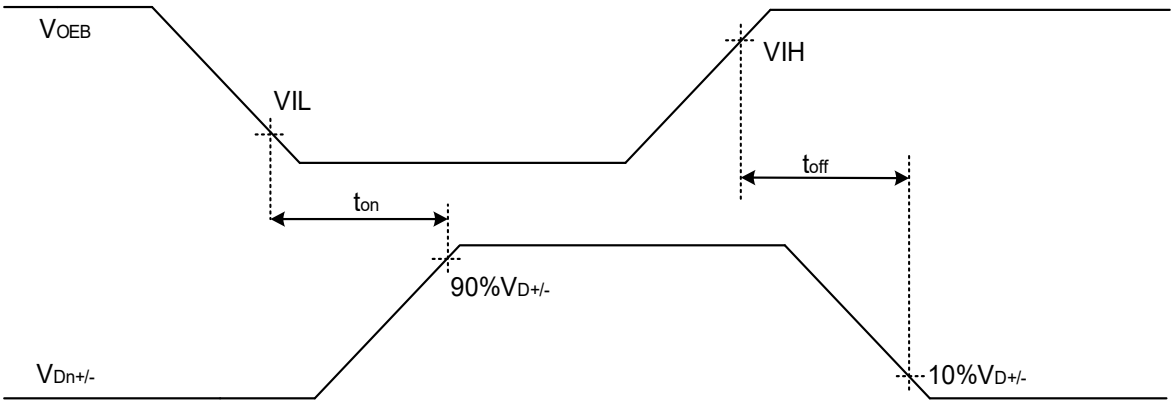


Figure 2. Device Turn On and Off Time

Timing Diagram (Continued)

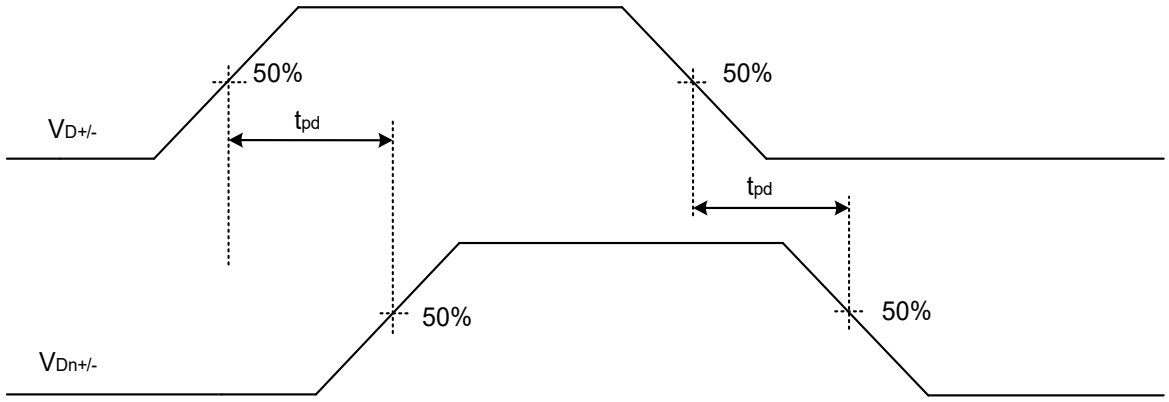


Figure 3. Propagation Delay

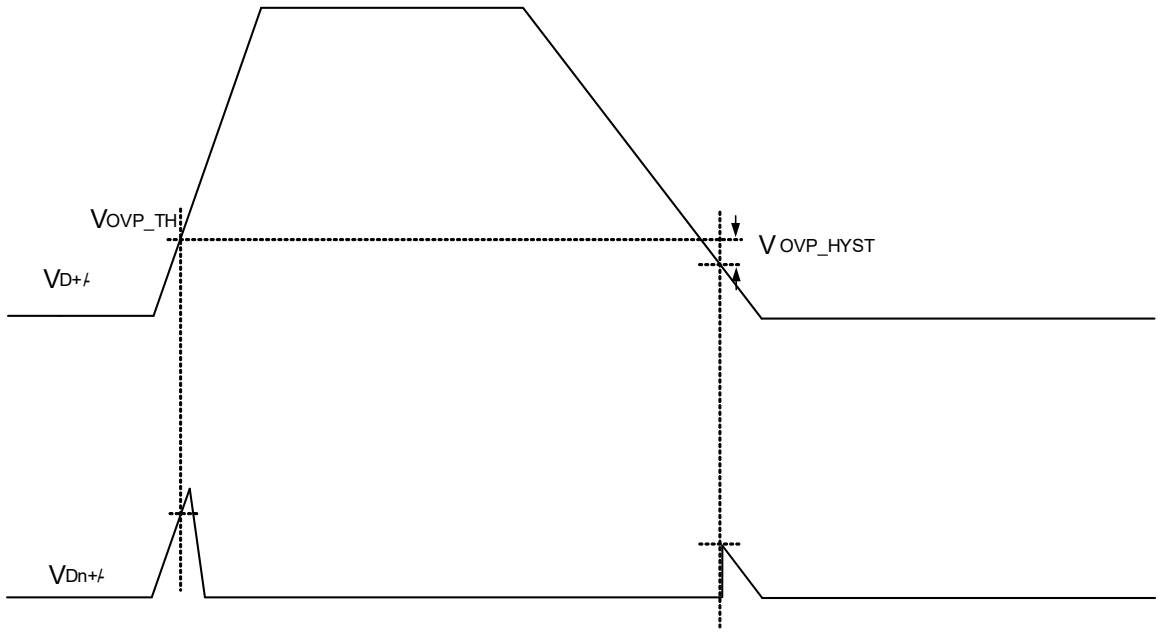


Figure 4. OVP Protection

Test circuits

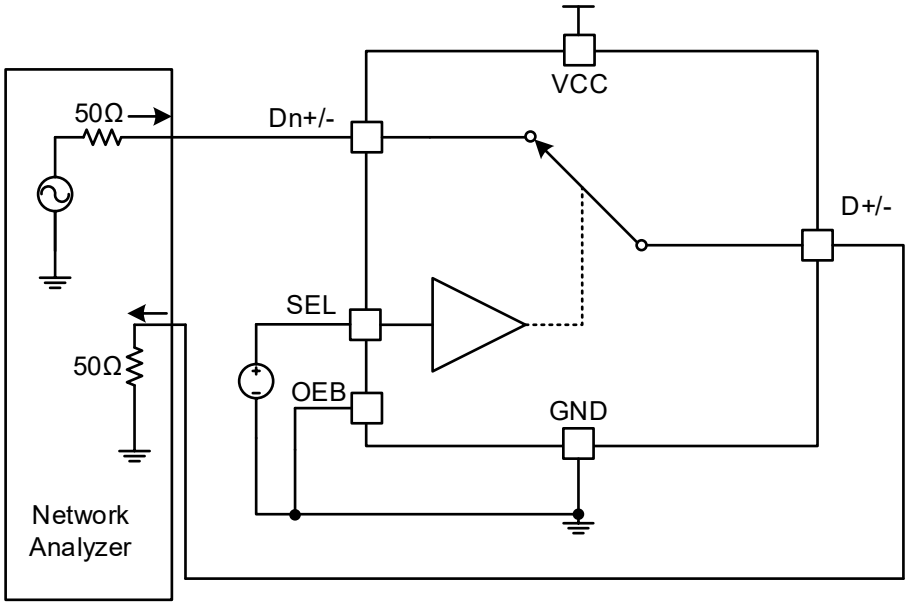


Figure 5. BW and Insertion Loss

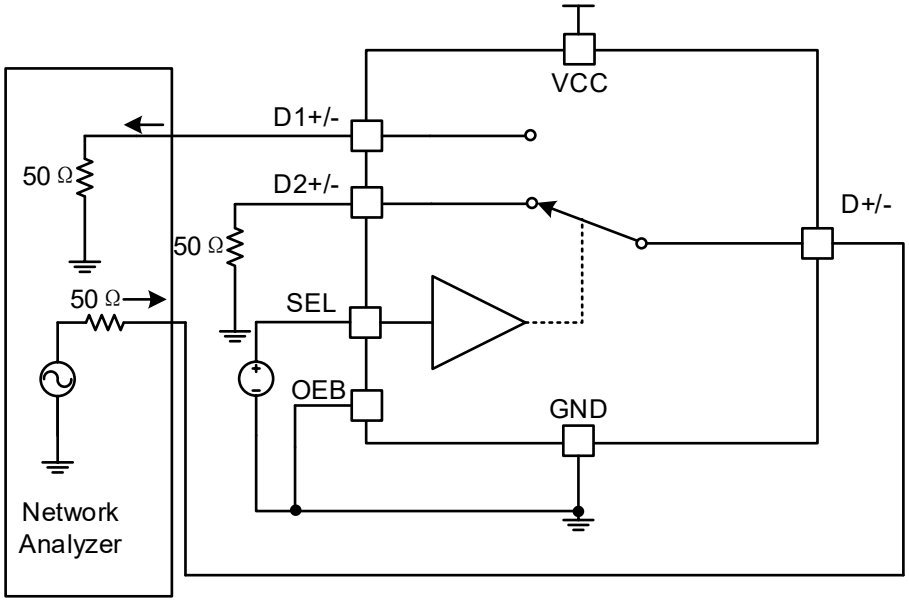


Figure 6. OFF Isolation

Test circuits (Continued)

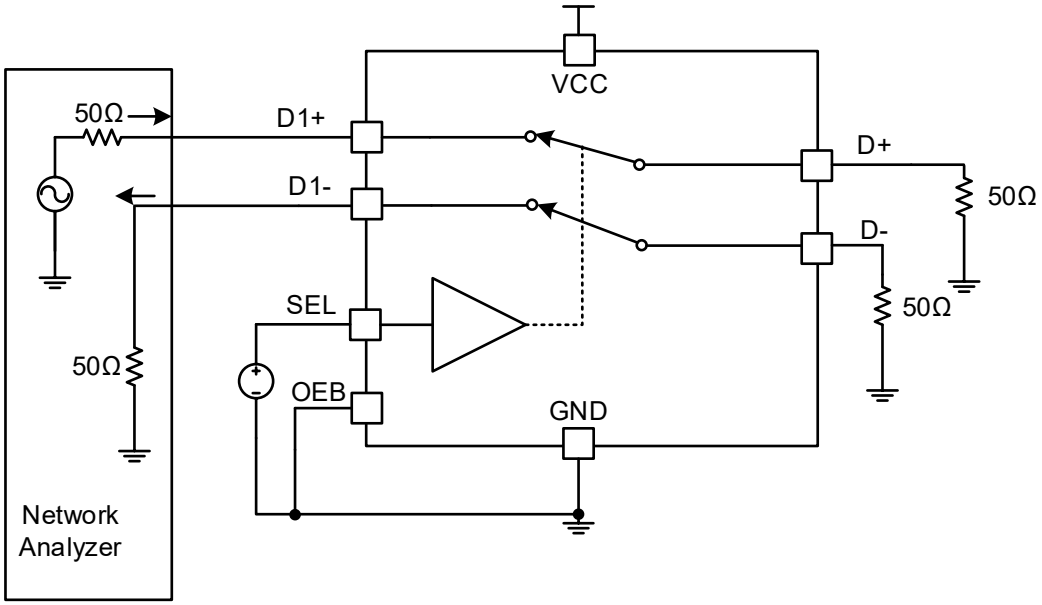


Figure 7. Crosstalk

Typical Characteristics

T_A=25°C, unless otherwise stated

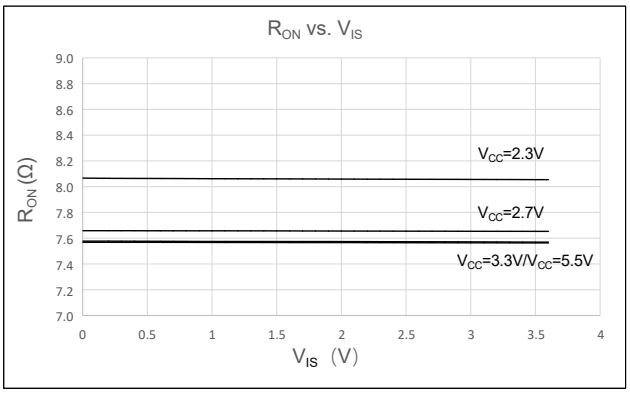


Figure 8. On-Resistance vs. V_{IS}

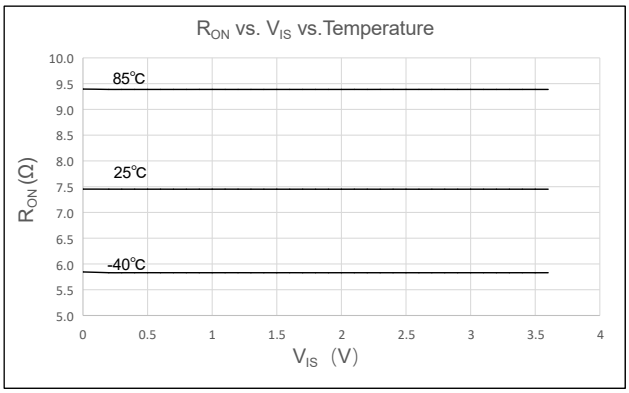


Figure 9. R_{ON} vs. V_{IS} vs. Temperature @V_{CC}=3.3V

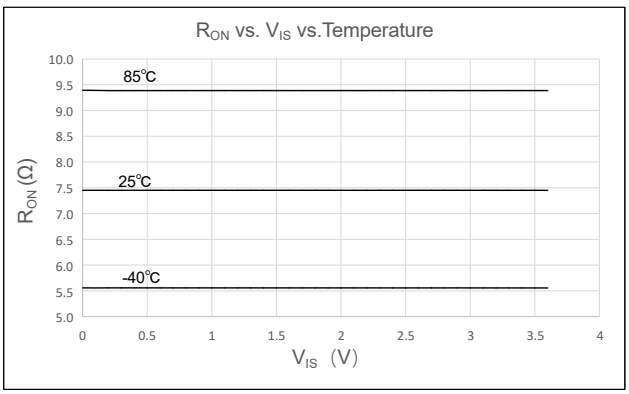


Figure 10. R_{ON} vs. V_{IS} vs. Temperature @V_{CC}=5.5V

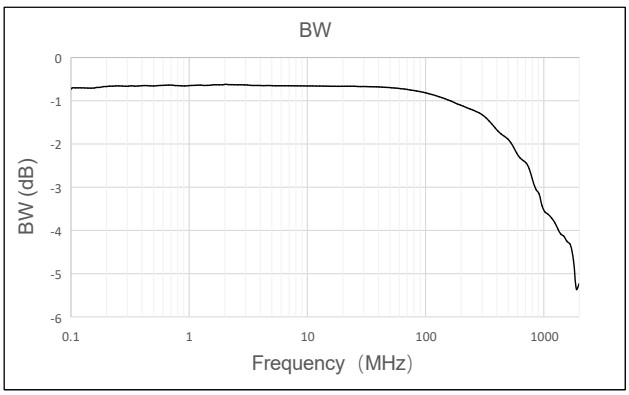


Figure 11. Bandwidth vs. Frequency @V_{CC}=3.3V

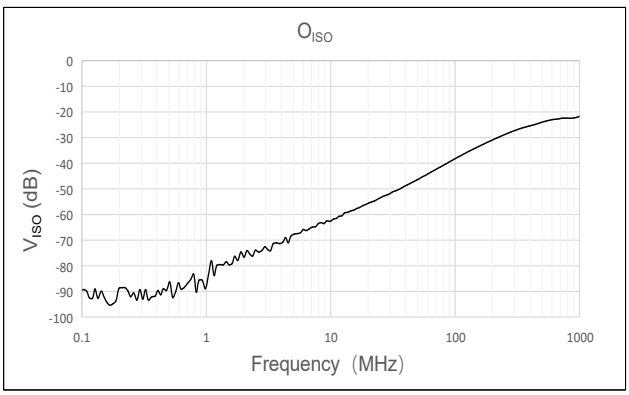


Figure 12. O_{ISO} vs. Frequency @V_{CC}=3.3V

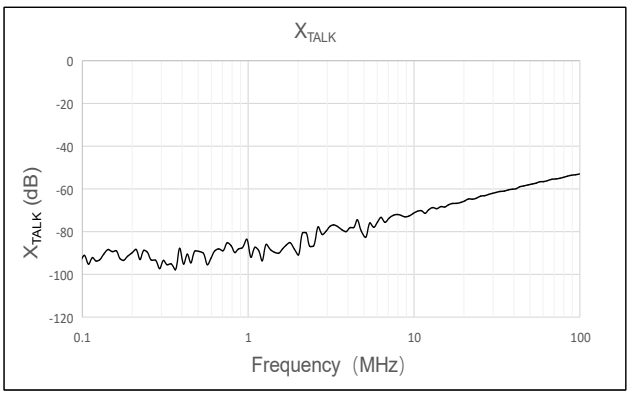


Figure 13. X_{TALK} vs. Frequency @V_{CC}=3.3V

Typical Performance Curves

T_A=25°C, unless otherwise stated

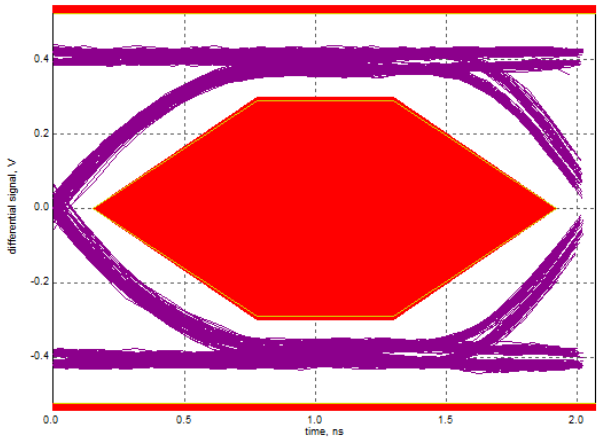


Figure 14. Eye Pattern : 480 Mbps with USB Switch in the Signal Path (near end mask)

Application Circuit

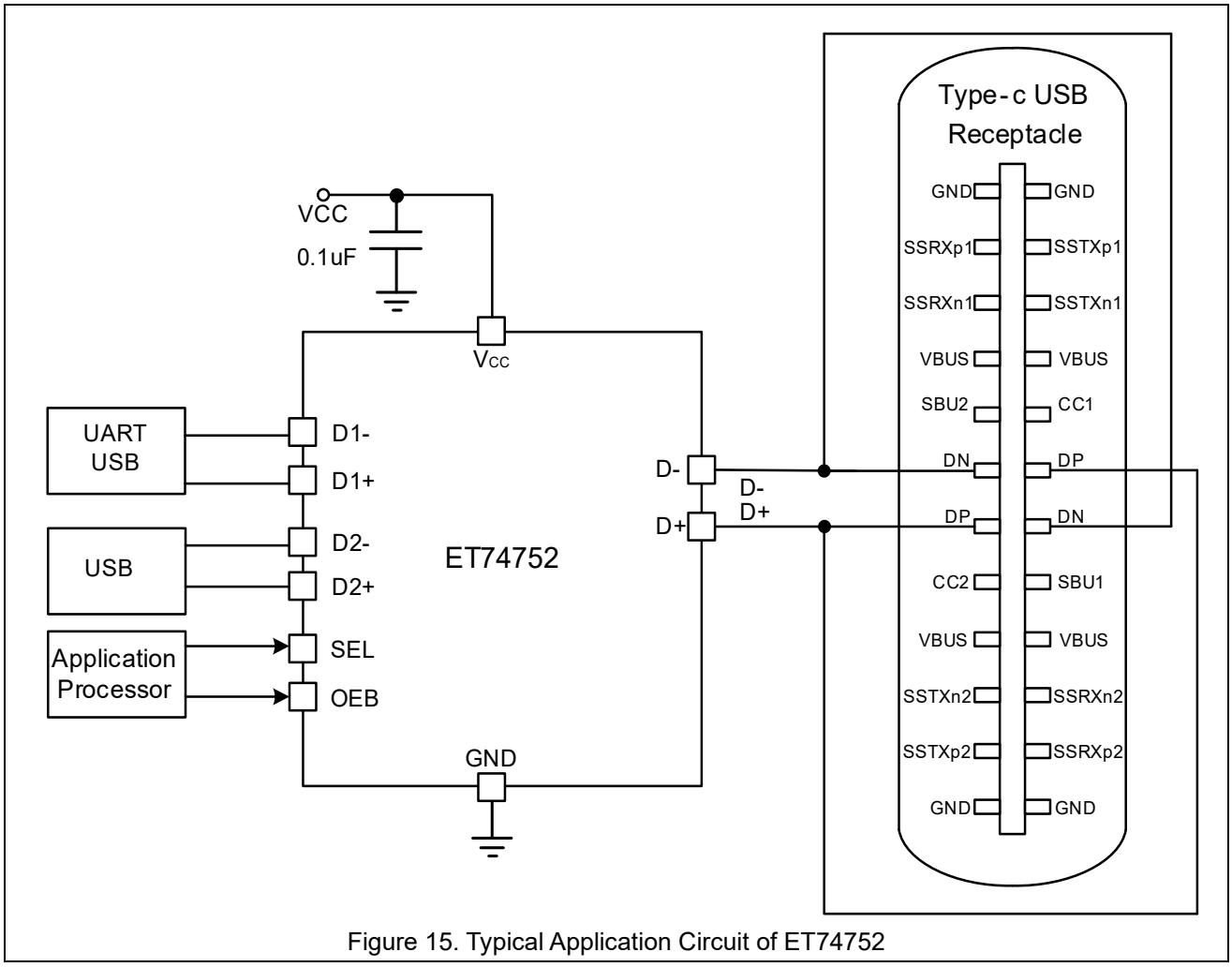
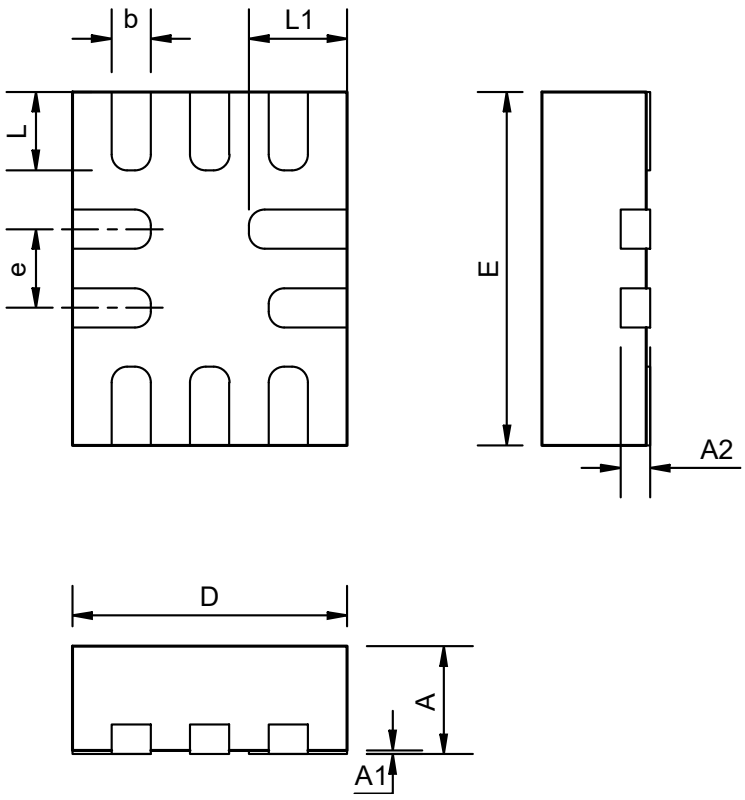


Figure 15. Typical Application Circuit of ET74752

Package Dimension

QFN10L(1.8mm*1.4mm)



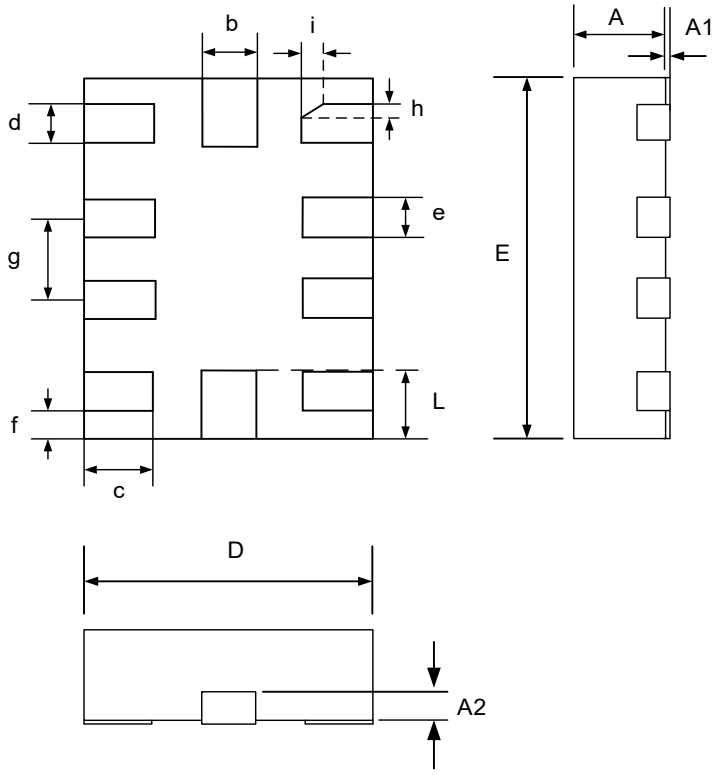
COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
A2		0.15 REF	
b	0.15	0.20	0.25
D	1.35	1.40	1.45
E	1.75	1.80	1.85
e		0.40 BSC	
L	0.30	0.40	0.50
L1	0.40	0.50	0.60

Package Dimension

QFN10L(2.0mm*1.5mm)



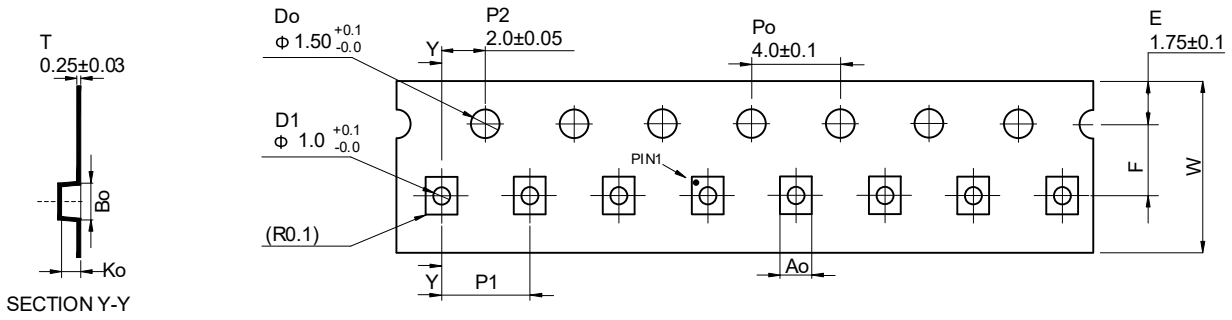
COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	-	0.05
A2		0.152 REF	
b	0.25	0.30	0.35
c	0.30	0.35	0.40
d	0.20	0.25	0.30
e	0.15	0.20	0.25
f		0.125REF	
g	-	0.50	-
h		0.10 REF	
i		0.10 REF	
D	1.45	1.50	1.55
E	1.95	2	2.05
L	0.35	0.40	0.45

Tape Information

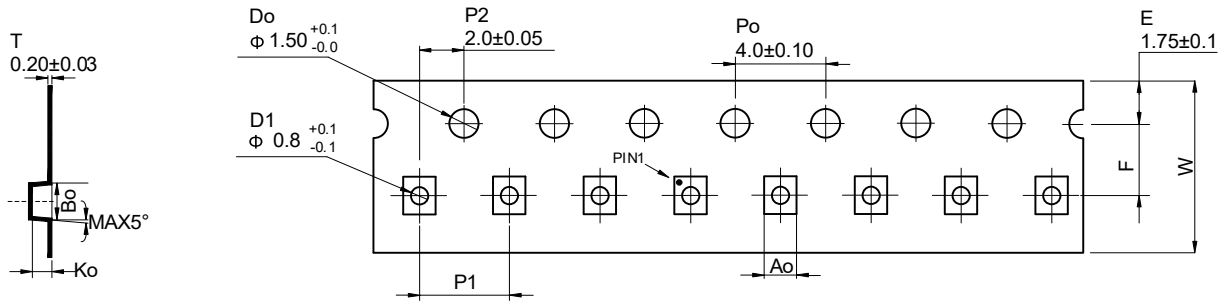
QFN10L(1.8mm*1.4mm)



Ao	1.60	+/-0.05
Bo	2.00	+/-0.05
Ko	0.80	+/-0.05
F	3.50	+/-0.05
P1	4.00	+/-0.1
W	8.00	+0.3/-0.1

Tape Information

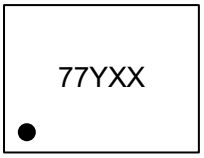
QFN10L(2.0mm*1.5mm)



Ao	1.70	+/-0.05
Bo	2.20	+/-0.05
Ko	0.75	+/-0.05
F	3.50	+/-0.05
P1	4.00	+/-0.10
W	8.00	+0.3/-0.1

Marking Information

QFN10L(1.8mm*1.4mm)



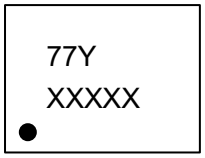
77Y- Part Number

XX - Tracking Number

Note：XX (Tracking Number) is variable, according to the wafer lot number.

Marking Information

QFN10L(2.0mm*1.5mm)



77Y- Part Number

XXXXX - Tracking Number

Note：XXXXX (Tracking Number) is variable, according to the wafer lot number.

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2024-04-02	Preliminary Version	Pansy	Luh	Liujy
0.1	2024-09-30	Initial Version	Pansy	Luh	Liujy
1.0	2025-01-24	Original Version	Wangh	Luh	Liujy
1.1	2025-02-07	Adding Typical Characteristics	Wangh	Luh	Liujy
1.2	2025-06-19	Adding tape and marking information	Wangh	Luh	Liujy
1.3	2025-07-02	Update Characteristics and Application Circuit	Wangh	Luh	Liujy
1.4	2025-07-09	Update Characteristics；Add Eye Pattern	Wangh	Luh	Liujy