Single 1.5A Current Source Camera Flash LED Driver With Adaptive Synchronous Boost

General Description

The ET93010A is an ultra-small LED flash driver that provides a high level of adjust ability with a small solution size.

The ET93010A utilizes a 2MHz or 4MHz fixed-frequency synchronous boost converter to provide power to the 1.5A constant current LED source. The 128 levels current source in Flash/IR modes and 256 levels current source in Torch mode provide the flexibility to adjust the current ratios. An adaptive regulation method ensures the current source remain in regulation and maximizes efficiency. The ET93010A provides IVFM protection mode to prevent system reset or shutdown under low battery condition.

The ET93010A are controlled via an I^2C compatible interface. These features include: flash/torch current, flash timeout duration, IVFM. The ET93010A also provides hardware pin (STROBE/TX) to control Flash/Torch events.

A 2MHz or 4MHz switching frequency options, over-voltage protection (OVP), under-voltage Protection and adjustable current limit allow for the use of tiny, low-profile inductors and ceramic capacitors. The device offers programmable currents in a Flash or Movie Mode (Torch) condition.

The ET93010A is available in WLCSP8 Package and operates over an ambient temperature range of -40°C to +85°C.

Features

- High efficiency 2MHz or 4MHz fixed frequency DC-DC Boost converter with soft start
- Accurate and programmable LED currents
  - -- Flash current range from 11mA to 1.5A
  - -- Torch current range from 1mA to 375mA
- Adaptive regulation method for constant current
- Flash timeout values up to 1.6 seconds
- Optimized flash LED current during low battery conditions
- Grounded cathode LED operation for improved thermal management
- Hardware strobe enable
- Synchronization Input for RF Power Amplifier Pulse Events(TX)
- 400KHz I^2C compatible interface
- Over-voltage and under-voltage protection
- LED/VOUT short circuit protection
- Less than 1uA shutdown current

Device Information

Part No.	Package	Size	MSL
ET93010A	WLCSP8	1.54mm × 0.79mm	Level 1

Application

- Flash/torch/video light for smart phones, feature-phones, tablets, DSCs, DVCs
- IR LED Driver
- Video Surveillance
- IP Camera
- Barcode Scanner
- Portable Data Terminal

Pin Assignments

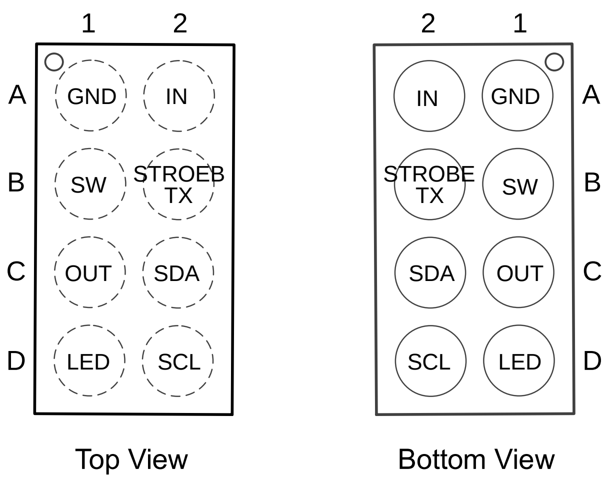


Figure 1. Pin Assignments

Pin Function

Pin No.	Name	I/O	Function
A1	GND	Ground	Ground
A2	IN	Power	Input voltage connection. Connect IN to the input supply and bypass to GND with a 10μF or larger ceramic capacitor.
B1	SW	Power	Drain connection for internal NMOS and synchronous PMOS switches.
B2	STROBE/TX	I	Active high hardware flash enable for drive STROBE high to turn on flash pulse or Configurable dual polarity power amplifier synchronization input. An internal pull-down resistor of 300 kΩ between STROBE/TX and GND
C1	OUT	Power	Step-up DC-DC converter output. Connect a 10μF ceramic capacitor between this pin and GND.
C2	SDA	I/O	I^2C serial data input/output.
D1	LED	Power	High-side current source output for flash LED.
D2	SCL	I	I^2C serial clock input.

Block Diagram

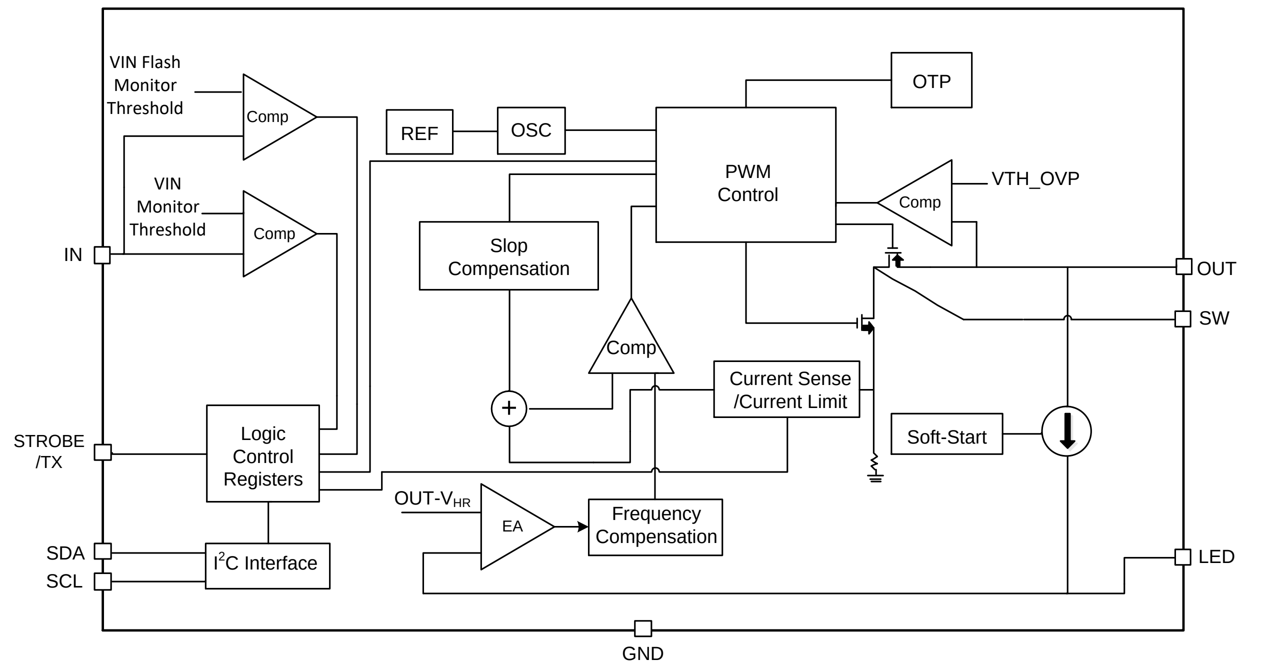


Figure 2. Block Diagram

Functions Description

The ET93010A is a high-power white LED flash driver capable of delivering up to 1.5A. The device incorporates a 2MHz or 4MHz constant frequency-synchronous current-mode PWM boost converter and high-side current source to regulate the LED current over the 2.5V to 5.5V input voltage range.

The ET93010A integrates an adaptive regulation method to ensure the current source remain in programmable current value when the input voltage or load varies. The ET93010A PWM DC-DC boost converter switches and boosts the output to maintain at least VHR across the current source (LED). This minimum headroom voltage ensures that the current source remain in regulation. If the input voltage is above the LED voltage + current source headroom voltage, the device would not switch, but turn the PMOS on continuously (Pass mode). In Pass mode the difference between ($VIN - ILED \times R_{PMOS}$) and the voltage across the LED is dropped across the current source.

The ET93010A has one logic input for a hardware Flash Enable (STROBE pin) or TX interrupt. This logic input has internal 300kΩ (typical) pull-down resistors to GND.

Control is done via an I^2C compatible interface. This includes adjustment of the Flash and Torch current levels, changing the Flash Timeout Duration, TX interrupt, and changing the switch current limit. Additionally, there are flags and status bits that indicate flash current timeout, LED over-temperature condition, LED failure (open and short), device thermal shutdown, thermal current scale-back, VIN under-voltage condition and TX interrupt.

Flash Mode

In Flash Mode, the LED current source provides 128 target current levels from 11mA to 1.5A. The Flash currents are adjusted via the LED Flash Brightness Register. Flash mode is activated by the Enable Register (setting M1, M0 to '11'), or by pulling the STROBE pin HIGH when the pin is enabled (Enable Register). Once the Flash sequence is activated, the LED current source ramps up to the programmed Flash current by stepping through all current steps until the programmed current is reached. The headroom on the current source is regulated to provide 11mA to 1.5A.

When the device is enabled in Flash Mode through the Enable Register, the mode bits in the Enable Register are cleared after a flash timeout event.

Torch Mode

In Torch mode, the LED current source provides 256 target current levels from 1.0mA to 375mA on ET93010A. The Torch currents are adjusted via the LED Torch Brightness Register. Torch mode is activated by the Enable Register (setting M1, M0 to '10'). Once the TORCH sequence is activated, the LED current source ramps up to the programmed Torch current by stepping through all current steps until the programmed current is reached. The rate of the current ramps is determined by the value chosen in the Torch Ramp bit [0] in Timing Register (0x02).

Torch Mode is not affected by Flash Timeout or by a TX Interrupt event.

In torch mode ,ET93010A can be configured to turn off the LED by pull down STROBE pin ,this function can avoid led is staying on until battery depleted when system is crashing. The timing of this function is as follows:

(1) write R50<3>=1;

(2) pull up STROBE pin , then write R01[1:0]=2'b10, the led will be turn on;

(3) pull down STROBE pin when system is crashing , the led will be turn off and R01[1:0] be cleared. See in Figure 3.

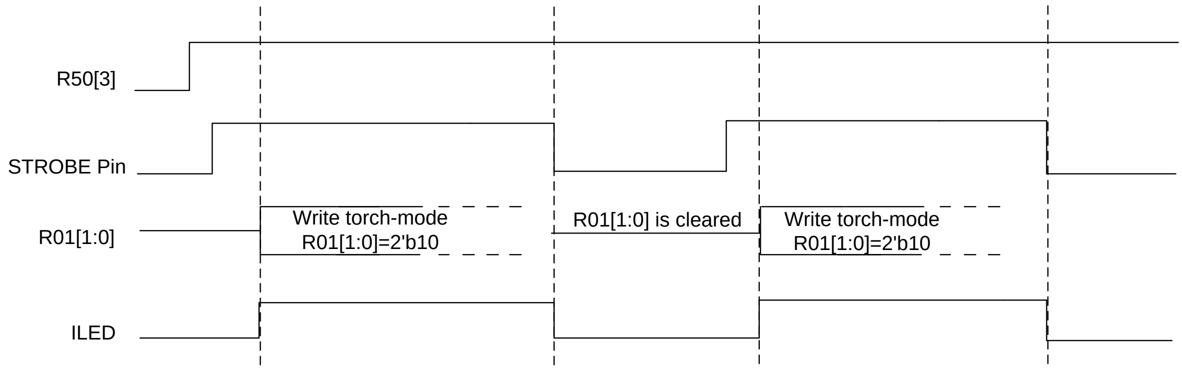


Figure 3. Pull down STROBE pin will turn off led in torch mode

IR Mode

In IR Mode, the target LED current is equal to the value stored in the LED Flash Brightness Register. When IR mode is enabled (setting M1, M0 to '01'), the boost converter turns on and sets the output equal to the input (pass-mode). At this point, toggling the STROBE pin enables and disables the LED current source (if enabled). The strobe pin can only be set to be Level sensitive, meaning all timing of the IR pulse is externally controlled. In IR Mode, the current source do not control the ramp rate of the LED output.

The current transitions immediately from off to on, and then on to off.

If needed, the DC/DC boost will turn on when the LED current is delivered (Strobe Pin = High). When the Strobe Pin goes low, the output voltage will return to VIN (Pass Mode).See in Figure 4.

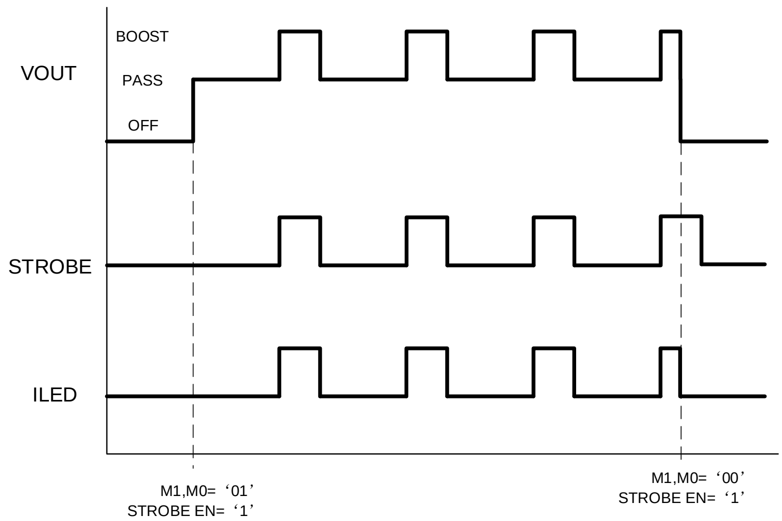


Figure 4. IR Mode with Boost

In pass mode, the boost stays disabled and VOUT = VIN when the Strobe Pin is high or low, See in Figure 5.

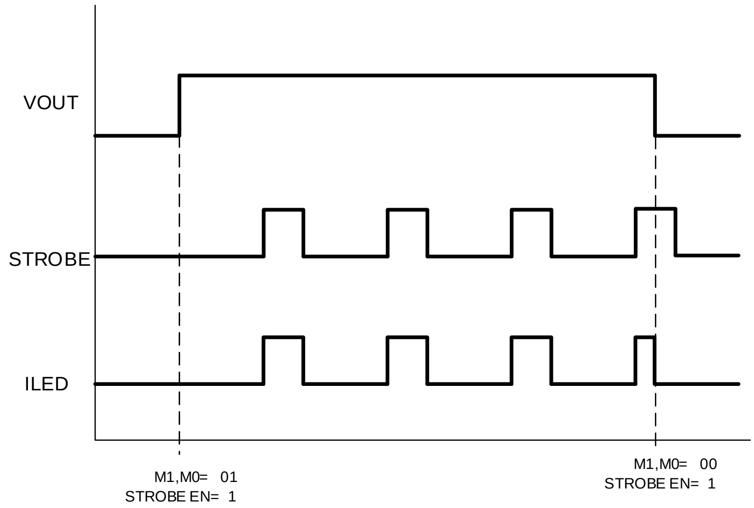


Figure 5. IR Mode Pass Only

When the flash timer elapses, the device goes into stand-by regardless of strobe state, see in Figure 6.

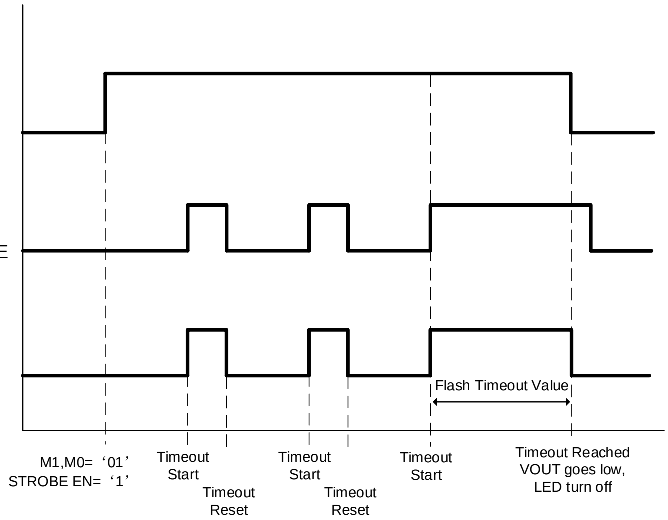


Figure 6. IR Mode Timeout

Soft Start-up

Turn on of the ET93010A Torch and Flash modes can be done through the Enable Register. On start-up, when VOUT is less than VIN the internal synchronous PMOS turns on as a current source and delivers 200mA (typical) to the output capacitor. During this time the current source (LED) is off. When the voltage across the output capacitor reaches 2.2 V (typical) the current source turns on. At turn-on the current source steps through each FLASH or TORCH level until the target LED current is reached. This gives the device a controlled turn-on and limits inrush current from the VIN supply. The target LED flash and the target LED torch currents are set by the LED Flash Brightness Register (0x03 bits [6:0]) and LED Torch Brightness Register

(0x04 bits [6:0]) respectively.

Pass Mode

The ET93010A starts up in Pass Mode and stays there until Boost Mode is needed to maintain regulation. In Pass Mode the boost converter does not switch, and the synchronous PMOS turns fully on bringing VOUT up to VIN − ILED × R_{PMOS}. In Pass Mode the inductor current is not limited by the peak current limit. If the voltage difference between VOUT and VLED falls below VHR, the device switches to Boost Mode.

Power Amplifier Synchronization (TX)

The STROBE/TX pin, when set to TX mode, serves as a Power Amplifier Synchronization input. This is designed to reduce the flash LED current and thus limit the battery current during high battery current conditions such as PA transmit events. The TX mode can be enabled by setting bit [6] of 0x06 Register (TX Enable) to '1'. When the ET93010A is engaged in Internal Flash event (R01 bits [1:0], M1, M0=11), and TX mode is set, then if the TX pin is pulled high, the LED current is forced into Torch Mode at the programmed Torch current setting. If the TX pin is then pulled low before the Flash pulse terminates, the LED current returns to the previous Flash current level. At the end of the Flash time-out, whether the TX pin is high or low, the LED current turns off.

Once TX is enabled, the external Flash and IR mode are not valid. After TX Interrupt event, TX flag (bit [5] of 0x06 Register) is set .Upon an I^2C read of the 0x06 register, the TX flag is cleared.

Input Voltage Flash Monitor (IVFM)

The ET93010A has the ability to adjust the flash current based upon the voltage level present at the IN pin utilizing the Input Voltage Flash Monitor (IVFM). The adjustable threshold ranges from 2.9 V to 3.6 V in 100mV steps .The IVFM threshold is controlled by bits [7:5], in the configuration Register (0x02). The Flag Register has the IVFM flag bit set when the input voltage crosses the IVFM threshold value. Additionally, the IVFM threshold sets the input voltage boundary that forces the ET93010A to stop ramping and hold the flash current during startup.

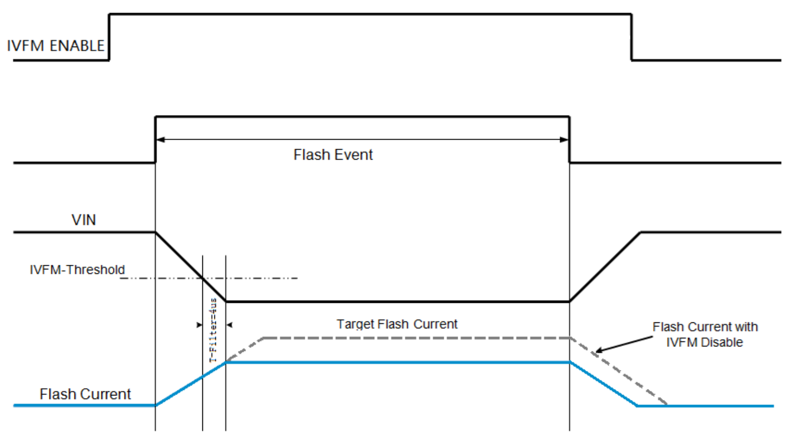


Figure 7. IVFM Modes

Flash Timeout

The Flash Timeout period sets the maximum time of one flash event, whether a flash stop command is received or not. The ET93010A has 16 timeout levels ranging from 40ms to 1.6s (see 0x02 bits [4:1] for more detail).

Current Limit

When the inductor current limit is reached, the ET93010A terminates the charging phase of the switching cycle until the next switching period. If the over-current condition persists, the device operates continuously in current limit. The ET93010A features two selectable inductor current limits (1.9A and 2.8A) that are programmable by bit [5] in Enable Register (0x01).

In pass mode, there is no mechanism to limit the current as the current does not flow through the NMOS, which senses the current limit.

In the boost mode or the pass mode, if VOUT falls below 2.3V, the device stops switching, and the PFET operates as a current source limiting the current to 100mA. This prevents the ET93010A from drawing excessive current from the battery during output short-circuit conditions.

Under Voltage Lock Output (UVLO)

The ET93010A has an internal comparator that monitors the voltage at IN and forces the ET93010A into standby if the input voltage drops to 2.45V. If the UVLO monitor threshold is tripped, the UVLO flag bit is set in the Flags Register. If the input voltage rises above 2.45V, the ET93010A is not available for operation until there is an I^2C read of the Flags Register. Upon an I^2C read of the Flags register, the Flags register is cleared, and normal operation can resume if the input voltage is greater than 2.45V.

VOUT Short Fault

The Output Short Fault flag reads back a '1' if the device is active in Flash or Torch mode and the boost output experiences a short condition. VOUT short condition occurs if the voltage at OUT goes below 2.3V (typ.) while the device is in Torch or Flash mode. There is a deglitch time of 2.048ms before the VOUT Short flag is valid. The mode bits are cleared upon a VOUT short fault. The ET93010A is not available for operation until VOUT Fault flags is cleared. The VOUT Short Faults can be reset to '0' by reading back the Flags Register (0x05), or by setting the RESET bit to a '1', or by removing power to the ET93010A.

LED Short Fault

The LED Short Fault flag read back a '1' if the device is active in Flash or Torch mode and either active LED output experiences a short condition. An LED short condition is determined if the voltage at LED goes below 500mV (typ.) while the device is in Torch or Flash mode. There is a deglitch time of 256us before the LED Short Fault flag is valid. The mode bits are cleared upon an LED short fault. The LED short fault can be reset to 0 by removing power to the ET93010A, or setting the software reset field (Register 0x06 bit [7]) to a 1, or by reading back the Flag Register.

Over Voltage Protection (OVP)

The output voltage is limited to typically 5V. In situations such as an open LED, the ET93010A raises the output voltage in order to try and keep the LED current at its target value. When VOUT reaches 5V (typ.) the Over voltage comparator trips and turns off the internal NMOS. When OVP condition is present for three consecutive OVP events, ET93010A enters stand-by mode and OVP flag (bit [0]) of Flags Register (0x01) is set. Checking for three consecutive events prevents forcing the device to shut down due to momentary OVP condition. When VOUT falls below the VOVP off threshold, the ET93010A switches again.

Thermal Scale-Back (TSB)

When the ET93010A die temperature reaches 125° C, the thermal scale-back (TSB) circuit trips and TSB flag (bit [3]) of Flags Register (0x05) is set. The LED current then shifts to torch current level, set by the LED Torch Brightness Register (0x04 bits [7:0]) for the duration of the flash pulse, set by the flash time-out in the Configuration Register (0x02 bits [4:1]). After I^2C read of the Flags Register and upon re-flash, if the die temperature is still above 125° C, the ET93010A re-enters into torch current level and sets the TSB flag bit again.

Thermal Shutdown (TSD)

When the ET93010A die temperature reaches 150° C, the thermal shutdown detection circuit trips, forcing the ET93010A into standby and writing a '1' to the Thermal Shutdown Fault flag of the Flags Register . The ET93010A restarts only after the Flags Register is read, which clears the fault flag. Upon restart, if the die temperature is still above 150° C, the ET93010A resets the TSD flag and re-enters standby.

Programming

Control Truth Table

MODE1	MODE0	STROBE EN	STROBE PIN	ACTION
0	0	0	X	Standby
0	0	1	Pos edge	Ext Flash
1	0	X	X	Int Torch
1	1	X	X	Int Flash
0	1	0	X	IR LED Standby
0	1	1	0	IR LED Standby
0	1	1	Pos edge	IR LED enabled

I^2C Interface

I^2C Compatible Chip Address

The device address for the ET93010A is 1100100 (0x64). After the START condition, the I^2C compatible master sends the 7-bit address followed by an eighth read or write bit (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data is written. The third byte contains the data for the selected register.

Data Validity

When the SCL signal is HIGH, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

Start (Re-start) and Stop Working Conditions

When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

Acknowledge

ACK means the successful transfer of I^2C bus data. After master sends 8bits data, SDA must be released;

SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

(1). Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

(2). Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

(3). Slave device sends acknowledge signal if the slave address is correct.

(4). Master sends control register address (8-bit)

(5). Slave sends acknowledge signal

(6). Master sends data byte to be written to the addressed register

(7). Slave sends acknowledge signal

(8). If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step 6, 7)

(9). Master generates STOP condition to indicate write cycle end

I²C Writing Command Register Interface Protocol (single)：

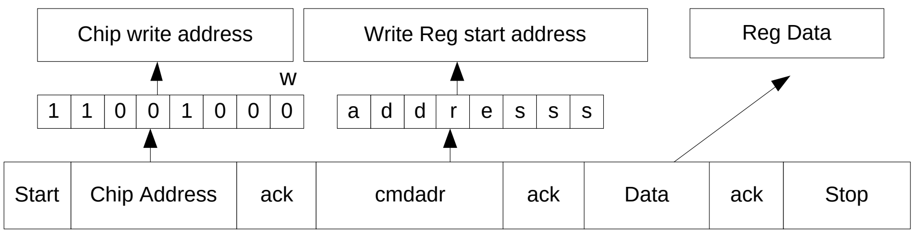


Figure 8. I²C Writing Command Register Protocol (single)

I²C Writing Command Register Interface Protocol (continuous)：

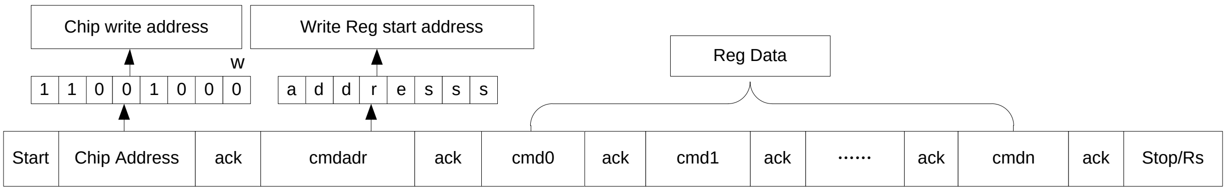


Figure 9. I²C Writing Command Register Protocol (continuous)

Read Cycle

In a read cycle, the following steps should be followed:

(1). Master device generates START condition

(2). Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

(3). Slave device sends acknowledge signal if the slave address is correct.

(4). Master sends control register address (8-bit)

(5). Slave sends acknowledge signal

(6). Master generates STOP condition followed with START condition or REPEAT START condition

(7). Master device sends slave address (7-bit) and the data direction bit (r/w = 1).

(8). Slave device sends acknowledge signal if the slave address is correct.

(9). Slave sends data byte from addressed register.

(10). If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.

(11). If the master device generates STOP condition, the read cycle is ended.

I²C Reading Command Register Interface Protocol(single)

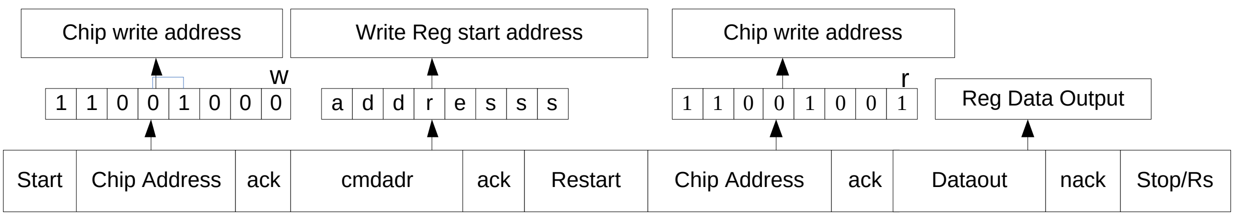


Figure 10. I²C Reading Command Register Interface Protocol(single)

I²C Reading Command Register Interface Protocol(continuous)

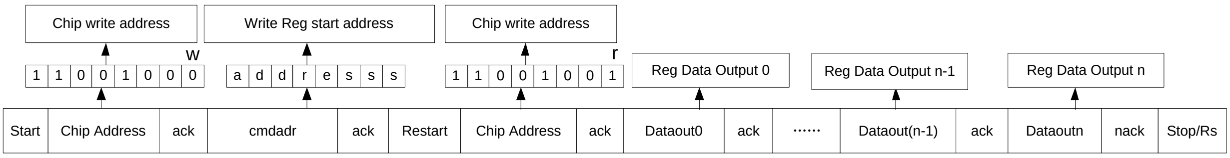


Figure 11. I²C Reading Command Register Interface Protocol(continuous)

Register Descriptions

Addr	Reg Name	Type	Reset -Val	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x01	Enable	R/W	20	BOOST _MODE	BOOST _FREQ	BOOST _ILIMIT	IVFM_EN	STROBE _TYPE	STROBE _EN	MODE[1:0]	
0x02	Config	R/W	15	IVFM_LEVEL [2:0]			FLASH_TIMEOUT[3:0]				TORCH_ RAMP
0x03	LED_F	R/W	80	TSB	LED_FBRIGHT[6:0]						
0x04	LED_T	R/W	00	LED_TBRICHT[7:0]							
0x05	Flags	R/W	00	F_OVP	F_IVFM	F_ SHORT	F_ILIMIT	F_TSB	F_TSD	F_ UVLO	F_ TIMEOUT
0x06	Chip_ID	R/W	29	SOFT _RST	TX_EN	Device ID[2:0]			F_TX	Silicon Revision Bits[1:0]	

Register Detailed Description

Address: 0x01h-- Enable Register

Bit	Name	Description
7	BOOST_MODE	**Boost Mode** 0=Normal (Default) 1=Pass Mode
6	BOOST_FREQ	**Frequency Select** 0 = 2 MHz (Default) 1 = 4 MHz
5	BOOST_ILIMIT	**Boost Current Limit Setting** 0 = 1.9 A 1 = 2.8 A (Default)
4	IVFM_EN	**IVFM Enable** 0 = Disabled (Default) 1 = Enabled
3	STROBE_TYPE	**Strobe Type** 0 = Level Triggered (Default)

		1 = Edge Triggered
2	STROBE_EN	**Strobe Enable** 0 = Disabled (Default) 1 = Enabled
1:0	MODE[1:0]	**Mode Bits: M1, M0** 00 = Standby (Default) 01 = IR Drive 10 = Torch 11 = Flash

Address: 0x02h-- Configuration Register

Bit	Name	Description
7:5	IVFM_LEVEL[2:0]	**IVFM Levels (IVFM-D)** 000 = 2.9 V (Default) 001 = 3.0 V 010 = 3.1 V 011 = 3.2 V 100 = 3.3 V 101 = 3.4 V 110 = 3.5 V 111 = 3.6 V
4:1	FLASH_TIMEOUT[3:0]	**Flash Time-out Duration** 0000 = 40 ms 0001 = 80 ms 0010 = 120 ms 0011 = 160 ms 0100 = 200 ms 0101 = 240 ms 0110 = 280 ms 0111 = 320 ms 1000 = 360 ms 1001 = 400 ms 1010 = 600 ms (Default) 1011 = 800 ms 1100 = 1000 ms 1101 = 1200 ms 1110 = 1400 ms 1111 = 1600 ms
0	TORCH_RAMP	**Torch Ramp** 0 = No Ramp 1 = 1 ms (default)

Address: 0x03h-- LED Flash Brightness Register

Bit	Name	Description
7	TSB	**Thermal Current Scale-Back** 0 = Disabled 1 = Enabled (default) If enabled, the LED current shifts to torch current level if TJ reaches 125 °C
6:0	LED_FBRIGHT[6:0]	**LED Flash Brightness Level** 0000000 = 11 mA (Default) .... 0010101 (0x15) = 0.257 A .... 0111111 (0x3F) = 0.75 A .... 1011111 (0x5F) = 1.09 A .... 1100110 (0x66) = 1.2 A .... 1111111 (0x7F) = 1.5 A

Address: 0x04h--LED Torch Brightness Register

Bit	Name	Description
7:0	LED_TBRICHT[7:0]	**LED Torch Brightness Levels** 00000000 = 1.0 mA (Default) .... 00010101 (0x15) = 32 mA .... 00111111 (0x3F) = 93.5 mA .... 01011111 (0x5F) = 140.5 mA .... 01100110 (0x66) = 151 mA .... 01111111 (0x7F) = 187.5 mA .... 11111111 (0xFF) = 375 mA

Address: 0x05h--Flags Register

Bit	Name	Description
7	F_OVP	OVP Fault
6	F_IVFM	IVFM Trip Flag
5	F_SHORT	V_{OUT} / V_{LED} Short Fault
4	F_ILIMIT	Current Limit Flag
3	F_TSB	Thermal Current Scale-back (TSB) Flag
2	F_TSD	Thermal Shutdown (TSD) Fault
1	F_UVLO	UVLO Fault
0	F_TIMEOUT	Flash Time-Out Flag

Address: 0x06h--Device ID and RESET Register (0x06)

Bit	Name	Description
7	SOFT_RST	**Software RESET** 0 = Normal (default) 1 = Force device RESET
6	TX_EN	**TX Enable** 0 = Disabled (Default) 1 = Enabled
5:3	Device ID	101 (Default)
2	F_TX	**TX Flag**
1:0	Silicon Revision Bits	01 (Default)

Absolute Maximum Ratings

Symbol	Parameter (Items)	Rating	Unit
V_{OS}	IN, SW, OUT, LED ports	-0.3 to 6	V
V_{SW_PEAK}	SW (10ns transient)	8.0	V
V_{IO}	SDA, SCL, STROBE/TX ports	-0.3 to V_{IN}+0.3	V
I_{MAX}	Continuous Power Dissipation	Internally limited	mA
T_J	Junction Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-65 to 150	°C
T_L	Lead Temperature (Soldering, 10 sec)	300	°C
V_{ESD}	Human Body Model (JESD22-A114)	±2000	V
	Charged Device Model (JESD22-C101)	±1000	V
I_{LU}	Max Latch Up Current (EIA/JESD78E)	±200	mA

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	2.5	5.5	V
T_J	Operating Junction Temperature	-40	125	°C
T_A	Ambient Temperature	-40	85	

Electrical Characteristics

(Unless otherwise noted, V_{DD}=3.6V ,T_A=25°C)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
IC SUPPLY							
V_{IN}	Input Voltage Range			2.5		5.5	V
V_{UVLO}	Under-Voltage Lockout	Rising edge		2.35	2.45	2.55	V
V_{UVLO_HYS}		Hysteresis			0.1		V
I_Q	Supply Current	Not switching			300	450	uA
I_{SB}	Standby Supply Current	Device disable 2.5 V ≤ V_{IN} ≤ 5.5 V			0.8	4	uA
STEP-UP CONVERTER							
R_{PMOS}	PMOS switch on-resistance				200		mΩ
R_{NMOS}	NMOS switch on-resistance				130		
I_{LIM}	Peak NMOS Current Limit	Reg 0x01, bit [5] = 0		1.65	1.9	2.25	A
		Reg 0x01, bit [5] = 1		2.4	2.8	3.2	A
f_S	Oscillator Frequency	2.5 V ≤ V_{IN} ≤ 5.5 V; Reg 0x01, bit [6] = 0		-10%	2.0	10%	MHz
		2.5 V ≤ V_{IN} ≤ 5.5 V; Reg 0x01, bit [6] = 1		-10%	4.0	10%	MHz
V_{OVP}	Over-Voltage Threshold of OUT			4.86	5.0	5.1	V
V_{OVP_HYS}	Output Over Voltage Hysteresis				300		mV
V_{IVFM}	Input Voltage Flash Monitor Trip Threshold	Reg 0x02, bits [7:5] = '000'		-3%	2.9	3%	V
CURRENT SOURCE SPECIFICATIONS							
I_{LED}	Current Source Accuracy	V_{LED} = 3.4 V, flash code = 0x7F = 1.5 A		-10%	1.5	10%	A
		V_{LED} = 3.4 V, torch code = 0xFF =375mA		-10%	375	10%	mA
V_{HR}	LED Current Source Regulation Voltage	I_{LED} = 1.5 A	Flash		500		mV
		I_{LED} = 375mA	Torch		300		mV
V_{SHORT}	LED Short Checking Voltage				500		mV
STROBE/TX VOLTAGE SPECIFICATIONS							
V_{IL}	Input Logic Low	2.5 V ≤ V_{IN} ≤ 5.5 V				0.4	V
V_{IH}	Input Logic High	2.5 V ≤ V_{IN} ≤ 5.5 V		0.9			V
I²C-COMPATIBLE INTERFACE SPECIFICATIONS (SCL, SDA)							
V_{IL}	Input Logic Low	2.5 V ≤ V_{IN} ≤ 5.5 V				0.4	V
V_{IH}	Input Logic High	2.5 V ≤ V_{IN} ≤ 5.5 V		0.9			V
V_{OL}	Output Logic Low	I_{LOAD} = 3 mA				400	mV

I²C Timing Specifications

Symbol	Parameter	Min	Max	Unit
f_{SCL}	I²C SCL Clock Frequency	0	400	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.6		us
t_{LOW}	Low Period of I²C SCL Clock	1.3		us
t_{HIGH}	High Period of I²C SCL Clock	0.6		us
$t_{SU;STA}$	Set-up Time for Repeated START Condition	0.6		us
$t_{HD;DAT}$	Data Hold Time	0		us
$t_{SU;DAT}$	Data Set-up Time	100		ns
t_r	Rise Time of I²C_SDA and I²C_SCL Signals		300	ns
t_f	Fall Time of I²C_SDA and I²C_SCL Signals		300	ns
$t_{SU;STQ}$	Set-up Time for STOP Condition	0.6		us
t_{BUF}	Bus-Free Time between STOP and START Conditions	1.3		us
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns
C_b	Capacitive Load for each Bus Line		550	pF

I²C Timing Waveform

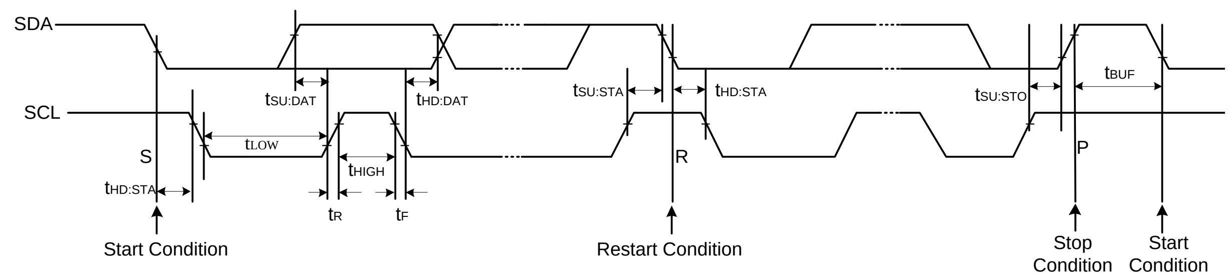


Figure 12. Definition of Timing for I²C Bus

Application circuit

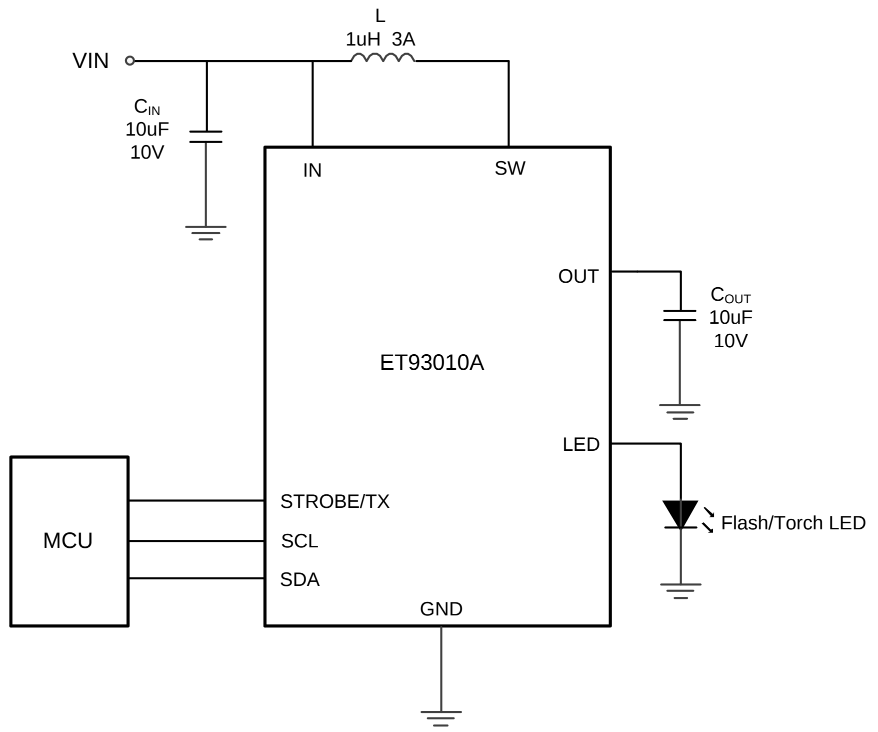


Figure 13. Typical Application(*)

Notes*:

1. Please place CIN，COUT as close to the chip as possible.

2. Connect the inductor on the top layer close to the SW pin.

3. For the sake of driving capability, the power lines, output lines, and the connection lines of L and LED should be short and wide as possible.

Application Information

The ET93010A can drive a flash LEDs at currents up to 1.5A. The 2MHz/4MHz DC-DC boost regulator allows for the use of small value discrete external components. Below are some peripheral selection guidelines.

Output Capacitor Selection

The ET93010A is designed to operate with a 10µF ceramic output capacitor. When the boost converter is running, the output capacitor supplies the load current during the boost converter on-time. When the NMOS switch turns off, the inductor energy is discharged through the internal PMOS switch, supplying power to the load and restoring charge to the output capacitor. This causes a sag in the output voltage during the on-time and a rise in the output voltage during the off-time. The output capacitor is therefore chosen to limit the output ripple to an acceptable level depending on load current and input/output voltage differentials and also to ensure the converter remains stable.

Larger capacitors such as a 22µF or capacitors in parallel can be used if lower output voltage ripple is desired.

To estimate the output voltage ripple considering the ripple due to capacitor discharge (ΔV_Q) and the ripple due to the capacitors ESR (ΔV_{ESR}) use the following equations:

For continuous conduction mode, the output voltage ripple due to the capacitor discharge is:

$$\Delta V_Q = \frac{(V_{OUT} - V_{IN}) \times I_{LED}}{V_{OUT} \times f \times C_{OUT}}$$

The output voltage ripple due to the output capacitors ESR is found by:

$$\Delta V_{ESR} = R_{ESR} \times \left(\frac{V_{OUT} \times I_{LED}}{V_{IN}} + \frac{\Delta I_L}{2} \right) \qquad \Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f \times L}$$

In ceramic capacitors the ESR is very low so the assumption is that 80% of the output voltage ripple is due to capacitor discharge and 20% from ESR. Table 1 lists different manufacturers for various output capacitors and their case sizes suitable for use with the ET93010A.

Input Capacitor Selection

Choosing the correct size and type of input capacitor helps minimize the voltage ripple caused by the switching of the ET93010A boost converter and reduce noise on the boost converter's input pin that can feed through and disrupt internal analog signals. In the typical application circuit a 10-µF ceramic input capacitor works well. It is important to place the input capacitor as close as possible to the ET93010A input (IN) pin. This reduces the series resistance and inductance that can inject noise into the device due to the input switching currents. Table 1 lists various input capacitors recommended for use with the ET93010A.

Table 1 Recommended Input/ Output Capacitors (X5R/X7R Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE	VOLTAGE RATING
TDK	C1608JB0J106M	10uF	0603	6.3V
TDK	C2012JB1A106M	10uF	0805	10V
Murata	GRM188R60J106M	10uF	0603	6.3V
Murata	GRM21BR61A106KE19	10uF	0805	10V

Inductor Selection

The ET93010A is designed to use a 0.47µH or 1µH inductor. When the device is boosting (VOUT > VIN) the inductor is typically the largest area of efficiency loss in the circuit. Therefore, choosing an inductor with the lowest possible series resistance is important. Additionally, the saturation rating of the inductor should be greater than the maximum operating peak current of the ET93010A. This prevents excess efficiency loss that can occur with inductors that operate in saturation. For proper inductor operation and circuit performance, ensure that the inductor saturation and the peak current limit setting of the ET93010A are greater than IPEAK in the following calculation:

$$I_{PEAK} = \frac{I_{LED} \times V_{OUT}}{\eta \times V_{IN}} + \Delta I_L \qquad \Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

f_{SW} =2 or 4MHz.

Table 2 lists various inductors and their manufacturers that work well with the ET93010A.

Table 2 Recommended Inductors

MANUFACTURER	L	PART NO.	SIZE	ISAT	RDC
TOKO	1μH	DFE201610P-1R0M	2.0 mm x 1.6 mm x 1.0 mm	3.7A	58mΩ
Sunlord	1μH	WPN252012H1R0MT	2.5mm × 2.0mm ×1.2mm	3.4A	48mΩ

PCB Layout Guidelines

The high switching frequency and large switching currents of the ET93010A make the choice of layout important. The following steps should be used as a reference to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range.

(1). Place C_{IN} on the top layer (same layer as the ET93010A) and as close to the device as possible. The input capacitor conducts the driver currents during the low-side MOSFET turn-on and turn-off and can detect current spikes over 1A in amplitude. Connecting the input capacitor through short, wide traces to both the IN and GND pins reduces the inductive voltage spikes that occur during switching which can corrupt the VIN line.

(2). Place C_{OUT} on the top layer (same layer as the ET93010A) and as close as possible to the OUT and GND pin. The returns for both C_{IN} and C_{OUT} should come together at one point, as close to the GND pin as possible. Connecting C_{OUT} through short, wide traces reduce the series inductance on the OUT and GND pins that can corrupt the VOUT and GND lines and cause excessive noise in the device and surrounding circuitry.

(3). Connect the inductor on the top layer close to the SW pin. There should be a low-impedance connection from the inductor to SW due to the large DC inductor current, and at the same time the area occupied by the SW node should be small so as to reduce the capacitive coupling of the high dV/dT present at SW that can couple into nearby traces.

(4). Avoid routing logic traces near the SW node so as to avoid any capacitive coupling from SW onto any high-impedance logic lines such as STROBE/TX, SDA, and SCL. A good approach is to insert an inner layer GND plane underneath the SW node and between any nearby routed traces. This creates a shield from the electric field generated at SW.

(5). Terminate the Flash LED cathodes directly to the GND pin of the ET93010A. If possible, route the LED returns with a dedicated path so as to keep the high amplitude LED currents out of the GND plane. For Flash LEDs that are routed relatively far away from the ET93010A, a good approach is to sandwich the forward and return current paths over the top of each other on two layers. This helps reduce the inductance of the LED current paths.

Typical characteristics

T_A = 25°C, V_{IN} = 3.6 V, C_{IN} = 10 μF, C_{OUT} = 10 μF, L = 1 μH, V_{LED} = 3.4 V, Flash Time_out=320ms, Thermal Scale-Back (TSB) disabled, unless otherwise noted.

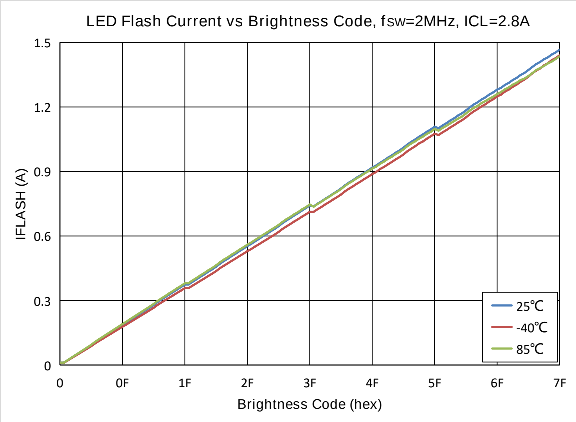


Figure 1. LED Flash Current vs Brightness Code

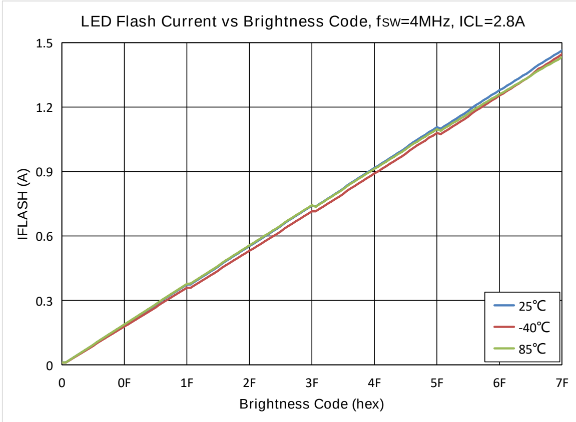


Figure 2. LED Flash Current vs Brightness Code

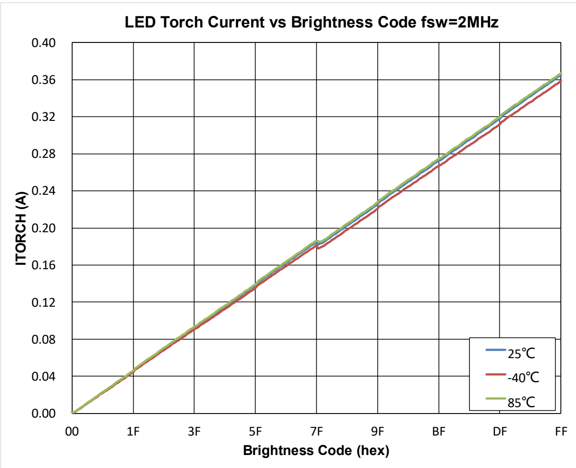


Figure 3. LED Torch Current vs Brightness Code

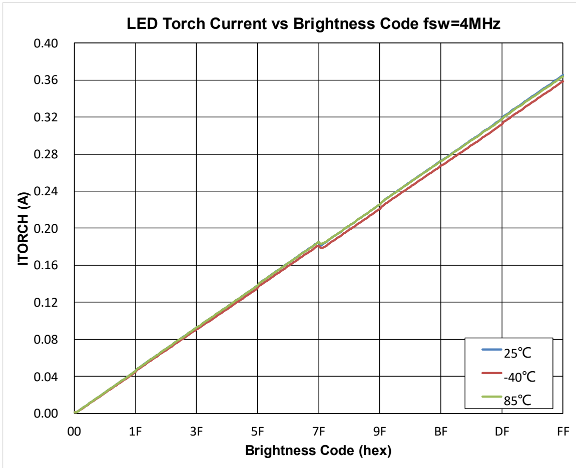


Figure 4. LED Torch Current vs Brightness Code

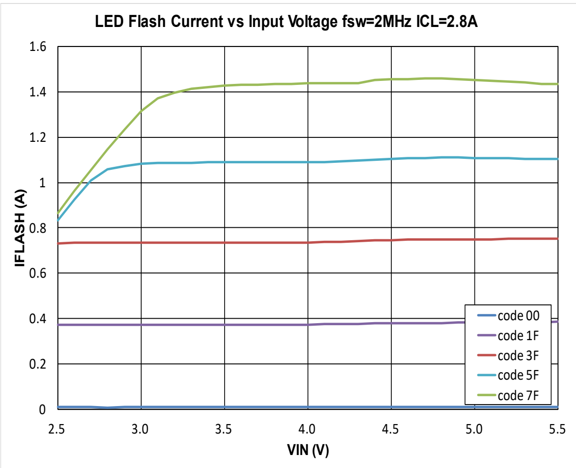


Figure 3. LED Flash Current vs Input Voltage

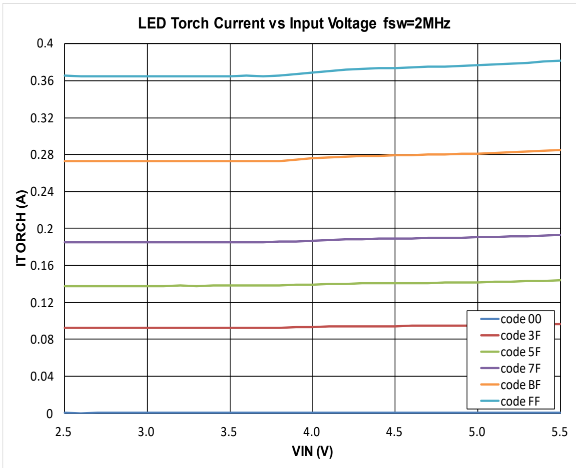


Figure 6. LED Torch Current vs Input Voltage

Typical characteristics (Continued)

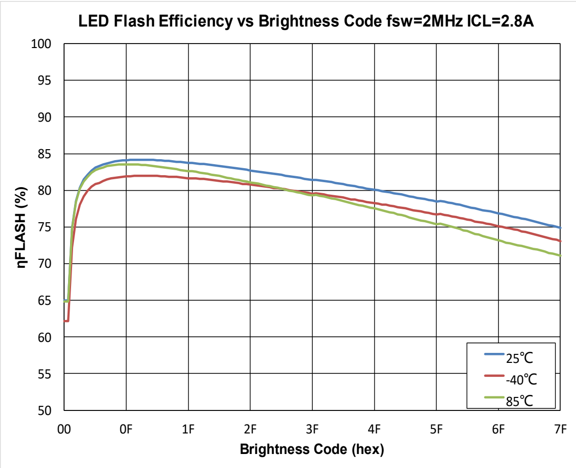


Figure 7. LED Flash Efficiency vs Brightness Code

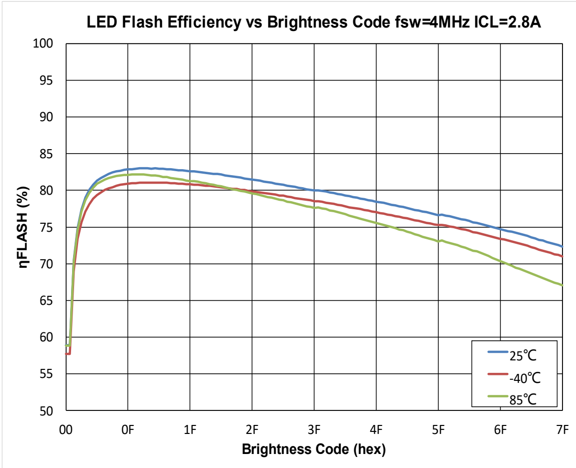


Figure 8. LED Flash Efficiency vs Brightness Code

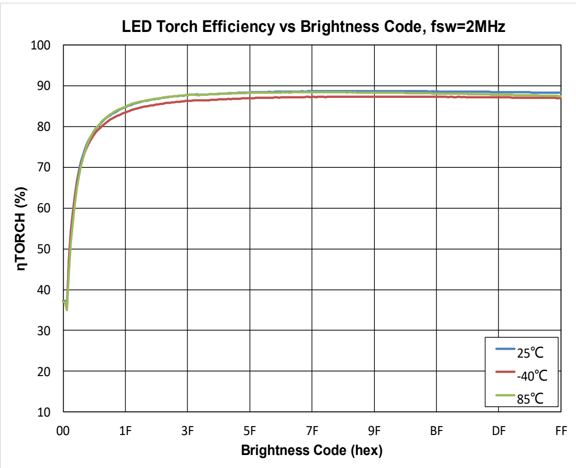


Figure 9. LED Torch Efficiency vs Brightness Code

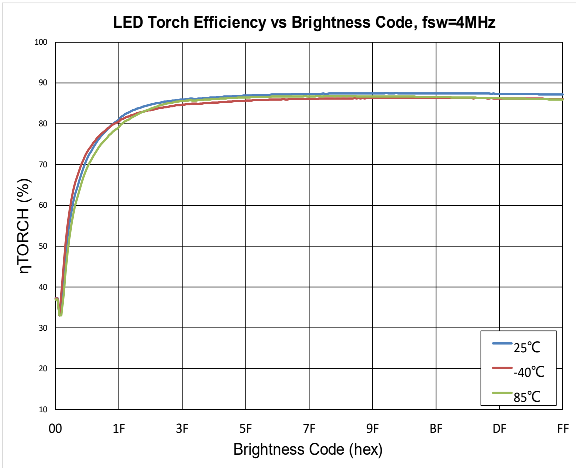


Figure 10. LED Torch Efficiency vs Brightness Code

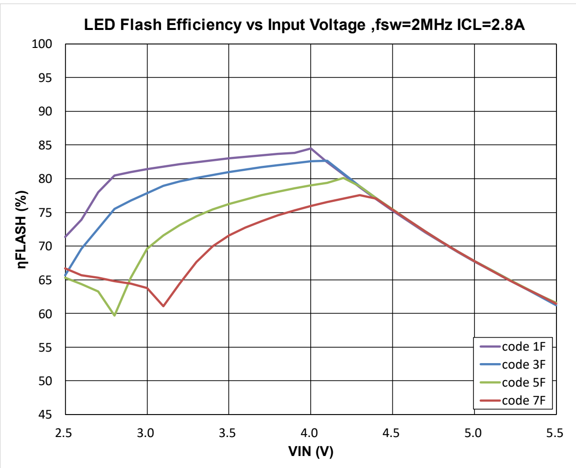


Figure 11. LED Flash Efficiency vs Input Voltage

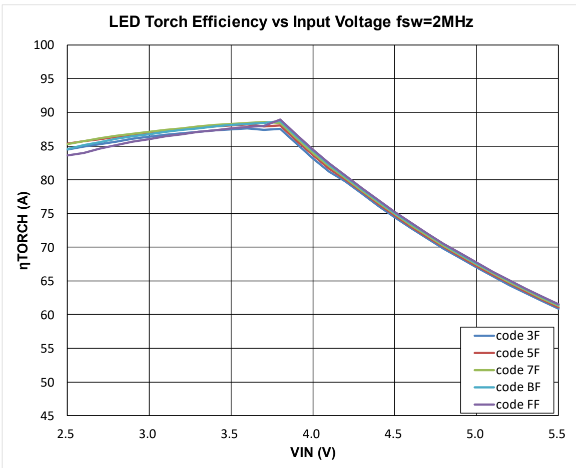


Figure 12. LED Torch Efficiency vs Input Voltage

Typical characteristics (Continued)

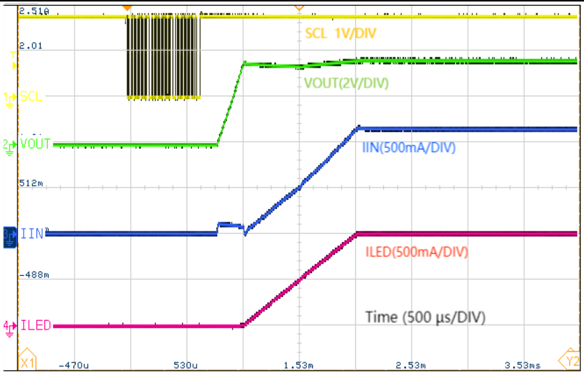


Figure 13. Flash Start-up with I²C

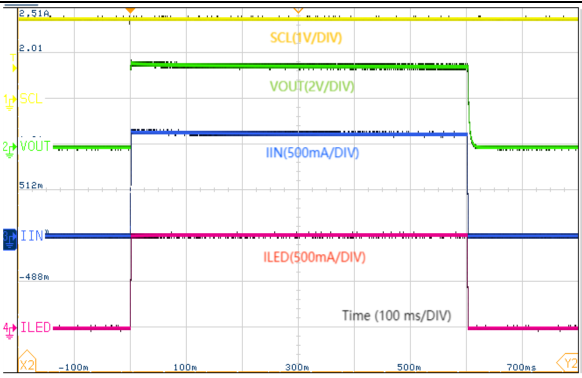


Figure 14.Flash Time-Out

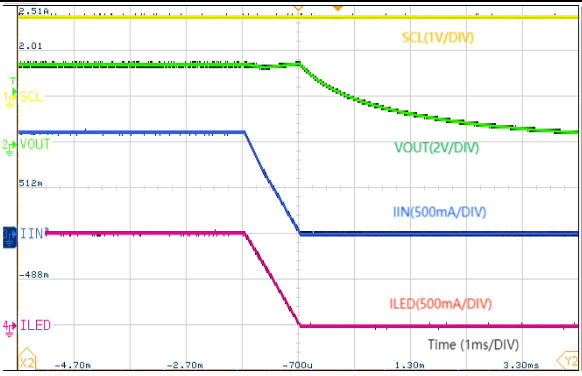


Figure 15. Flash Turnoff with I²C

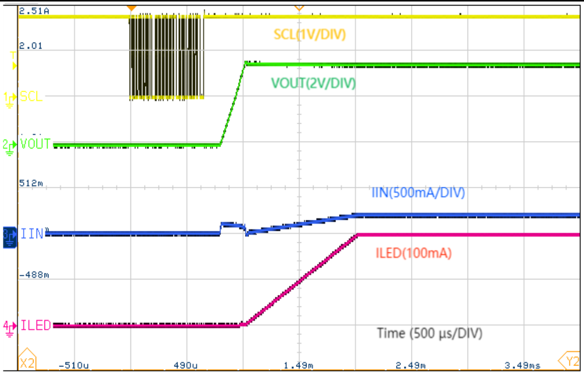


Figure 16. Torch Start-up with I²C

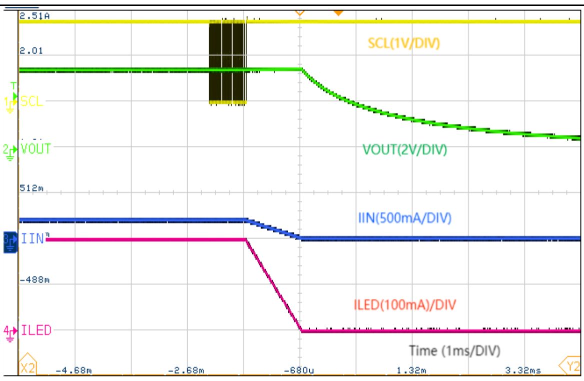


Figure 17. Torch Turnoff with I²C

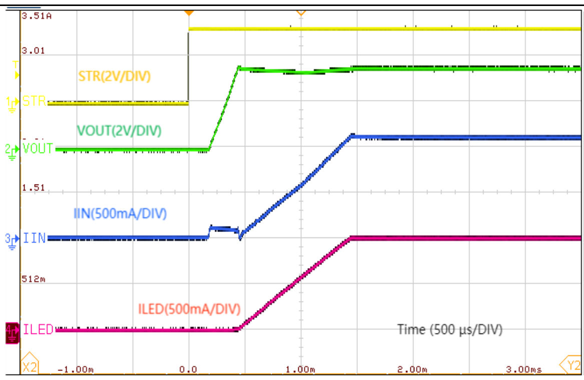


Figure 18. Flash Start-up with STROBE

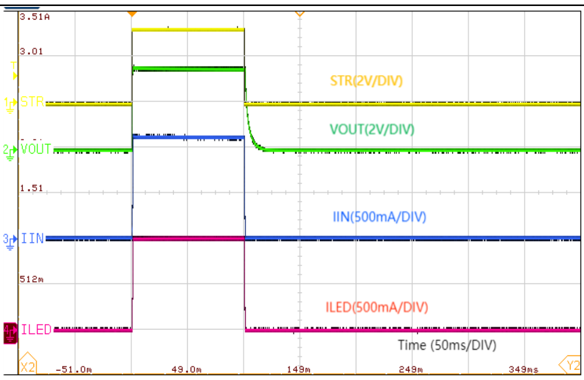


Figure 19. Flash Turnoff with Level Triggered STROBE

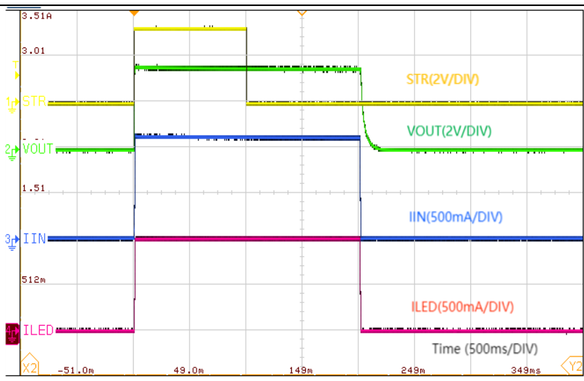
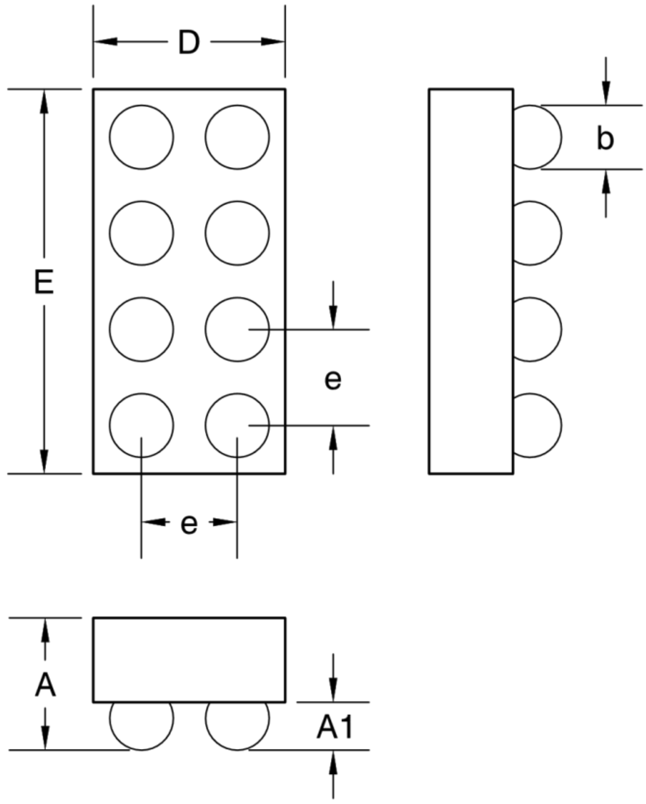


Figure 20. Flash Turnoff with Edge Triggered STROBE

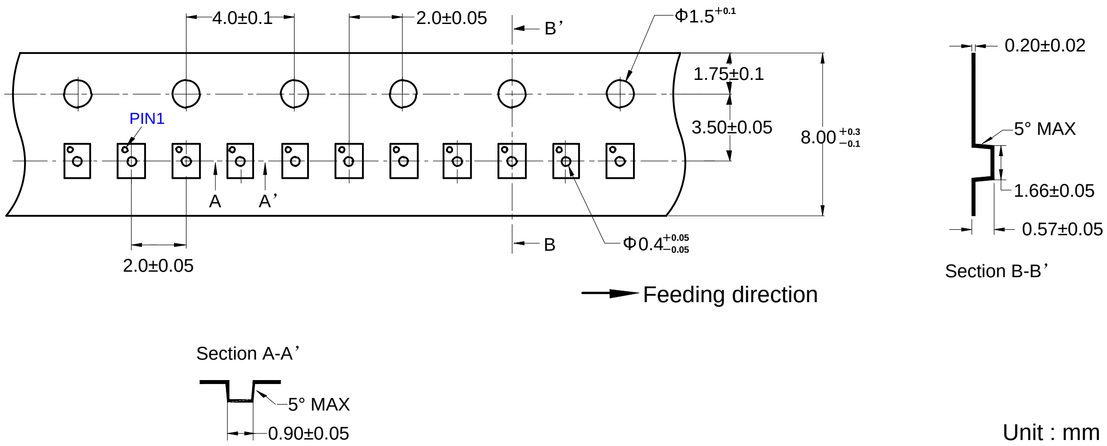
Package



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

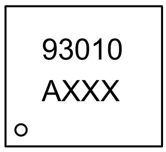
SYMBOL	MIN	NOM	MAX
A	0.394	0.447	0.500
A1	0.120	0.145	0.170
b	0.195	0.220	0.245
D	0.760	0.790	0.820
E	1.510	1.540	1.570
e	0.350BSC		

Tape Information



Unit : mm

Marking



93010 - Part Number

XXXX - Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2023-04-30	Initial Version	Lih	Liuyg	Liujy
1.0	2023-08-30	Official Version	Chenlj	Liuyg	Liujy
1.1	2023-10-24	Update EC table	Wuhesong	Liuyg	Liujy
1.2	2024-01-03	Update Package Dimension	Wuhesong	Liuyg	Liujy
1.3	2024-03-12	Update Functions Description Figure	Tugz	Liuyg	Liujy
1.4	2024-05-10	Update Tape Information	Wuhs,shib	Liuyg	Liujy
1.5	2025-06-24	Update TSB	Wuhs	Liuyg	Liujy