3A, Low-noise (3.9μV) Voltage Regulator

General Description

The ET5CS0XX is a low-noise (3.9μV_{RMS}), low- dropout voltage regulator (LDO) capable of sourcing a 3A load with low dropout. The output voltages are fully user-adjustable using a printed circuit board (PCB) layout without the need of external resistors, thus reducing overall component count. For higher output voltage applications, the device achieves output voltages up to 5V with the use of external resistors. The device supports very low input voltages (down to 1.0V) with the use of an additional BIAS rail.

With very high accuracy, remote sensing, and soft-start capabilities to reduce inrush current, the ET5CS0XX is ideal for powering high-current, low-voltage devices such as high-end microprocessors and field-programmable gate arrays.

The ET5CS0XX is designed to power-up noise-sensitive components in high-speed communication applications. The very low-noise, 3.9μV_{RMS} device output and high broad-bandwidth PSRR minimizes phase noise and clock jitter in high-frequency signals. These features maximize performance of clocking devices, analog-to-digital converters, and digital-to-analog converters.

Features

- Ultra-low Dropout: 100mV TYP at 3A
- Output Voltage Noise: 3.9μV_{RMS}
- Power-Supply Ripple Rejection: 80dB at 1kHz
- Input Voltage Range: Without BIAS:1.4V to 6.5V; With BIAS:1.0V to 6.5V
- Two Output Voltage Modes:
  - -- Programmable output Version: Output Voltage Range: 0.6V to 3.75V (ET5CS01X)
  - -- Programmable output Version: Output Voltage Range: 0.6V to 2.175V (ET5CS02X)
  - -- Adjustable Version: Output Voltage Range: 0.6V to 5.2V (ET5CS01X, ET5CS02X, ET5CS03X)
- 1.5% Accuracy Over Line, Load, and Temperature
- Programmable Soft-Start Output
- Power-Good (PG) Output
- Built-in Under Voltage Lockout (UVLO)
- Built-in Internal Current Limit

Device Information

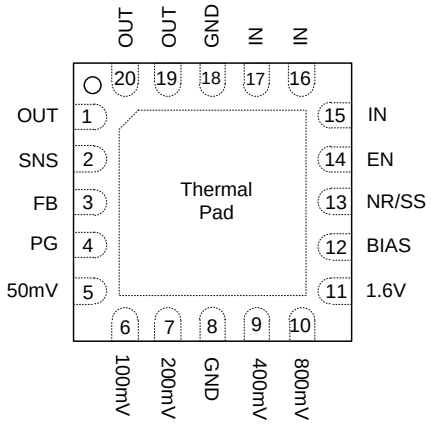
ET5CS0 X X

Part No. X		Package X		Packing Option	MSL
ET5CS01X	0.6~5.2V adj (50mV/step)	Y	QFN20 (5mm×5mm)	Tape and Reel ,3K	Level 3
ET5CS02X	0.6~5.2V adj (25mV/step)				
ET5CS03X	0.6~5.2V adj	Y1	QFN20 (3.5mm×3.5mm)	Tape and Reel ,3K	Level 3

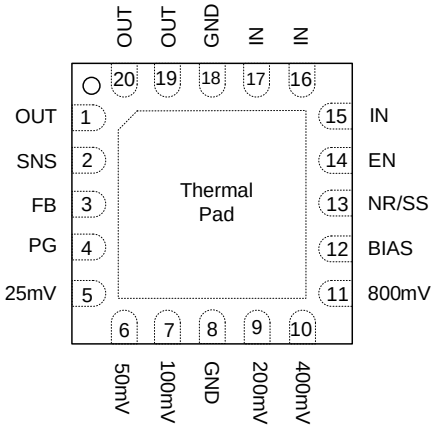
Applications

- RF, IF Components: VCO, ADC, DAC, LVDS
- Wireless Infrastructure: FPGA, DSP
- Test and Measurement
- Instrumentation, Medical, and Audio

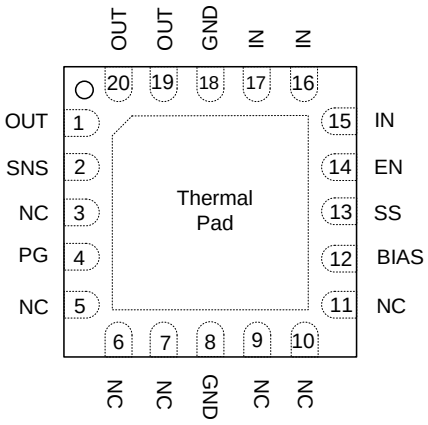
Pin Configuration



QFN20 (ET5CS01X)



QFN20 (ET5CS02X)



QFN20 (ET5CS03X)

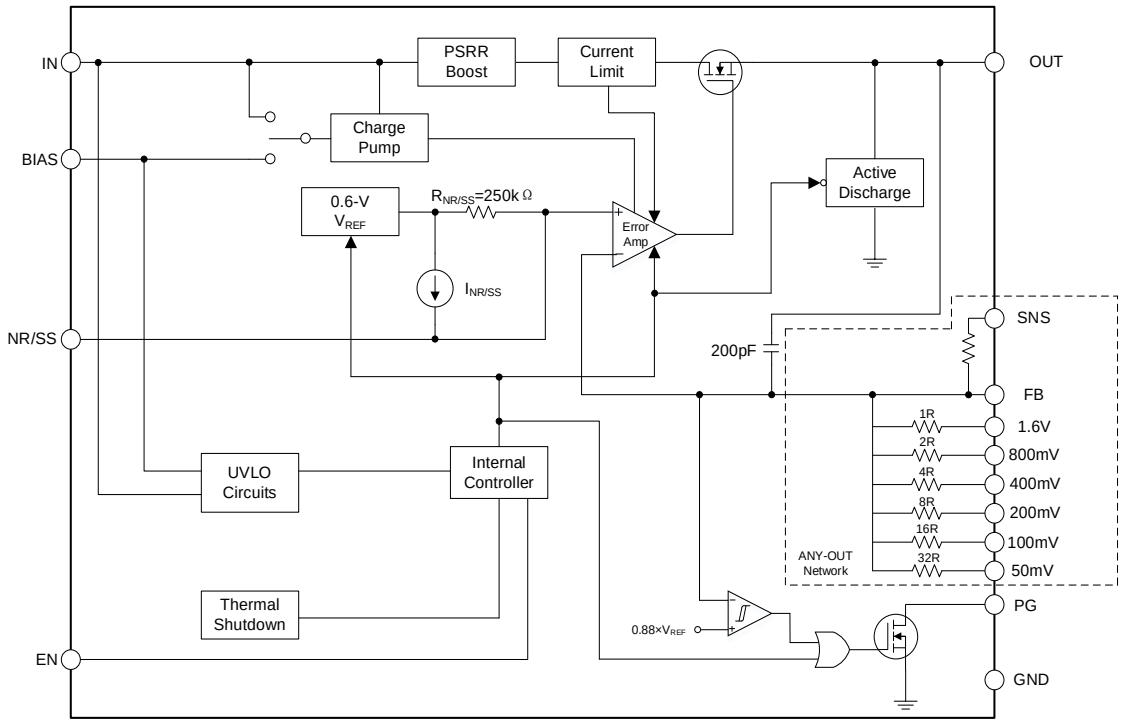
Top View

Pin Function

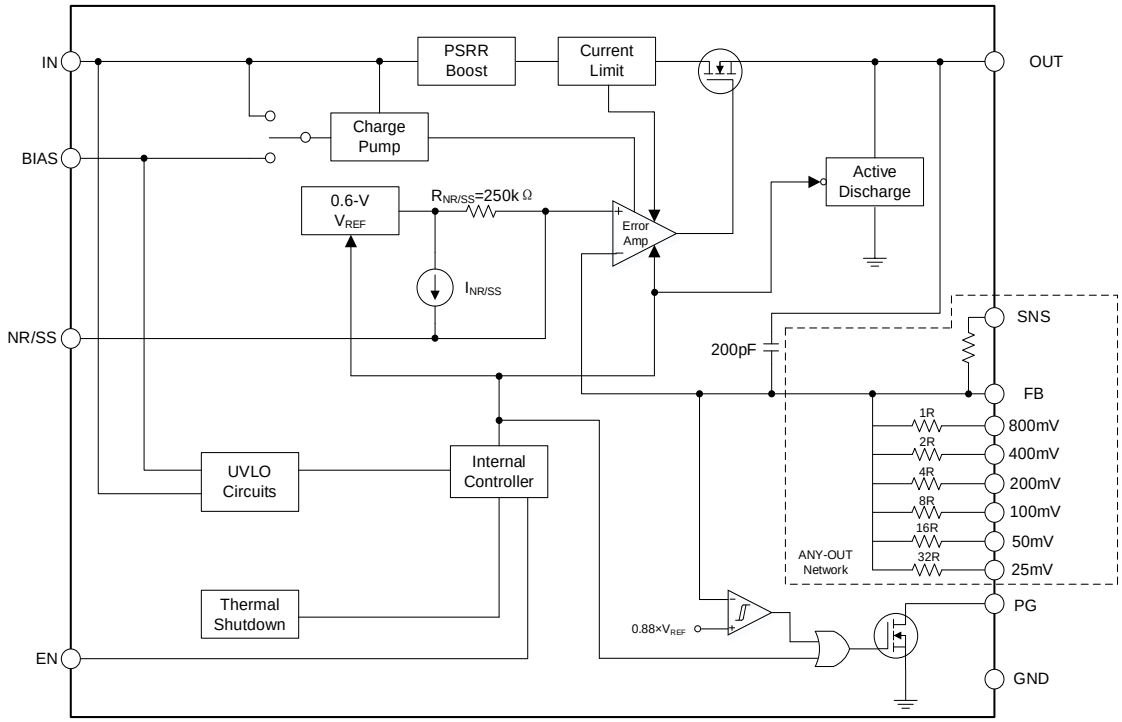
ET5CS01X	ET5CS02X	ET5CS03X	Pin Name	Pin Function
1,19,20	1,19,20	1,19,20	OUT	Regulated output pin. A ceramic capacitor is required for stability.
2	2	2	SNS	Output voltage sense input pin. Connect this pin only if the Programmable output feature is used.
3	3	-	FB	Output voltage feedback pin connected to the error amplifier. Although not required, a 10nF feed-forward capacitor from FB to OUT (as close to the device as possible) is recommended for low-noise applications to maximize ac performance. The use of a feed-forward capacitor may disrupt PG (power good) functionality. See the Programmable Output Voltage and Adjustable Operation sections for more details.
4	4	4	PG	Active-high power-good pin. An open-drain output indicates when the output voltage reaches the target. The use of a feed-forward capacitor may disrupt PG functionality.
-	5	-	25mV	Output voltage setting pins. Connect these pins to ground or leave floating. Connecting these pins to ground increases the output voltage by the value of the pin name; multiple pins can be simultaneously connected to GND to select the desired output voltage. Leave these pins floating (open) when not in use. See the Programmable Output Voltage section for more details.
5	6	-	50mV	
6	7	-	100mV	
7	9	-	200mV	
9	10	-	400mV	
10	11	-	800mV	
11	-	-	1.6V	
-	-	3,5,6,7, 9,10,11	NC	No connect.
8,18	8,18	8,18	GND	Ground pin.
12	12	12	BIAS	BIAS supply voltage pin for the use of 1.0V ≤ IN ≤ 1.4V and to connect a 10μF capacitor between this pin and ground.
-	-	13	SS	Soft-start pin.
15,16,17	15,16,17	15,16,17	IN	Input supply voltage pin. A 10μF input ceramic capacitor is required.

13	13	-	NR/SS	Noise-reduction and soft-start pin. Connecting an external capacitor between this pin and ground reduces reference voltage noise and also enables the soft-start function. Although not required, a capacitor is recommended for low-noise applications to connect a 10nF capacitor from NR/SS to GND (as close to the device as possible) to maximize ac performance.
14	14	14	EN	Enable pin. Driving this pin to logic high enables the device; Driving this pin to logic low disables the device. See the Start-Up section for more details.
Thermal Pad				Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

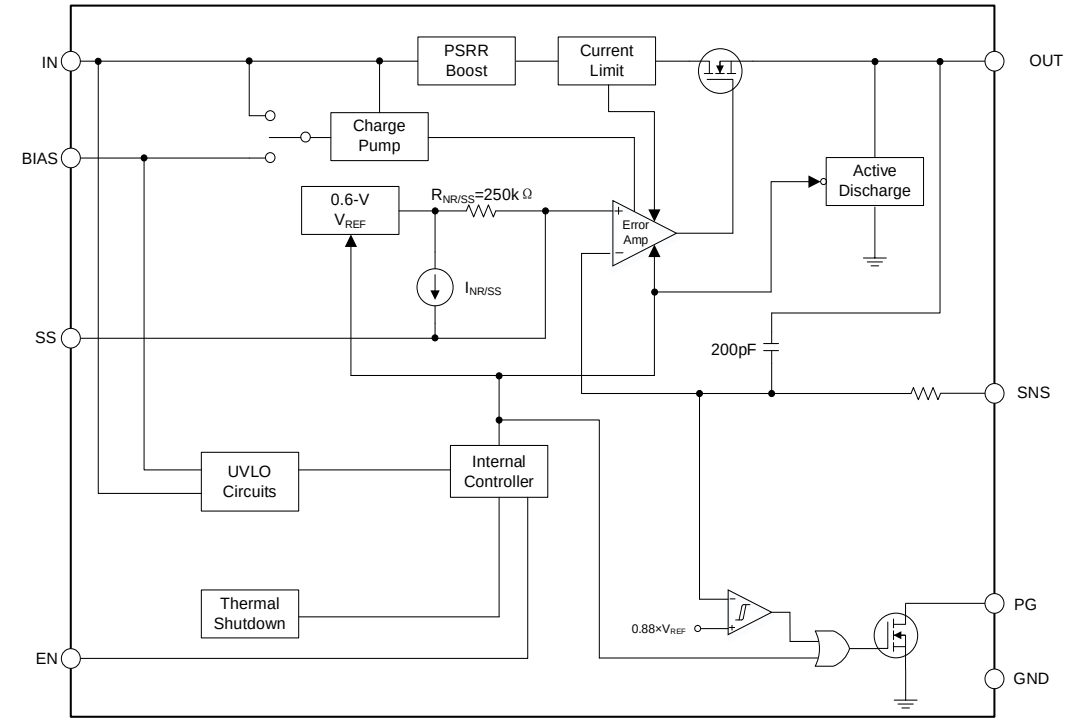
Block Diagram



ET5CS01X



ET5CS02X



ET5CS03X

Functional Description

Overview

The ET5CS0XX is a low-noise, high PSRR, low-dropout regulator capable of sourcing a 3A load with low dropout. The ET5CS0XX can operate down to 1.0V input voltage and 0.6V output voltage. This combination of low noise, high PSRR, and low output voltage makes the device an ideal low dropout regulator to power a multitude of loads from noise-sensitive communication components in high-speed communication applications to high-end microprocessors or field-programmable gate array.

The ET5CS0XX block diagram contains several features, including:

- With an internal charge pump;
- Low-noise, 0.6V reference;
- Internal protection circuitry: UVLO, Internal current limit, TSD;
- Programmable soft-start;
- Power-good output;
- An integrated resistance network (Programmable output) with a 50mV minimum resolution.

Device Functional Modes

- Operation with $1.0V>V_{IN}>1.4V$

The ET5CS0XX requires a bias voltage on the BIAS pin≥3.0V if the high-current input supply voltage is between 1.0V to 1.4V. The bias voltage pin consumes 2.4mA, nominally.

- Operation with $1.4V\geq V_{IN}>6.5V$

If the input voltage is equal to, or exceeds 1.4V, no bias voltage is necessary. The device is automatically selected to be powered from the IN pin in this condition and the BIAS pin can be left floating.

- Disabled

If the voltage on the EN pin is less than 0.4V, the device is disabled and the output is high impedance. The output impedance of the LDO is then set by the gain setting resistors if a path to GND is provided between OUT and GND. In this state, quiescent current does not exceed 2.5μA. Raising EN above 0.8V (minimum) initiates the startup sequence of the device.

Start-Up

- Enable (EN) and Under voltage Lockout (UVLO)

The ET5CS0XX only turns on when both EN and UVLO are above the respective voltage thresholds. The UVLO circuit monitors input and bias voltage (V_{IN} and V_{BIAS}, respectively) to prevent device turn-on before V_{IN} and V_{BIAS} rise above the lockout voltage. The UVLO circuit also causes a shutdown when V_{IN} and V_{BIAS} fall below lockout. The EN signal allows independent logic-level turn-on and shutdown of the LDO. If the device turn-on is required to be controlled, the device must be enabled with or after V_{IN}. Connect EN to VIN if turn-on control of the output voltage is not needed.

Feature Description

Programmable Output Operation

The ET5CS0XX does not require external resistors to set output voltage, which is typical of adjustable low-dropout voltage regulators. However, the ET5CS01X/ET5CS02X uses pins 5, 6, 7, 9, 10, and 11 to program the regulated output voltage. Each pin is either connected to ground (active) or left open (floating). Programmable output programming is set by Equation 1 as the sum of the internal reference voltage (V_{REF}=0.6V) plus the accumulated sum of the respective voltages assigned to each active pin; that is (Such as ET5CS01X), 50mV (pin5), 100mV (pin6), 200mV (pin7), 400mV (pin9), 800mV (pin10), or 1.6V (pin11). By leaving all program pins open, or floating, the output is thereby programmed to the minimum possible output voltage equal to V_{REF}.

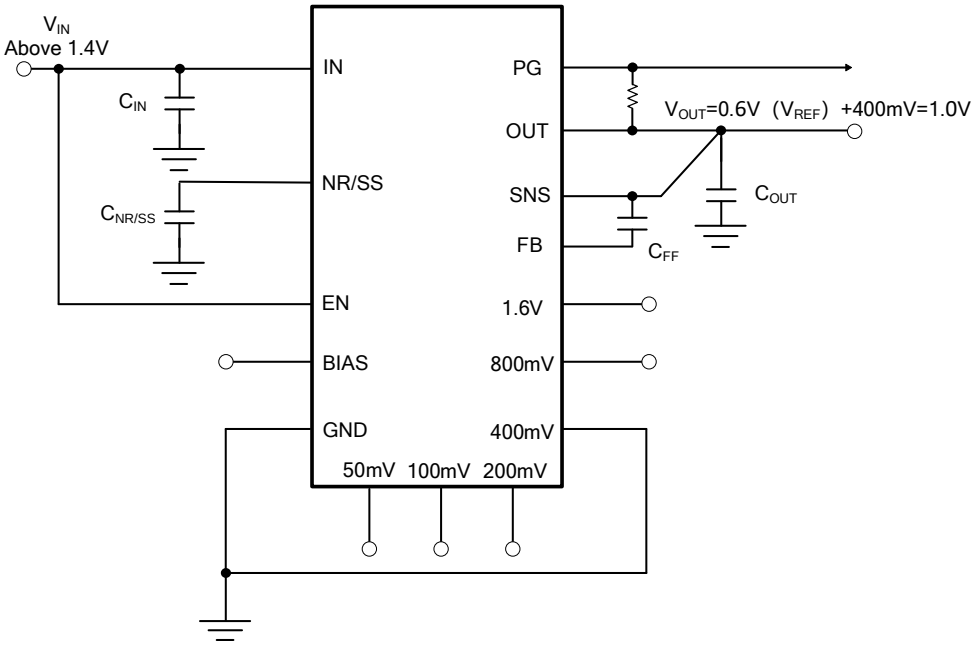
$V_{OUT}=V_{REF}+(\sum$Pins to Ground)

Program Pins (Active Low)	Additive Output Voltage Level
Pin 5 (50/25mV)	50/25mV
Pin 6 (100/50mV)	100/50mV
Pin 7 (200/100mV)	200/100mV
Pin 9 (400/200mV)	400/200mV
Pin 10 (800/400mV)	800/400mV
Pin 11 (1.6/0.8V)	1.6/0.8V

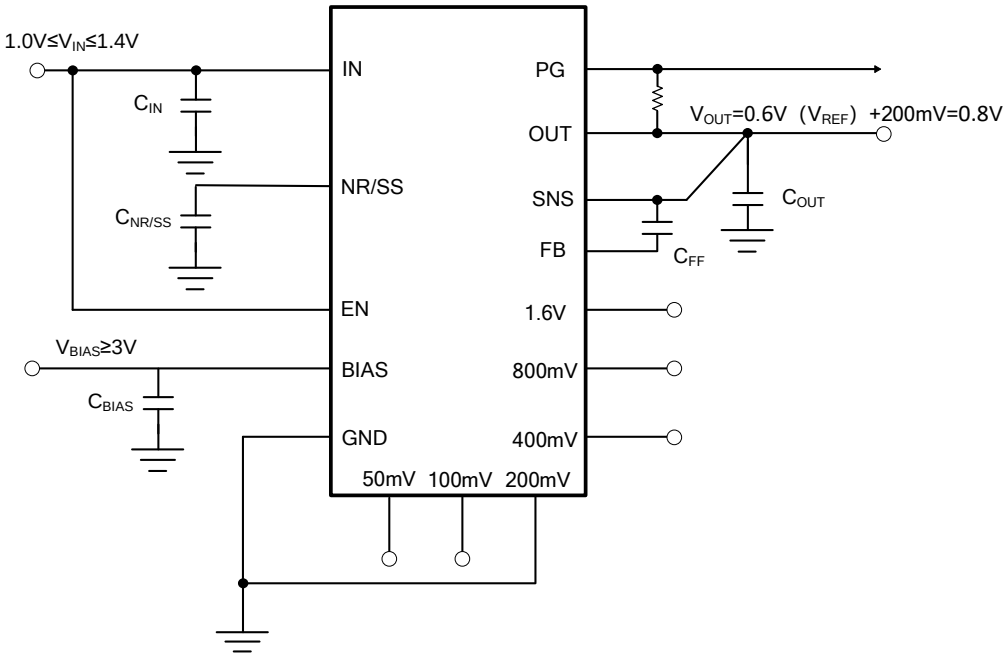
The voltage setting pins have a binary weight; therefore (Such as ET5CS01X), the output voltage can be programmed to any value from 0.6V to 3.75V in 50mV steps. As followed: Binary 0 means the pin is open, Binary 1 means the pin is connected to GND. It is possible to connect any pin of the internal resistance network Pin5~Pin11 to the SNS pin, which can increase the resolution by 50%, from 50mV to 25mV, but the output voltage range will be limited.

Fixed output voltage setting reference (ET5CS01X)	
{1.6V,800mv, 400mv, 200mv, 100mv, 50mv}	Output Voltage(V)
00_0000(default)	0.60
00_0001	0.65
00_0010	0.70
……	……
10_0000	2.20
10_0001	2.25
10_0010	2.30
……	……
11_1101	3.65
11_1110	3.70
11_1111	3.75

Considering the use of the programmable output internal network, the output voltage is set by grounding the appropriate control pins. When grounded, all control pins add a specific voltage on top of the internal reference voltage (V_{REF}=0.6V). The followed figures show a 1.2V and 1V output voltage, respectively, that provide an example of the circuit usage with and without BIAS voltage. These schematics are described in more detail in the Application Circuits.



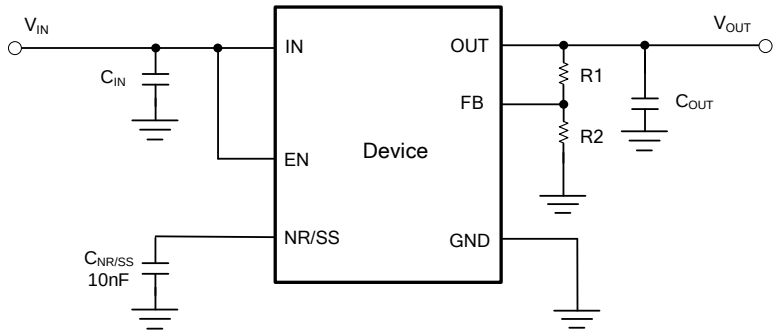
Typical application: V_{IN}≥1.4V (1.4V Input, 1.0V Output, no external BIAS)



Typical application: 1.0V≤V_{IN}<1.4V (1.4V Input, 0.8V Output, 3V BIAS voltage)

Adjustable Operation

The ET5CS0XX can be used either with the internal programmable output network or using external resistors. Using the programmable output network allows the ET5CS01/02X to be programmed from 0.6V to 5.2V. This configuration is referred to as the adjustable configuration of the ET5CS0XX throughout this document. Regardless whether the internal resistor network or whether external resistors are used, the nominal output voltage of the device is set by two resistors. Using an internal resistor ensures a 1% matching and minimizes both the number of external components and layout footprint.



Adjustable Operation for Maximum AC Performance

R1 and R2 can be calculated for any output voltage range using followed Equation.

$$V_{OUT}=V_{REF}*(1+R1/R2)$$

The followed table shows the resistor combination required to achieve a few of the most common rails using commercially-available, 0.1%-tolerance resistors to maximize nominal voltage accuracy while abiding to the formula shown in. Recommended feedback resistor values (R1+R2) <100KΩ.

Recommended Feedback Resistance			
Target Output Voltage（V）	Feedback Resistance Value		Calculate Output Voltage（V）
	R1（kΩ）	R2（kΩ）	
0.7	12.1	72	0.700
0.75	12.1	48.7	0.749
0.8	12.1	36	0.802
0.9	12.1	24	0.903
1.0	12.1	18	1.003
1.05	12.1	16	1.054
1.1	12.1	14.7	1.094
1.2	12.1	12.1	1.200
1.5	12.1	8.06	1.501
1.8	12.1	6.04	1.802
3	12.1	3.01	3.012
5.0	12.1	1.65	5.000
5.2	12.1	1.58	5.195

3A LDO with an Internal Charge Pump

The ET5CS0XX can be used either with the internal resistor network provided, or with the external component as a traditional adjustable LDO. Regardless of the implementation, the ET5CS0XX provides excellent regulation to 1.5% accuracy, excellent dropout voltage, and high output current capability.

If the input voltage is below 1.4V, an external BIAS voltage must be supplied to maintain the dropout characteristics. The input voltage or the BIAS voltage is fed through to an internal charge pump to power the internal error amplifier providing the regulation.

The internal charge pump ensures proper operation without requiring an external BIAS voltage down to +1.4V input voltage. Below a 1.4V input voltage, a BIAS input voltage between 3.0V and 5.5V is required.

Low-Noise, 0.6V Reference

The ET5CS0XX includes a low-noise reference ensuring minimal noise during operation because the internal reference is normally the dominant term in noise analysis. Further noise reduction can be achieved using the NR/SS pin and by adding an external C_{FF} between the SNS pin and the FB pin.

Under voltage Lockout (UVLO)

The under-voltage lockout (UVLO) circuit monitors the input and bias voltage (V_{IN} and V_{BIAS}, respectively) to prevent the device from turning on before VIN and VBIAS rise above the lockout voltage. The UVLO circuit also causes a shutdown when V_{IN} and V_{BIAS} fall below the lockout voltage.

Internal Current Limit (I_{LIMIT})

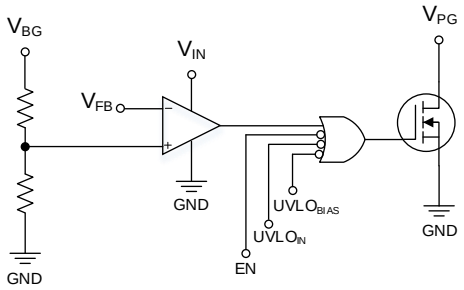
The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. Note also that if a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting in a thermal shutdown of the output.

A fold back feature limits the short-circuit current to protect the regulator from damage under all load conditions. If V_{OUT} is forced below 0 V before EN goes high and the load current required exceeds the fold back current limit, the device does not start up. In applications that function with both a positive and negative voltage supply, there are several ways to ensure proper start-up:

- Enable the ET5CS0XX first and disable the device last.
- Delaying the EN voltage with respect to the IN voltage allows the internal pull-down resistor to discharge any residual voltage at V_{OUT}. If a faster discharge rate is required, use an external resistor from OUT to GND.

Power Good (PG)

The PG signal provides a concise solution for monitoring the power status of the system. When the output voltage approaches, equals, or exceeds the set output voltage $V_{OUT\ (nom)}$, the PG circuit sets the PG pin to a high impedance state, and the PG is pulled to a high level to indicate that the power status is good. The PG signal is an open drain output structure that requires a pull-up resistor to be connected to an external power source. The pull-up resistor is generally recommended to be 10-100K ohm.



Thermal Shutdown Protection (TSD)

Thermal shutdown disables the output when the junction temperature rises to approximately 160°C which allows the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the ET5CS0XX has been designed to protect against temporary thermal overload conditions. The TSD circuitry was not intended to replace proper heat-sinking. Continuously running the ET5CS0XX device into thermal shutdown may degrade device reliability

Programmable Soft-Start

Soft-start refers to the ramp-up characteristic of the output voltage during LDO turn-on after EN and UVLO exceed the respective threshold voltage. The noise-reduction capacitor ($C_{NR/SS}$) serves a dual purpose of both governing output noise reduction and programming the soft-start ramp during turn-on.

Power-Good Function

The ET5CS0XX has a power-good function that works by toggling the state of the PG output pin. When the output voltage falls below the PG threshold voltage, the PG pin open-drain output engages (low impedance to GND). When the output voltage exceeds the PG threshold voltage by an amount greater than VHYS (PG), the PG pin becomes high-impedance. By connecting a pull-up resistor to an external supply, any downstream device can receive PG as a logic signal. Make sure that the external pull-up supply voltage results in a valid logic signal for the receiving device or devices. Use a pull-up resistor from 10kΩ to 100kΩ for best results.

When employing the feed-forward capacitor (C_{FF}), the turn-on time-constant for the LDO is increased and the power-good output time-constant stays the same, resulting in an invalid status of the LDO. To avoid this issue and receive a valid PG output, ensure that the time-constant of both the LDO and the power-good output match.

Capacitor Recommendation

The ET5CS0XX is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR, pin13). Ceramic capacitors that employ X7R, X5R, and COG rated dielectric materials provide relatively good capacitive stability across temperature.

- Input and Output Capacitor Requirements (C_{IN} and C_{OUT})

The ET5CS0XX is designed and characterized for operation with ceramic capacitors of 47μF||10μF||10μF or greater at the output can effectively improve the PSRR, while also meeting the minimum effective capacitance requirements for different output voltages and 47μF(Effective capacitance value ≥ 22 μF) at the input. Locate the input and output capacitors as near as practical to the respective input and output pins.

- Feed-Forward Capacitor (C_{FF})

Although a feed-forward capacitor (C_{FF}), from the FB pin to the OUT pin is not required to achieve stability, a 10nF, feed-forward capacitor optimizes the noise and PSRR performance. A higher capacitance C_{FF} can be used; However, the startup time is longer and the power-good signal may incorrectly indicate the output voltage has settled.

- Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)

The ET5CS0XX features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor ($C_{NR/SS}$). This soft-start eliminates power-up initialization problems when powering field-programmable gate arrays (FPGAs), digital signal processors (DSPs), or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transients to the input power bus.

To achieve a linear and monotonic start-up, the ET5CS0XX error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft- start charging current ($I_{NR/SS}$), the soft-start capacitance ($C_{NR/SS}$), and the internal reference (V_{REF}). Soft- start ramp time can be calculated as followed:

$$\mathbf{t_{SS} = (V_{REF} \times C_{NR/SS}) / I_{NR/SS}}$$

***Note*:** That $I_{NR/SS}$ is provided in the Electrical Characteristics table and has a typical value of 6μA

For low-noise applications, the noise reduction capacitor and noise reduction resistor together form a low-pass filter (LPF), which filters out noise from the reference before utilizing the gain of the error amplifier, thereby reducing the background noise of the device. LPF is a single pole filter, and the cutoff frequency can be calculated by $F_{cutoff}=1/(2 \times \pi \times R_{NR/SS} \times C_{NR/SS})$. The typical value of $R_{NR/SS}$ is 250 kΩ. For low-noise applications, a 10nF to 1μF $C_{NR/SS}$ is recommended, also it is necessary to consider the impact of large capacitors on startup time.

Absolute Maximum Ratings

Symbol	Parameters (Items)		Value	Unit
$V_{IN}/V_{BIAS}/V_{PG}/V_{EN}$	IN, BIAS, PG, EN Voltage		-0.3 to 6.5	V
V_{SNS}/V_{OUT}	SNS, Output Voltage		-0.3 to 6.5	V
$V_{NR/SS}/V_{FB}$	NR/SS, FB Output Voltage		-0.3 to 2	V
V_{OTHER_PINS}	50/25mV, 100/50mV, 200/100mV, 400/200mV, 800/400mV, 1.6/0.8V Voltage		-0.3 to V_{OUT}+0.3	V
I_{OUT_MAX}	Maximum Load Current		4500	mA
I_{PG_MAX}	PG (sink current into device)		5	mA
P_D	Maximum Power Consumption	QFN20(5*5)	2000	mW
V_{ESD}	Human Body Model (JESD22-A114)		±2000	V
	Charged Device Model (JESD22-C101)		±1000	
$R_{\theta JA}$	Junction-to-ambient Thermal Resistance		62.5	°C/W
T_J	Operating Junction Temperature		-40 to 150	°C
T_{STG}	Storage Temperature		-65 to 150	°C
T_{SLOD}	Lead Temperature (Soldering, 10 sec)		300	°C

Recommended Operating Conditions

Symbol	Parameters	Rating	Unit
V_{IN}	Input Voltage	1.0 to 6.5	V
V_{BIAS}	Supply Bias Voltage	3.0 to 6.5	V
V_{OUT}	Output Voltage Range (ET5C001X/ET5C002X)	0.6 to 5.2	V
I_{OUT}	Output Current	0 to 3000	mA
T_J	Operating Junction Temperature	-40 to 125	ºC
C_{IN}	Effective Input Ceramic Capacitor Value	Min 10, Typ 47	μF
C_{BIAS}	Effective Input Ceramic Capacitor Value	Min 1, Typ 10	μF
C_{OUT}	Effective Output Ceramic Capacitor Value	Min 47, Typ 47||10||10	μF
R_{PG}	PG Pull-up Resistor	10~100	kΩ
$C_{NR/SS}$	Effective NR/SS Ceramic Capacitor Value	10~1000	nF
ESR	Input and Output Capacitor Equivalent Series Resistance (ESR)	5 to 100	mΩ

Electrical Characteristics

Over operating temperature range (T_J=-40°C to 125°C), {1.0V≤V_{IN}<1.4V and 3.0V≤V_{BIAS}≤6.5V} or {V_{IN}≥1.4V and V_{BIAS} open}[(1)], V_{IN}≥$V_{OUT(TARGET)}$+0.4V[(2)], $V_{OUT(TARGET)}$=0.6V, V_{EN}=1.4V, C_{IN}= 47μF || 10μF || 10μF, C_{OUT}= 47μF || 10μF || 10μF, $C_{NR/SS}$=10nF, C_{FF}=100nF, and PG pin pulled up to V_{IN} with 100kΩ, unless otherwise noted.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range		1.0		6.5	V
V_{BIAS}	Bias supply voltage[(1)]		3.0		6.5	V
V_{REF}	Reference voltage	V_{REF}=V_{FB}=$V_{NR/SS}$		0.6		V
$V_{UVLO1(IN)}$	Input supply UVLO with BIAS	V_{IN} increasing		0.9	1	V
$V_{HYS1(IN)}$	$V_{UVLO1(IN)}$ hysteresis	V_{IN} falling		250		mV
$V_{UVLO2(IN)}$	Input supply UVLO without BIAS	V_{IN} increasing		1.3	1.39	V
$V_{HYS2(IN)}$	$V_{UVLO2(IN)}$ hysteresis	V_{IN} falling		350		mV
$V_{UVLO(BIAS)}$	Bias supply UVLO	V_{BIAS} increasing		2.8	2.9	V
$V_{HYS(BIAS)}$	$V_{UVLO(BIAS)}$ hysteresis	V_{BIAS} falling		260		mV
V_{OUT}	Output voltage	Use internal resistor to adjust output	0.6	3.750 2.175	4.163 2.414	V
		Use external resistor to adjust output	0.6		5.717	
	Output voltage Accuracy[(3)(4)]	0.6V ≤ V_{OUT} ≤ 5.15V, 5mA ≤ I_{OUT} ≤ 3A	-1.5		1.5	%
		1.1V ≤ V_{IN} ≤ 2.2V, 3.0V ≤ V_{BIAS} ≤ 6.5V, 5mA ≤ I_{OUT} ≤ 3A	-0.9		0.9	
△V_{OUT}	Output Voltage Line Regulation	V_{IN} = V_{OUT} + 0.4V or 1.4V to 6.5V, I_{OUT} = 5mA		0.03	1.6	mV/V
	Output Voltage Load Regulation	I_{OUT} from 1mA to 3000mA		0.5		mV/A
V_{DROP}	Dropout Voltage	V_{IN} = 1.4V, V_{OUT}=1V I_{OUT} = 3000mA		100	250	mV
I_{LIMIT}	Current Limit	V_{OUT} forced at 0.9×$V_{OUT(TARGET)}$, V_{IN} = V_{OUT} + 0.4V or 1.4V		4500	5700	mA
$I_{NR/SS}$	NR/SS Pin Current	$V_{NR/SS}$=GND, V_{IN}=6.5V	4	6	9	μA
I_{FB}	FB Pin Current	V_{IN}=6.5V	-100		100	nA

Electrical Characteristics (Continued)

Over operating temperature range (T_J=-40°C to 125°C), {1.0V≤V_{IN}<1.4V and 3.0V≤V_{BIAS}≤6.5V} or {V_{IN}≥1.4V and V_{BIAS} open}[(1)], V_{IN}≥$V_{OUT(TARGET)}$+0.4V[(2)], $V_{OUT(TARGET)}$=0.6V, V_{EN}=1.4V, C_{IN}= 47 µF || 10µF || 10µF, C_{OUT}= 47µF || 10µF || 10µF, $C_{NR/SS}$=10nF, C_{FF}=100nF, and PG pin pulled up to V_{IN} with 100kΩ, unless otherwise noted.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
I_{GND}	GND pin current	Minimum load, V_{IN}=6.5V, no V_{BIAS} supply, I_{OUT}=5mA		3000	4000	µA
		Maximum load, V_{IN}=1.4V, no V_{BIAS} supply, I_{OUT}=3A		4000	5500	
		Shutdown, PG=(open), V_{IN}=6.5V, no V_{BIAS} supply, V_{EN}=0V		1.2	25	
I_{EN}	EN pin input current	V_{IN}=6.5V, no V_{BIAS} supply, V_{EN}=0V and 6.5V	-0.1		0.1	µA
I_{BIAS}	BIAS pin current	V_{IN}=1.1V, V_{BIAS}=6.5V, $V_{OUT(TARGET)}$=0.6V, I_{OUT}=3A		2.4	3.5	mA
$V_{IL(EN)}$	EN Low Threshold	V_{EN} falling from 1.2V	0		0.4	V
$V_{IH(EN)}$	EN High Threshold	V_{EN} increasing from 0V	0.8		6.5	V
$V_{IT(PG)}$	PG pin threshold	V_{OUT}/ V_{OUT_SET}, when V_{OUT} rising	0.82* V_{OUT}	0.9* V_{OUT}	0.93* V_{OUT}	V
$V_{HYS(PG)}$	PG pin hysteresis	V_{OUT}/ V_{OUT_SET}, when V_{OUT} falling		0.05* V_{OUT}		V
$V_{OL(PG)}$	PG pin low-level output voltage	V_{OUT}<$V_{IT(PG)}$, I_{PG}=-1mA (current into device)		0		V
$I_{LEAK(PG)}$	PG pin leakage current	V_{OUT}>$V_{IT(PG)}$, $V_{(PG)}$=6.5V		<1		µA
$I_{NR/SS}$	NR/SS pin charging current	$V_{NR/SS}$=GND, V_{IN}=6.5V	4.0	6.0	9.0	µA
I_{FB}	FB pin leakage current	V_{IN}=6.5V	-100		100	nA
PSRR	Power Supply Rejection Ratio[(5)] (V_{IN} – V_{OUT} = 0.4V,I_{OUT} = 3 A, $C_{NR/SS}$ = C_{IN} = 100 nF,C_{FF} = 10 nF)	f = 1kHz, V_{OUT} = 0.6V, V_{BIAS} = 5V		80		dB
		f = 100kHz, V_{OUT} = 0.6V, V_{BIAS} = 5V		45		
		f = 1MHz, V_{OUT} = 0.8V, V_{BIAS} = 5V		40		

Electrical Characteristics (Continued)

Over operating temperature range (T_J=-40°C to 125°C), {1.0V≤V_{IN}<1.4V and 3.0V≤V_{BIAS}≤6.5V} or {V_{IN}≥1.4V and V_{BIAS} open}(1), V_{IN}≥$V_{OUT(TARGET)}$+0.4V(2), $V_{OUT(TARGET)}$=0.6V, V_{EN}=1.4V, C_{IN}= 47 µF || 10µF || 10µF, C_{OUT}= 47µF || 10µF || 10µF, $C_{NR/SS}$=10nF, C_{FF}=100nF, and PG pin pulled up to V_{IN} with 100kΩ, unless otherwise noted.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
e_N	Output noise(5)	BW = 10 Hz to 100 kHz, V_{IN}=1.1V, V_{OUT} = 0.8 V, V_{BIAS} = 5.0 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 47 µF || 10µF || 10µF		3.9		µV_{RMS}
		BW = 10 Hz to 100 kHz, V_{IN}=1.1V, V_{OUT}= 5V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 47 µF || 10µF || 10µF		6.9		
T_{TSD}	Over-temperature Shutdown Threshold(5)	T_J rising		160		°C
		T_J falling from shutdown		140		°C

***Note1*:** BIAS supply is required when the V_{IN} supply is below 1.4V. Conversely, no BIAS supply is needed when the V_{IN} supply is higher than or equal to 1.4 V.

***Note2*:** $V_{OUT\ (TARGET)}$ is the calculated V_{OUT} target value from the output voltage setting pins: 50mV, 100mV, 200mV, 400mV, 800mV, and 1.6V in a fixed configuration. In an adjustable configuration, $V_{OUT\ (TARGET)}$ is the expected V_{OUT} value set by the external feedback resistors.

***Note3*:** When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.

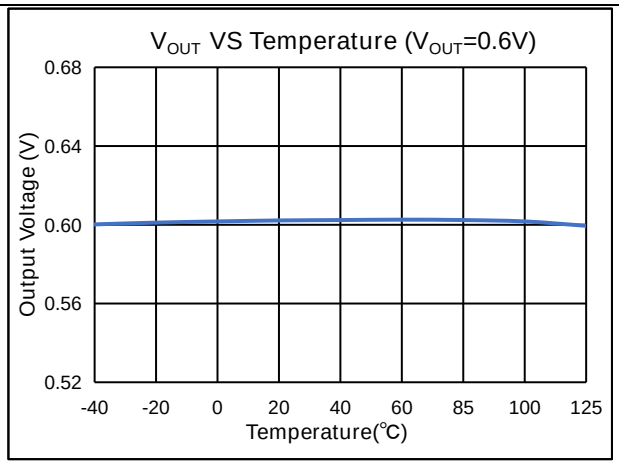
***Note4*:** The device is not tested under conditions where V_{IN}>V_{OUT}+2.5V and I_{OUT}=3A, because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package under test.

***Note5*:** Guaranteed by design and characterization. not a FT item.

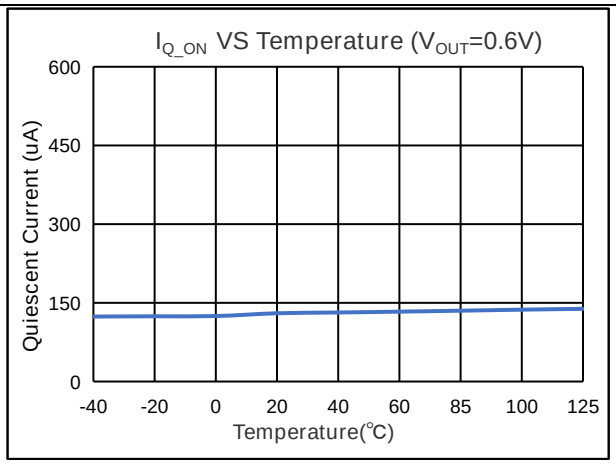
Typical Characteristics

VOLTAGE VERSION 0.6 V

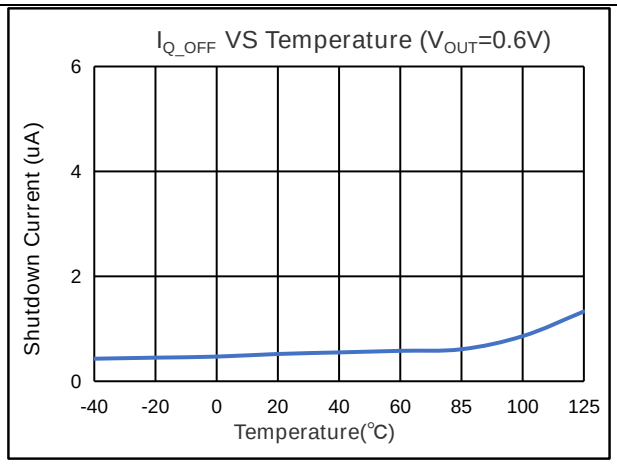
(V_{IN}=1.4V, V_{BIAS}=3.0V, I_{OUT}=1mA, V_{EN}=1.4V, C_{IN}= 47 μF || 10μF || 10μF, C_{OUT}= 47μF || 10μF || 10μF, $C_{NR/SS}$=10nF, C_{FF}=100nF, and PG pin pulled up to V_{IN} with 100kΩ, unless otherwise noted. Typical values are at T_A=25°C.)



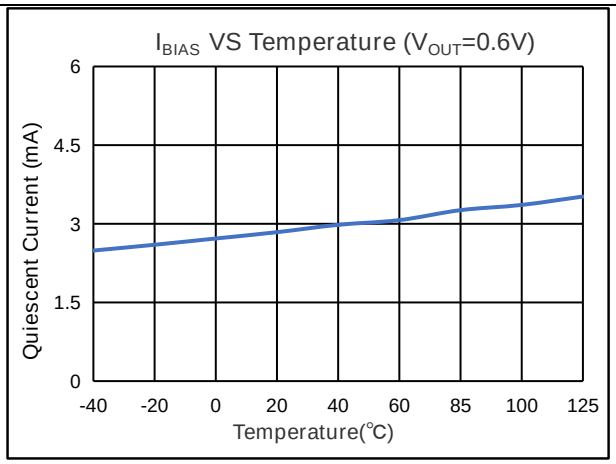
Output Voltage VS Temperature



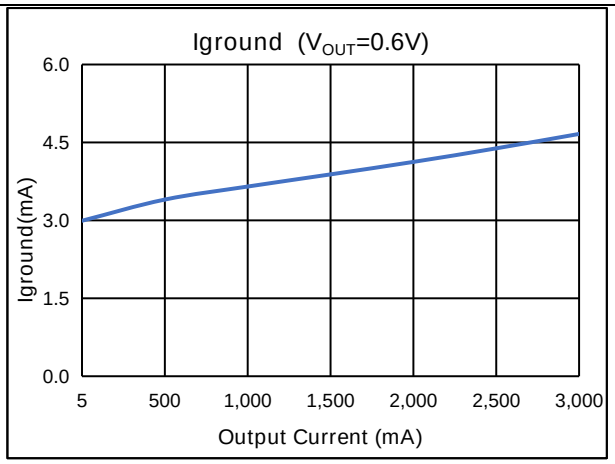
IN Supply Current VS Temperature



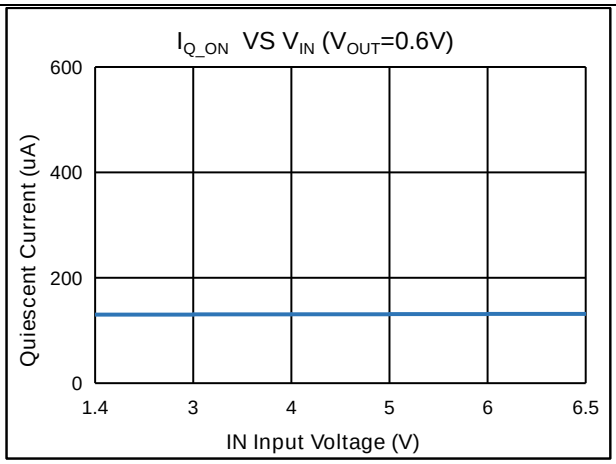
Shutdown Current VS Temperature



BIAS Supply Current VS Temperature



GND Current VS Output Current (V_{IN}=1.4V)

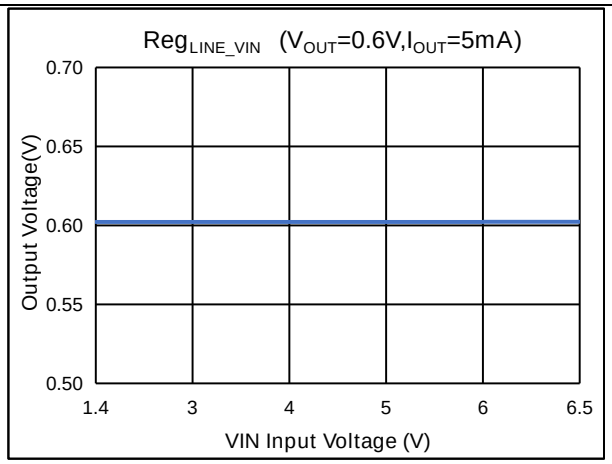


IN Supply Current VS V_{IN}

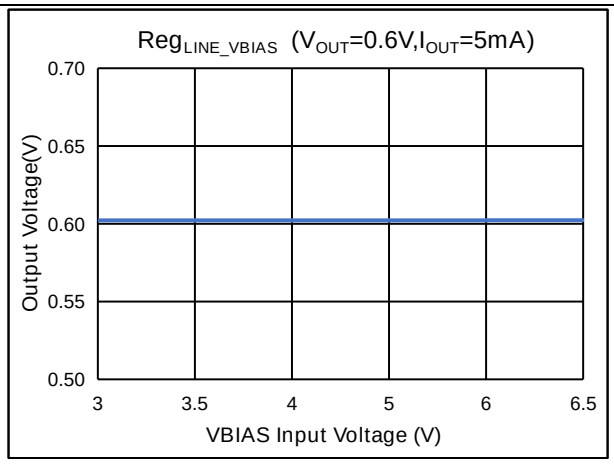
Typical Characteristics(Continue)

VOLTAGE VERSION 0.6 V

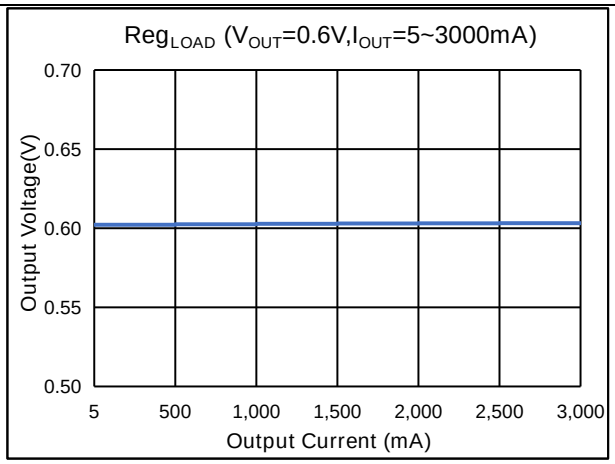
(V_{IN}=1.4V, V_{BIAS}=3.0V, I_{OUT}=1mA, V_{EN}=1.4V, C_{IN}= 47 μF || 10μF || 10μF, C_{OUT}= 47μF || 10μF || 10μF, $C_{NR/SS}$=10nF, C_{FF}=100nF, and PG pin pulled up to V_{IN} with 100kΩ, unless otherwise noted. Typical values are at T_A=25°C.)



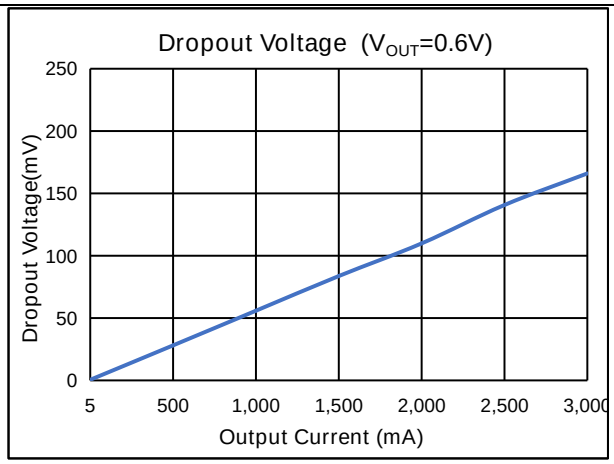
Output Voltage VS V_{IN} Voltage



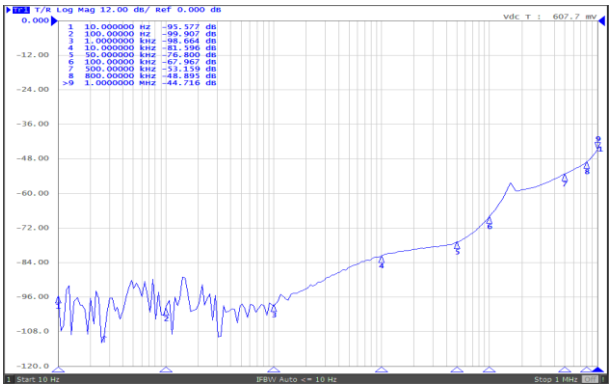
Output Voltage VS V_{BIAS} Voltage



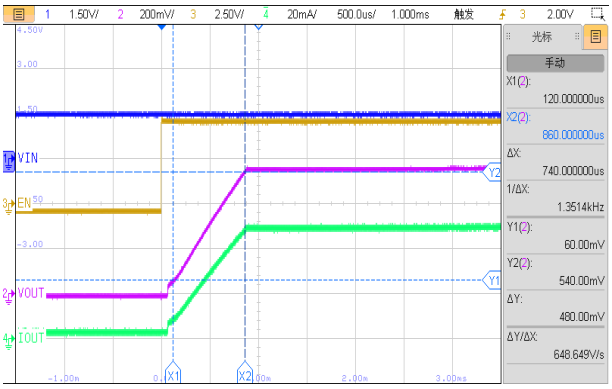
Output Voltage VS Output Current (V_{IN}=1.4V)



Drop Voltage VS Output Current



PSRR @20mA

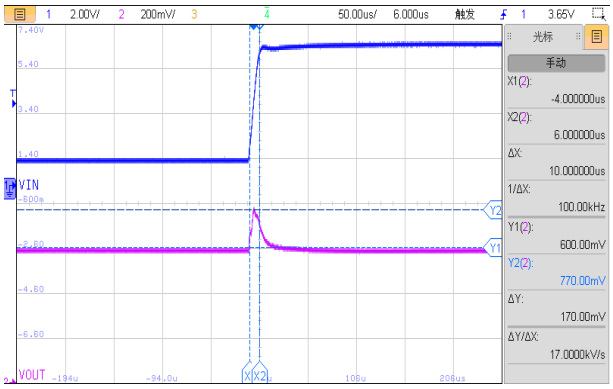


Turn On Speed VS EN Voltage (I_{OUT}=50mA)

Typical Characteristics(Continue)

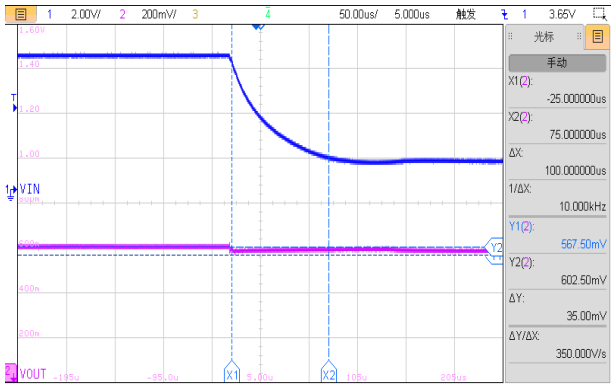
VOLTAGE VERSION 0.6 V

(V_{IN}=1.4V, V_{BIAS}=3.0V, I_{OUT}=1mA, V_{EN}=1.4V, C_{IN}= 47 μF || 10μF || 10μF, C_{OUT}= 47μF || 10μF || 10μF, $C_{NR/SS}$=10nF, C_{FF}=100nF, and PG pin pulled up to V_{IN} with 100kΩ, unless otherwise noted. Typical values are at T_A=25°C.)



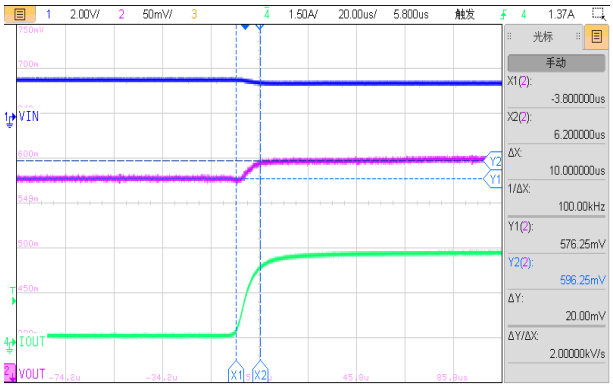
Line Transient Response

V_{IN}=1.4V~6.5V, V_{OUT}=0.6V, I_{OUT}=1mA



Line Transient Response

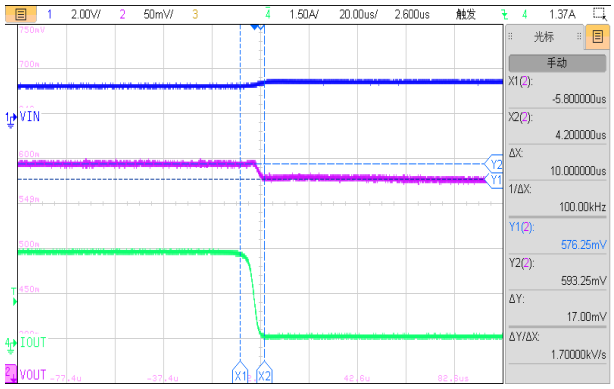
V_{IN}=6.5V~1.4V, V_{OUT}=0.6V, I_{OUT}=1mA



Load Transient Response

V_{IN}=1.4V, V_{BIAS}=3V, V_{OUT}=0.6V,

I_{OUT}=100mA~3000mA



Load Transient Response

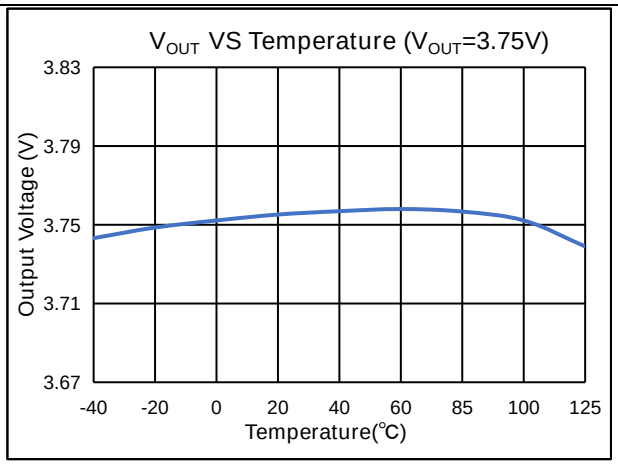
V_{IN}=1.4V, V_{BIAS}=3V, V_{OUT}=0.6V,

I_{OUT}=3000mA~100mA

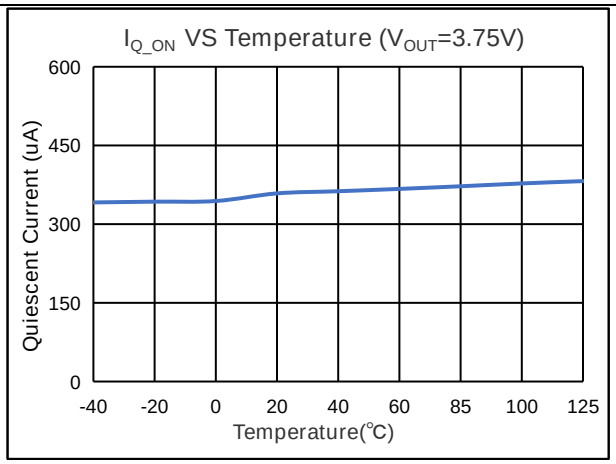
Typical Characteristics(Continue)

VOLTAGE VERSION 3.75 V

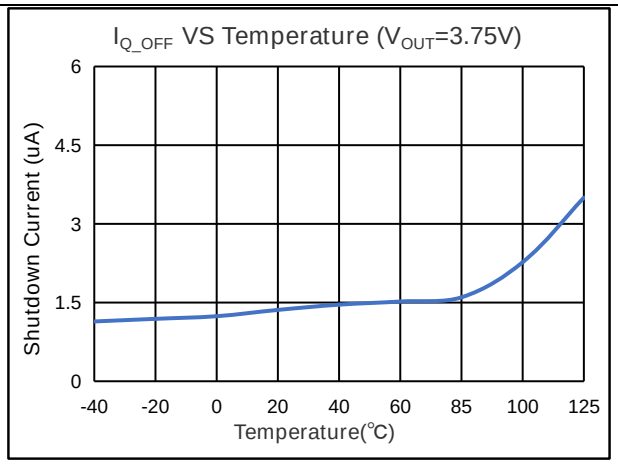
(V_{IN}=4.15V, no V_{BIAS}, I_{OUT}=1mA, V_{EN}=1.4V, C_{IN}= 47 μF || 10μF || 10μF, C_{OUT}= 47μF || 10μF || 10μF, $C_{NR/SS}$=10nF, C_{FF}=100nF, and PG pin pulled up to V_{IN} with 100kΩ, unless otherwise noted. Typical values are at T_A=25°C.)



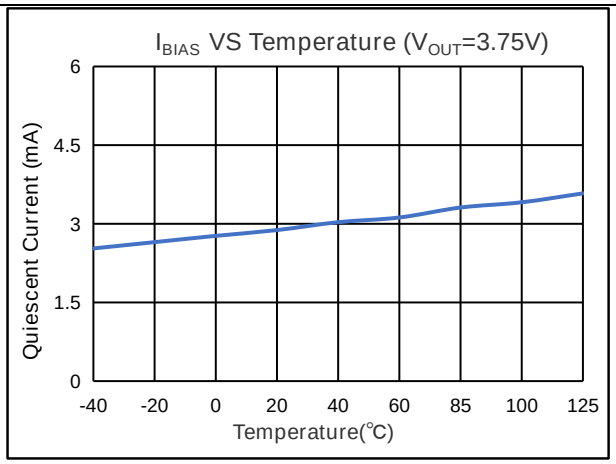
Output Voltage VS Temperature



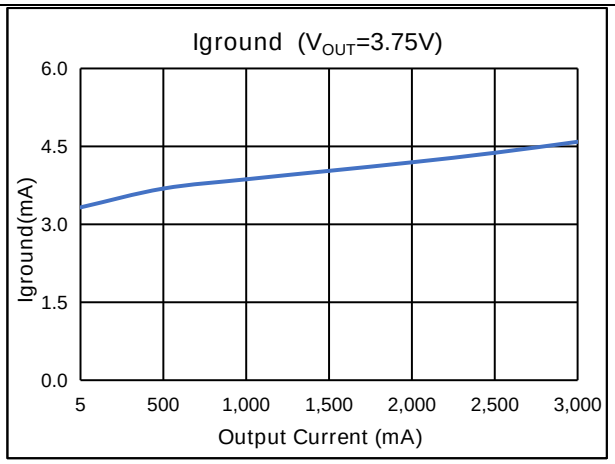
IN Supply Current VS Temperature



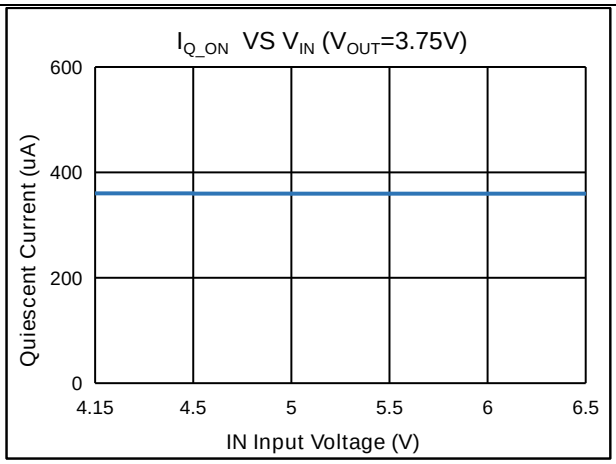
Shutdown Current VS Temperature



BIAS Supply Current VS Temperature



GND Current VS Output Current

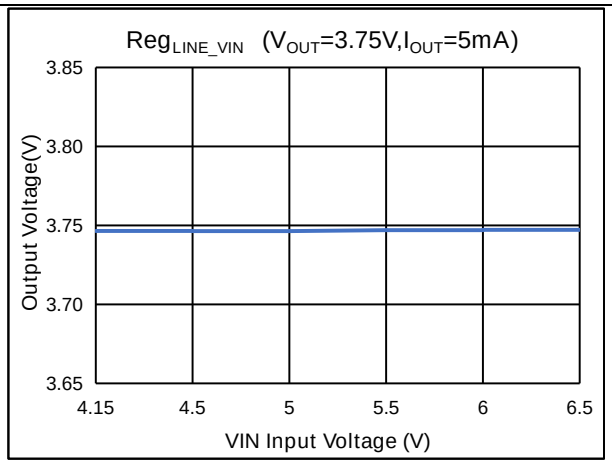


IN Supply Current VS V_{IN}

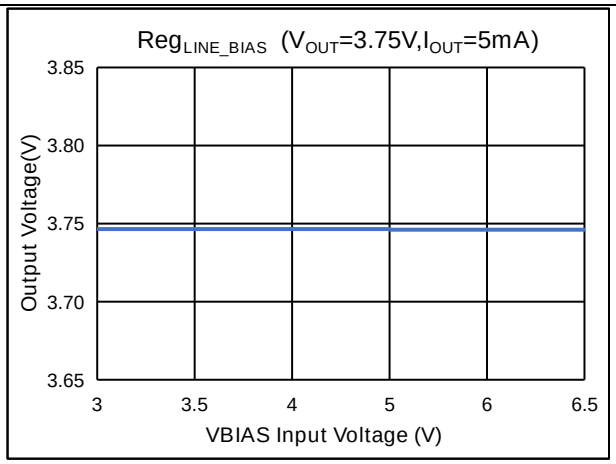
Typical Characteristics(Continue)

VOLTAGE VERSION 3.75 V

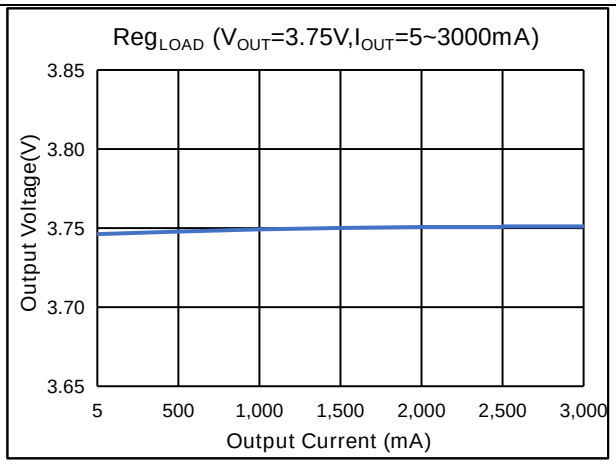
(V_{IN}=4.15V, no V_{BIAS}, I_{OUT}=1mA, V_{EN}=1.4V, C_{IN}= 47 μF || 10μF || 10μF, C_{OUT}= 47μF || 10μF || 10μF, $C_{NR/SS}$=10nF, C_{FF}=100nF, and PG pin pulled up to V_{IN} with 100kΩ, unless otherwise noted. Typical values are at T_A=25°C.)



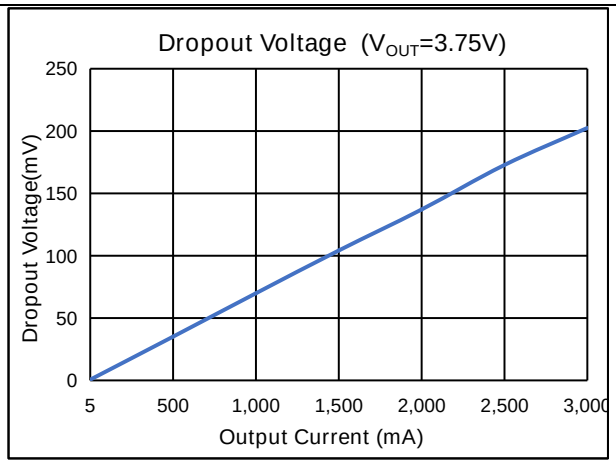
Output Voltage VS V_{IN} Voltage



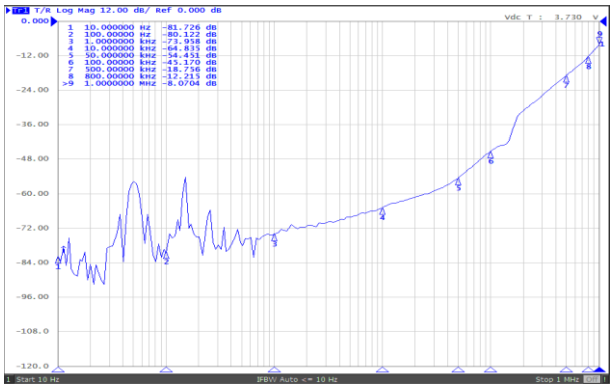
Output Voltage VS V_{BIAS} Voltage



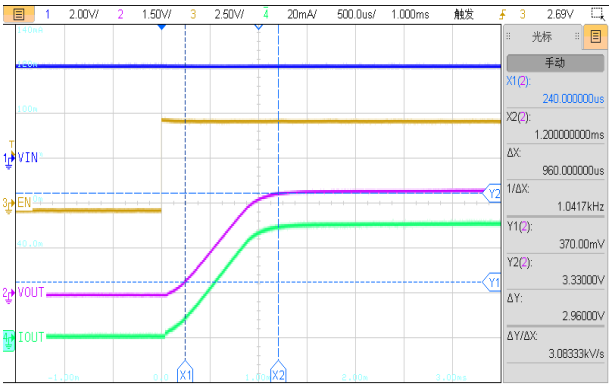
Output Voltage VS Output Current



Drop Voltage VS Output Current



PSRR @20mA

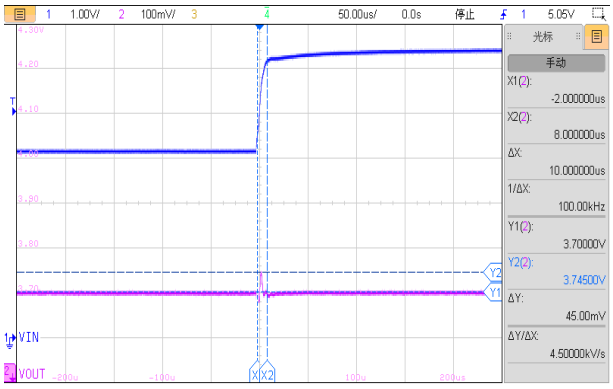


Turn On Speed VS EN Voltage (I_{OUT}=50mA)

Typical Characteristics(Continue)

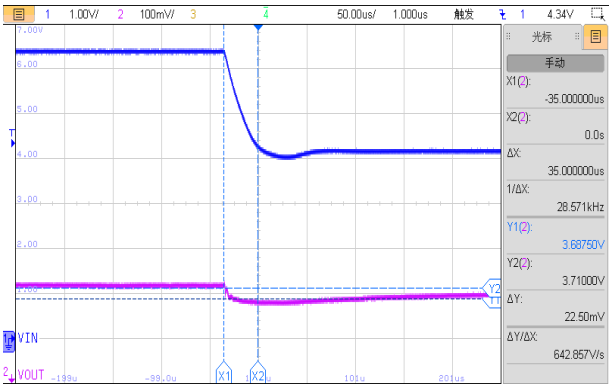
VOLTAGE VERSION 3.75 V

(V_{IN}=4.15V, no V_{BIAS}, I_{OUT}=1mA, V_{EN}=1.4V, C_{IN}= 47 μF || 10μF || 10μF, C_{OUT}= 47μF || 10μF || 10μF, $C_{NR/SS}$=10nF, C_{FF}=100nF, and PG pin pulled up to V_{IN} with 100kΩ, unless otherwise noted. Typical values are at T_A=25°C.)



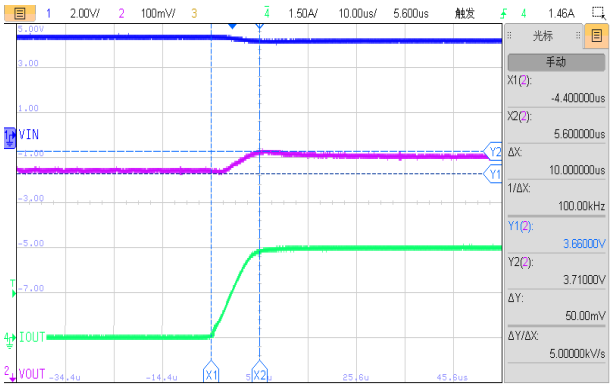
Line Transient Response

V_{IN}=4.15V~6.5V, V_{OUT}=3.75V, I_{OUT}=1mA



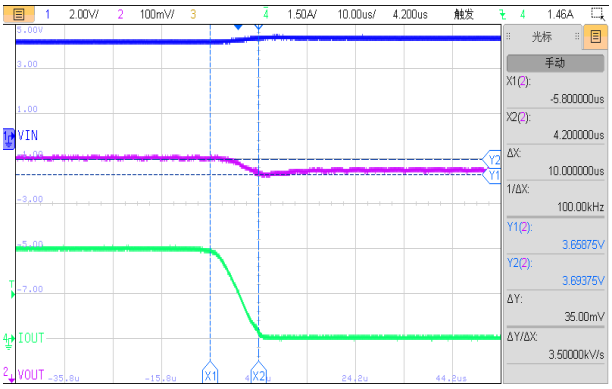
Line Transient Response

V_{IN}=6.5V~4.15V, V_{OUT}=3.75V, I_{OUT}=1mA



Load Transient Response

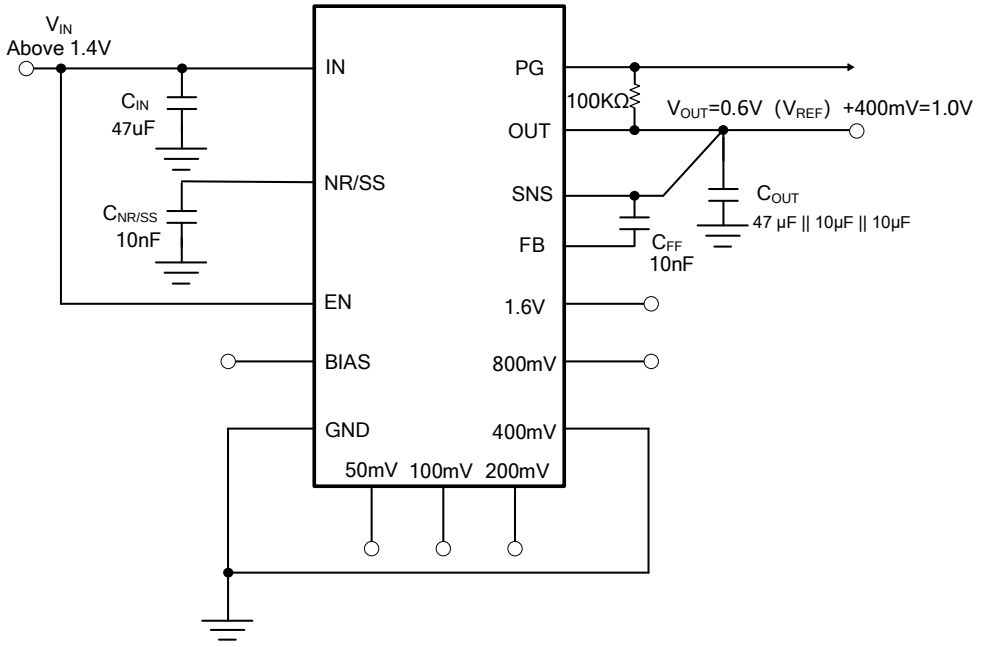
V_{IN}=4.15V, V_{OUT}=3.75V, I_{OUT}=100mA~3000mA



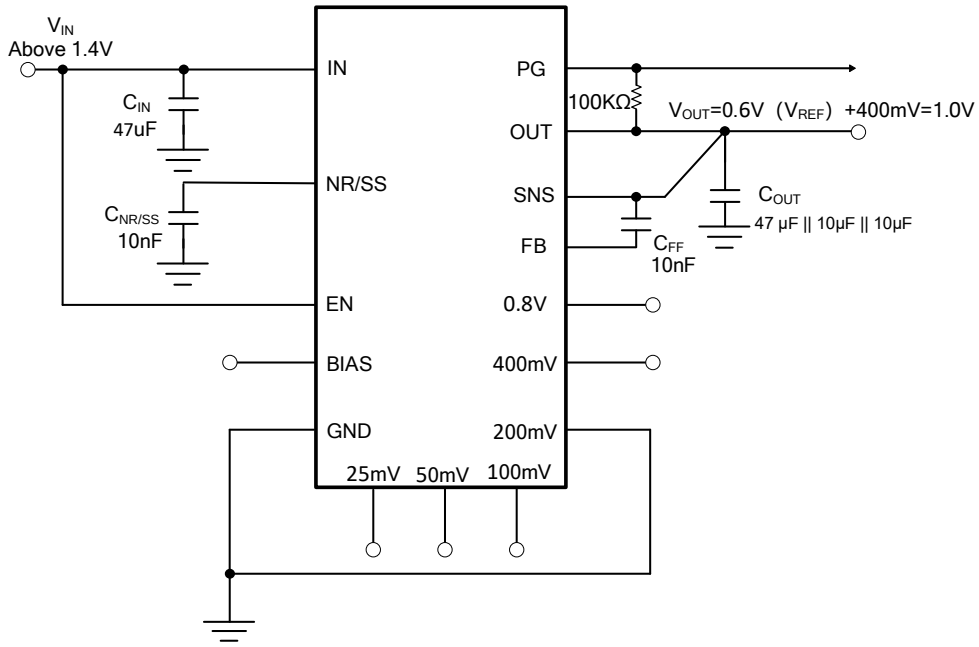
Load Transient Response

V_{IN}=4.15V, V_{OUT}=3.75V, I_{OUT}=3000mA~100mA

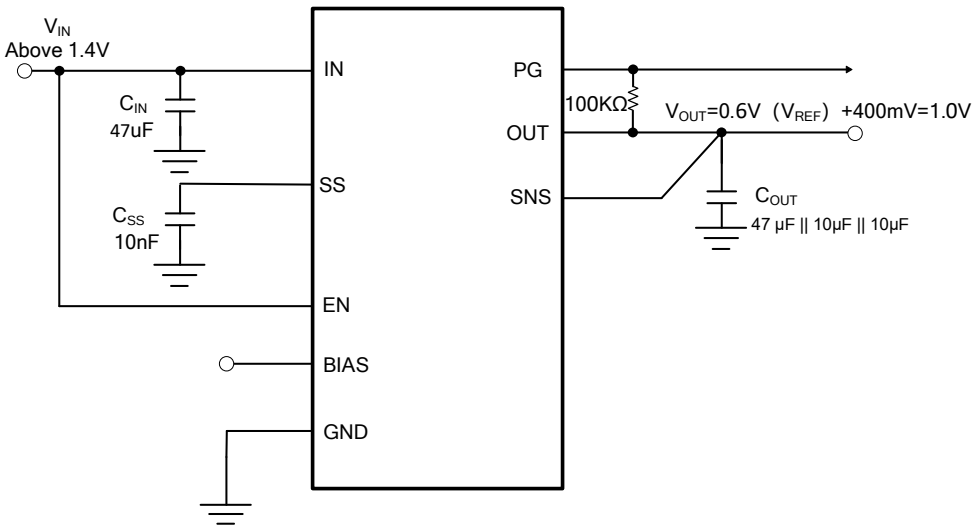
Application Circuits



ET5CS01X

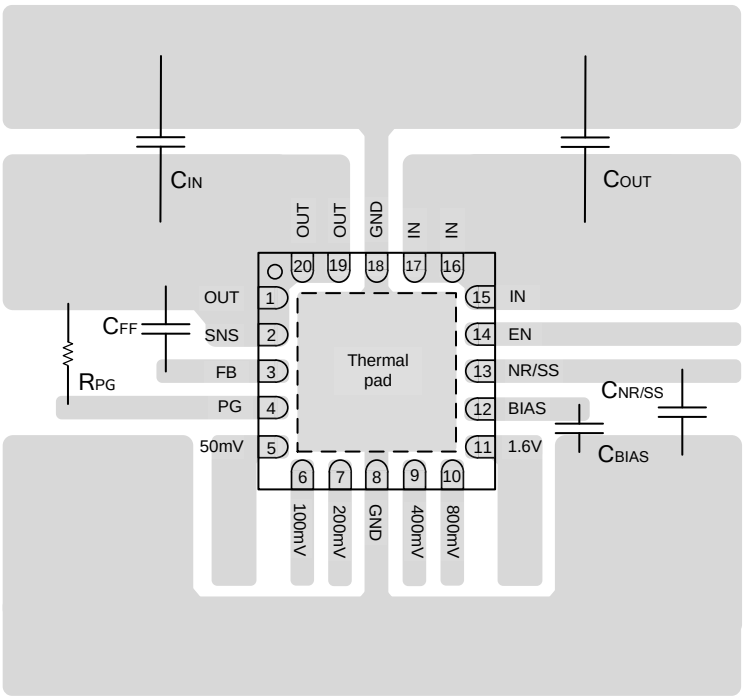


ET5CS02X


V_{IN}
Above 1.4V
C_{IN}
47uF
C_{SS}
10nF
IN
SS
EN
BIAS
GND
PG
OUT
SNS
100KΩ
V_{OUT}=0.6V (V_{REF}) +400mV=1.0V
C_{OUT}
47 µF || 10µF || 10µF

ET5CS03X

PCB Layout Guide



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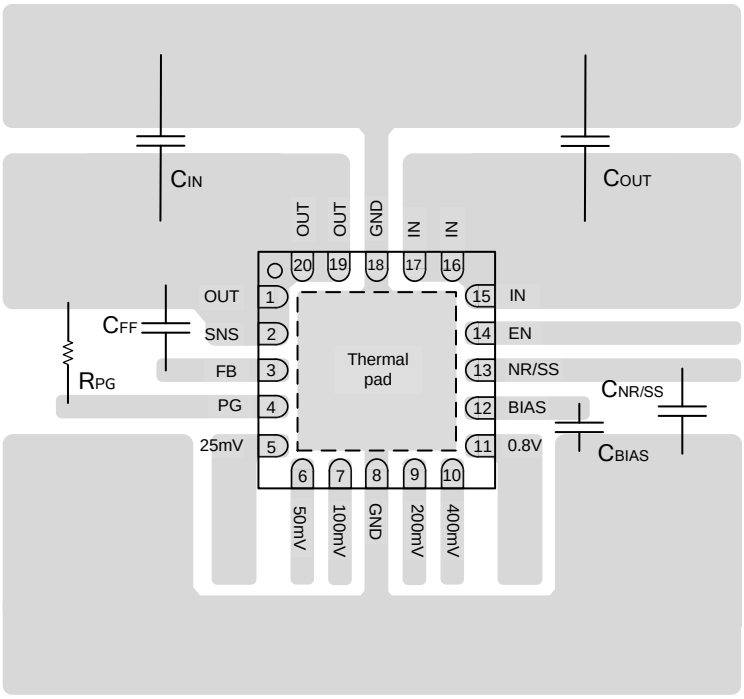
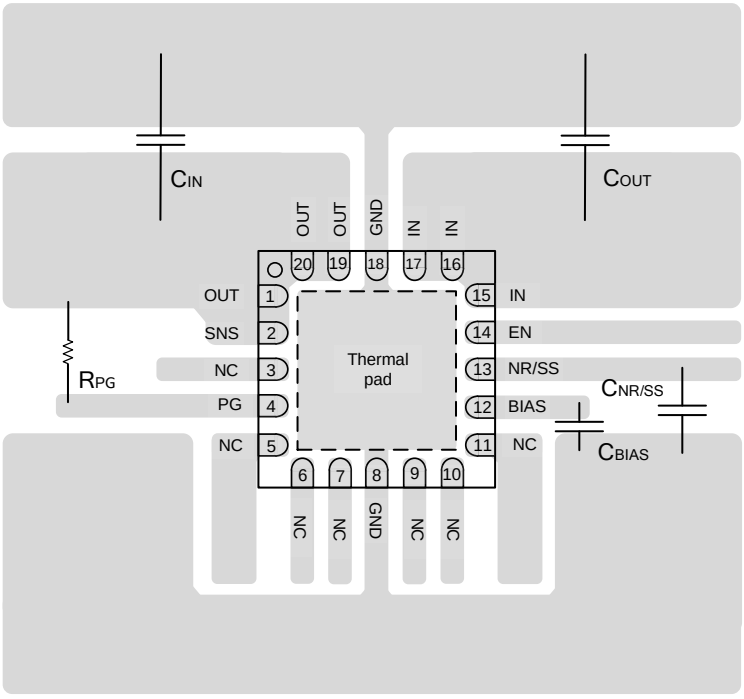


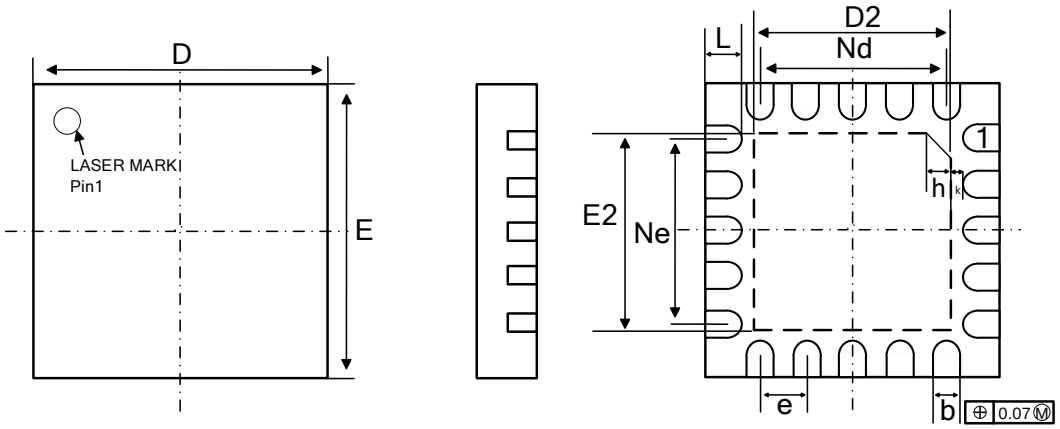
ET5CS02X


CIN
COUT
OUT
OUT
GND
IN
IN
20
19
18
17
16
OUT 1
SNS 2
NC 3
PG 4
NC 5
15 IN
14 EN
13 NR/SS
12 BIAS
11 NC
Thermal pad
RPG
CNR/SS
CBIAS
6
7
8
9
10
NC
NC
GND
NC
NC

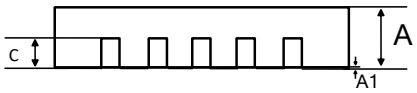
ET5CS03X

Package Dimension

QFN20-3.5mm*3.5mm



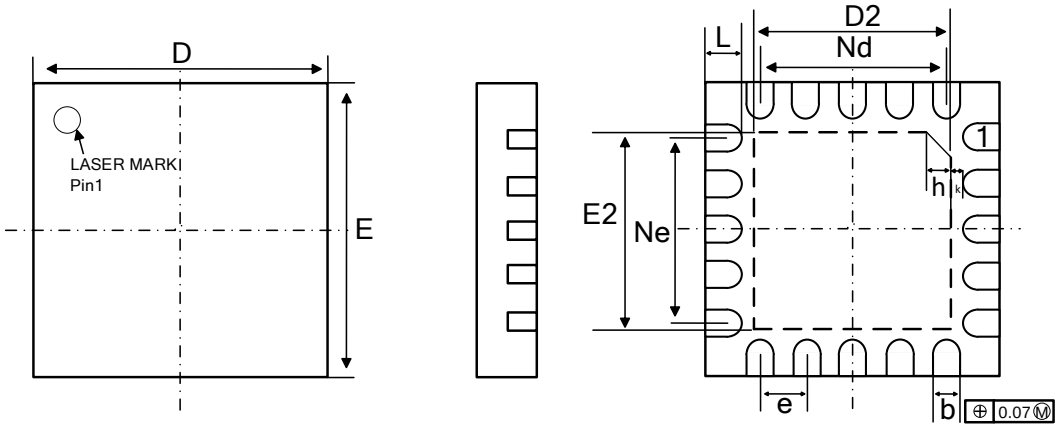
Top View Side View Bottom View



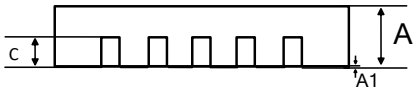
Side View

QFN20-3.5mm*3.5mm			
Symbol	**Unit: mm**		
	Min	**Nom**	**Max**
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.18	0.23	0.30
c	0.203 REF		
D	3.40	3.50	3.60
D2	1.95	2.05	2.15
E	3.40	3.50	3.60
E2	1.95	2.05	2.15
e	0.5 BSC		
Ne	2.00 BSC		
Nd	2.00 BSC		
L	0.35	0.40	0.45
k	0.275	0.325	0.375
h	0.25	0.30	0.35

QFN20-5.0mm*5.0mm



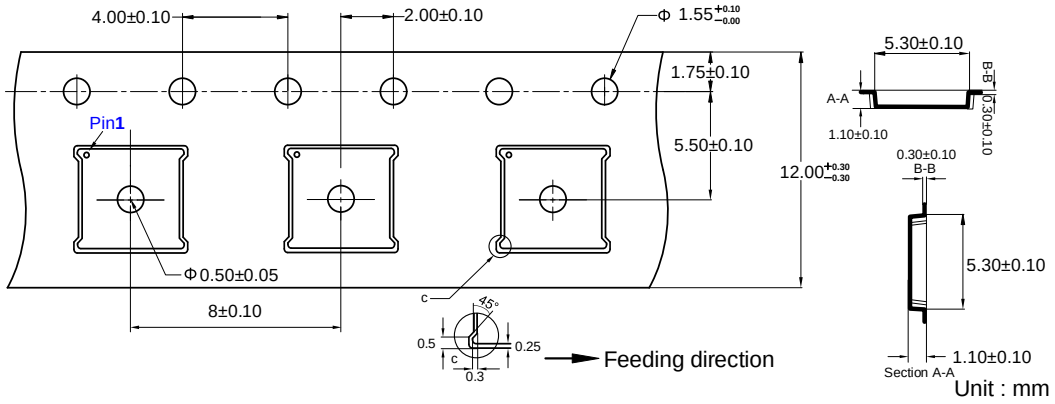
Top View Side View Bottom View



Side View

QFN20-5.0mm*5.0mm			
Symbol	**Unit: mm**		
	Min	**Nom**	**Max**
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.25	0.30	0.35
c		0.203 REF	
D	4.90	5.00	5.10
D2	3.05	3.15	3.25
E	4.90	5.00	5.10
E2	3.05	3.15	3.25
e		0.65 BSC	
Ne		2.60 BSC	
Nd		2.60 BSC	
L	0.45	0.55	0.65
k	0.275	0.325	0.375
h	0.30	0.35	0.40

Tape Information



QFN20 (5mm×5mm)

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025-07-01	Original Version	Pengjj	Yangxx	Liujy