# 4 Channel LDO PMIC with I²C Control

## General Description

The ET5924A is CMOS-based low dropout, low power linear regulator. It's a 4-channels integrated LDO with I²C control. LDO1 offer up to 1500mA with NMOS pass transistor, LDO2 offer up to 1200mA with NMOS pass transistor, LDO3/4 offer up to 400mA with PMOS pass transistor. ET5924A include 1MHz high speed I²C interface, the function setting is flexible such as power sequence, output voltage, output discharge, current limit per channel. The chip enable control support EN pin control and I²C control.

The ET5924A is available in DFN10(2×2) package.

## Features

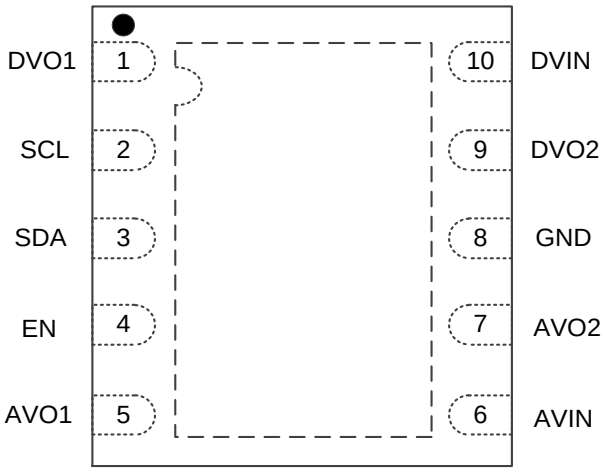
- DVIN input voltage range from 0.6V to 2.2V
- AVIN input voltage range from 2.5V to 5.5V
- LDO1/2 output voltage range from 0.6V to 1.8V with step 6mV
- LDO1 output current are up to 1500mA
- LDO2 output current are up to 1200mA
- LDO1 ultra-low dropout are typical 150mV at 1500mA, 1.2V output
- LDO2 ultra-low dropout are typical 160mV at 1200mA, 1.2V output
- LDO3/4 output voltage range from 1.2V to 4.3V with step 12.5mV
- LDO3/4 output current range are 400mA
- LDO3/4 ultra-low dropout are typical 120mV at 400mA, 2.8V output
- LDO3/4 built-in inrush current limit at typical 250mA for appr.700us period after start-up
- Very low input quiescent current of 85μA typical
- Built-in over-current protection and thermal shutdown circuit
- Built-in auto-discharging circuit (optional)
- Built-in under voltage lock-out
- Part No. and Package

| Part No. | Package | MSL |
|---|---|---|
| ET5924A | DFN10 (2mm × 2mm) | 1 |

## Applications

- Constant-Voltage Power Supply for Battery-powered Device
- Constant-Voltage Power Supply for Smartphones, Tablets
- Constant-Voltage Power Supply for Cameras, DVRs, STB and Camcorders

## Pin Configuration

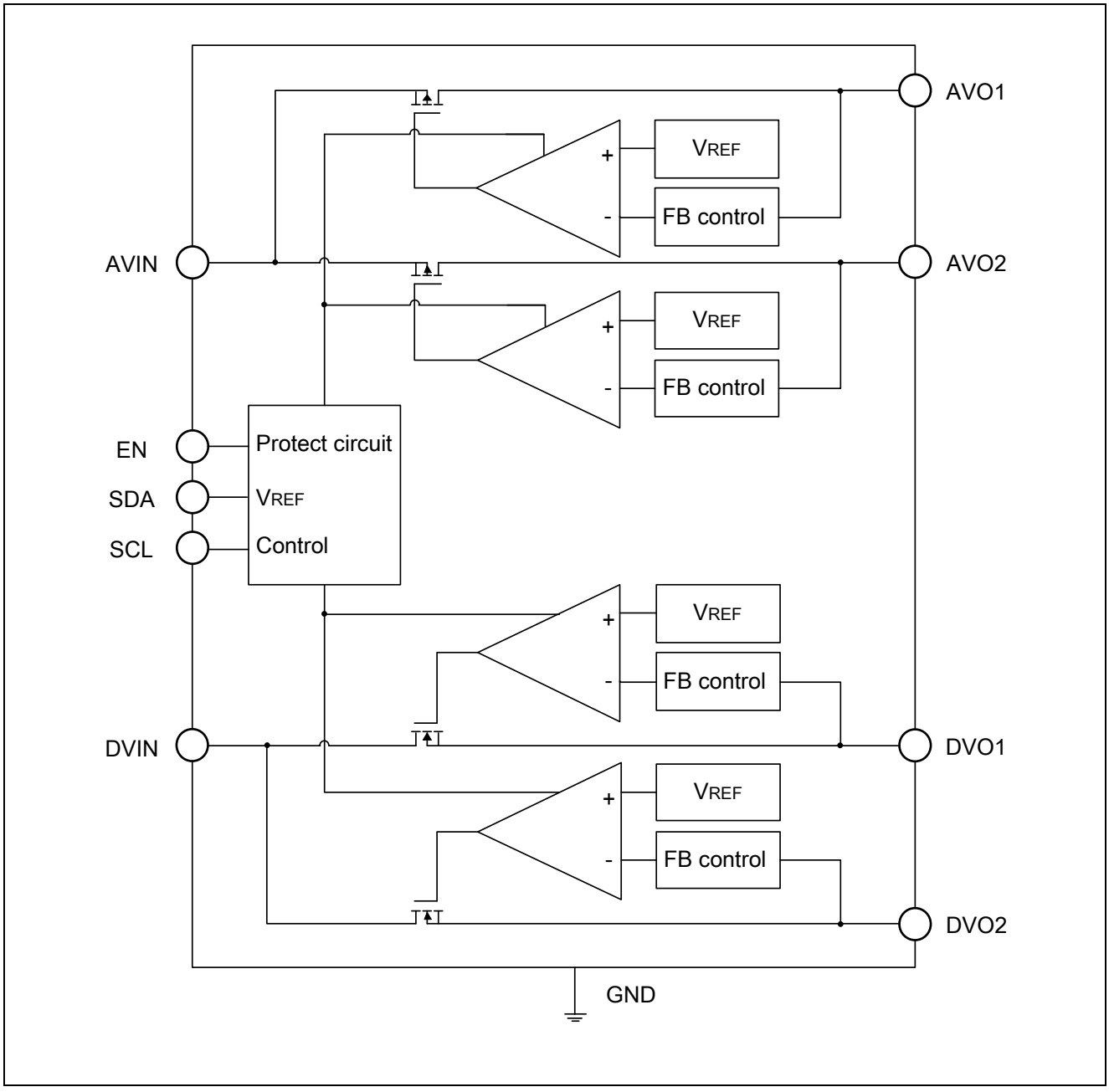



Top view

## Pin Function

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1 | DVO1 | LDO1 regulate output |
| 2 | SCL | $I^2C$ interface Clock |
| 3 | SDA | $I^2C$ interface Data |
| 4 | EN | Global enable control, active high.<br>Maintain to low with 0.3uA pull down current source |
| 5 | AVO1 | LDO3 regulator output |
| 6 | AVIN | LDO3~4 supply input and LDO1~2 bias input |
| 7 | AVO2 | LDO4 regulator output |
| 8 | GND | Ground |
| 9 | DVO2 | LDO2 regulator output |
| 10 | DVIN | LDO1~2 supply input |

## Block Diagram




## Functional Description

### Power Up and Power Down Control

ET5924A has 4 LDO regulators. LDO1/2 are using NMOS pass transistor for output voltage regulation from DVIN. LDO3/4 are using PMOS pass transistor for output voltage regulation from AVIN. The ET5924A offers smooth start-up. Power up/down of each regulator can be controlled by the following three ways. It can be set at the registers LDOx_SEQ[3:0] (x=1 to 4) respectively.

**1.** External EN pin control.

External EN pin toggles from low to high when EN_SEL=0(bit6 in LDO_EN register) by I²C, it will force all 4 LDO regulators powered up, output voltage of each LDO is default voltage. LDO1/2 output default voltage 1.2V, LDO3/4 output default voltage 2.8V. When external EN pin is low, LDO output can be controlled by I²C register(LDO1_VSET~ LDO4_VSET).

External EN pin toggles from low to high when EN_SEL=1(bit6 in LDO_EN register) by I²C, then LDO output can be controlled by I²C register. When external EN pin is low, it will force all 4 LDO regulators powered down.

**2.** Individual on/off control.

Power-up and shut down of each regulator can be controlled by an I²C register. LDOx_EN is an internal signal to enable one of regulators, If LDOx_SEQ[3:0] set to '0000', that LDOx channel can be controlled directly by a bit specified in register LDOx_EN[3:0]. LDOx_VSET[3:0] can set output voltage of each channel.

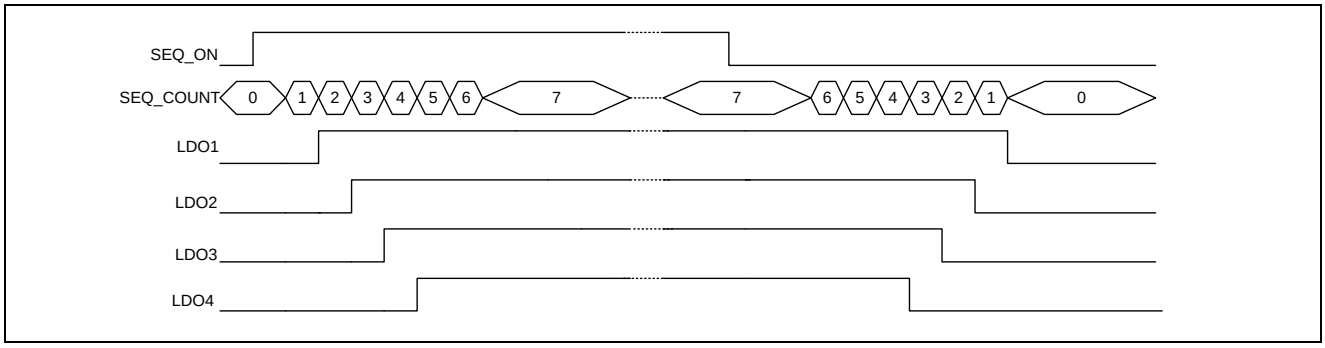
**3.** Automatic power up/down sequence control.

ET5924A has 7 SLOTs to which each regulator can be assigned.

They are started by SEQ_ON signal. when SEQ_ON is high. Internal counter SEQ_COUNT [2:0] starts increments from 0 ("000") to 7 ("111"). When SEQ_ON is low, SEQ_COUNT [2:0] decrements from 7 ("111") to 0 ("000"). Regulators assigned to one of SLOTs starts power-up or power-down.

When SEQ_COUNT [2:0] matches the SLOT number.

Internal logic signal SEQ_ON is asserted by I²C, write '00' to SEQ_CTRL [1:0] will set SEQ_ON to '0', while write '01' to SEQ_CTRL[1:0] will set SEQ_ON to '1'.




* Example of Power-up in the case of LDO1/2/3/4 are assigned to SLOT1/2/3/4 respectively

* Example of Shutdown in the case of LDO1/2/3/4 are assigned to SLOT1/2/3/4 respectively.

**Input and Output Capacitor**

The LDO1/2 are designed to be stable for ceramic output capacitors with Effective capacitance in the range from 3.3μF to 47μF. The LDO3~LDO4 are designed to be stable for ceramic output capacitors with Effective capacitance in the range from 0.47μF to 10μF. The recommended $C_{DVO1/2}$ =4.7μF and $C_{AVO3/4}$= 1μF.

The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range. In applications where no low input supplies impedance available (PCB inductance in DVIN and/or AVIN inputs as example), the recommended $C_{AVIN}$ =4.7μF and $C_{DVIN}$= 4.7μF or greater.

### Current Limit Protection

For each channel, when output current of LDO output pin is higher than current limit threshold or the output pin is direct short to GND, the current limit protection will be triggered and clamp the output current at a predesigned level to prevent over-current and thermal damage. Set related bits to select Current limit threshold register.

### Thermal Shutdown Protection

Thermal protection disables all the output when the junction temperature rises to approximately +150°C, allowing the device to cool down. When the junction temperature reduces to approximately +120°C all the output circuit is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

### Auto Discharging

For each channel, when shut down the output, the Auto-discharging circuit will be turned on to discharge the electric charge on output capacitor, and decrease the voltage of output pin in very short time.

The Auto-discharging function is optional. Set related bits to select output discharge function for discharge resistor (RDIS Register) : “0” is Disable. “1” is Enable.

***Note :*** When use the discharge function by register control , should set Bit7 =1 .
When set Bit7 =”0”, EN=”0”, discharge resistor selection[3:0]=0x00, discharge function enable.
When set Bit7 =”1”, EN=”0”, discharge resistor selection[3:0]=0x00, discharge function disable.

### Serial Port Interface ($I^2C$)

- **Bus Interface**

Baseband Processor can transmit data with ET5924A each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected.

- **Data Validity**

When the SCL signal is high, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

- **Start (Re-start) and Stop Working Conditions**

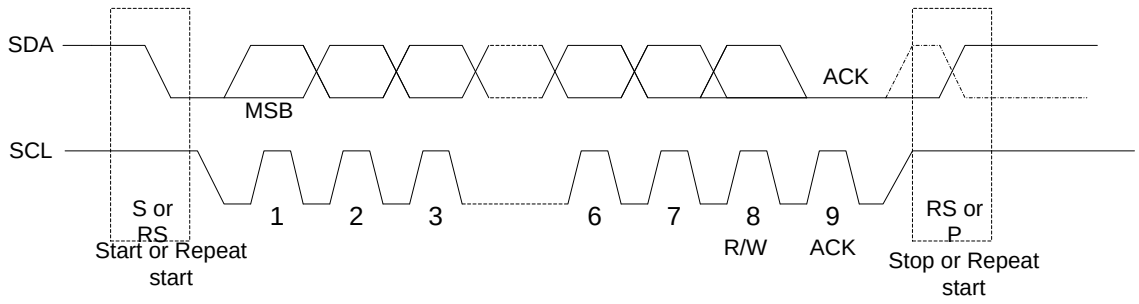
When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

- **Byte format**

Each byte of data line contains 8 bits, which contains an acknowledge bit. The first data is transmitted MSB.

- **Acknowledge**

During the writing mode, ET5924A will send a low level response signal with one period width to the SDA port. During the reading mode, ET5924A will not send response signal and the host will send a high response signal one period width to the SDA.



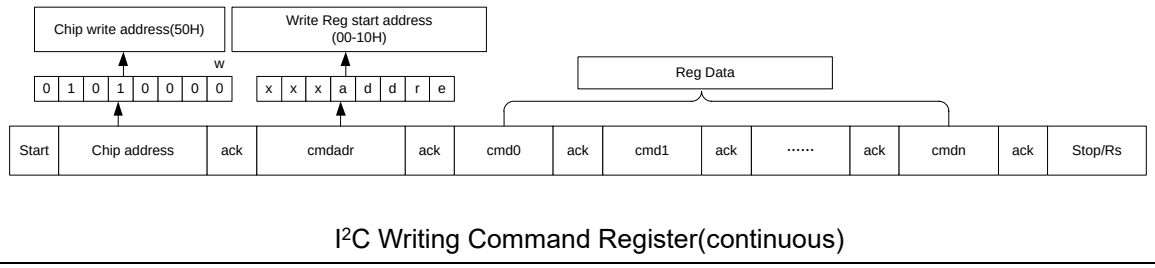

I²C write mode

- ACK=Acknowledge
- MSB=Most Significant Bit
- S=Start Conditions RS=Restart Conditions P=Stop Conditions
- Fastest Transmission Speed =400kHz
- Restart: SDA-level turnover as expressed by the dashed line waveform

- **Chip Address**

Chip address is 01010000(Writing Register mode)/01010001(Reading Register Mode)

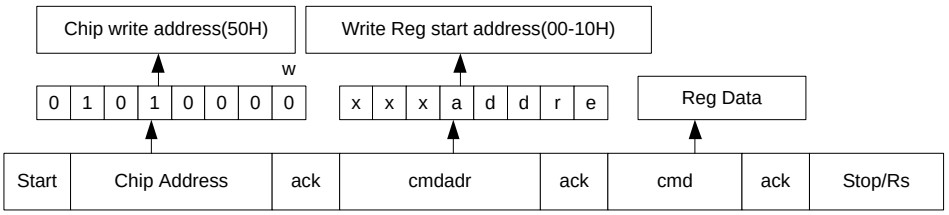
- **I²C Writing Command Register Interface Protocol (continuous):**




I²C Writing Command Register(continuous)

- Start=Start Conditions
- Chip address=Write register address =0101000+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr(xxx + REG's 5bit addr)
- ack=Acknowledge
- Reg data 0 = cmd0(Command data0)
- ack=Acknowledge
- ……
- Reg data n =cmdn(Command datan)
- ack=Acknowledge
- Stop/Rs=Stop Condition/Restart Condition

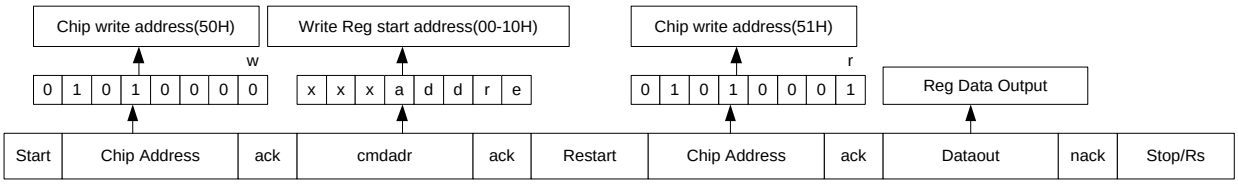
- **I²C Writing Command Register Interface Protocol (single):**




I²C Writing Command Register(single)

- Start=Start Conditions
- Chip address =Write register address=0101000+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr (xxx + REG's 5bit addr)
- ack=Acknowledge
- Reg data= cmd(Command data)
- ack=Acknowledge
- Stop/Rs=Stop Condition/Restart Condition

- **I²C Reading Command Register Interface Protocol(continuous)**




I²C Reading Command Register

- Start=Start Conditions
- Chip address =Write register address=0101000+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr(xxx + REG's 5bit addr)
- ack=Acknowledge
- Restart=Restart condition
- Chip address Read register address=0101000+1(r)b
- ack=Acknowledge
- Dataout=Register data output
- nack=No Acknowledge
- Stop/Rs=Stop Condition/Restart Condition

**Register Map**

| Addr | Name | Type | Rst | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | CHIPID | R/W | 0x0A | Chip_ID[7:0] | | | | | | | |
| 0x01 | ILIMIT | R/W | 0x00 | LDO2_ILA | LDO2_ILS | LDO1_ILA | LDO1_ILS | LDO3/4_IL [1:0] | | LDO1/2_IL [1:0] | |
| 0x02 | RDIS | R/W | 0x00 | RDIS_EN | Rev. | | | Discharge Resistor Selection [3:0] | | | |
| 0x03 | DVO1 | R/W | 0x64 | LDO1_VSET [7:0] | | | | | | | |
| 0x04 | DVO2 | R/W | 0x64 | LDO2_VSET [7:0] | | | | | | | |
| 0x05 | AVO1 | R/W | 0x80 | LDO3_VSET [7:0] | | | | | | | |
| 0x06 | AVO2 | R/W | 0x80 | LDO4_VSET [7:0] | | | | | | | |
| 0x0A | SEQ1 | R/W | 0x00 | LDO2_SEQ [3:0] | | | | LDO1_SEQ [3:0] | | | |
| 0x0B | SEQ2 | R/W | 0x00 | LDO4_SEQ [3:0] | | | | LDO3_SEQ [3:0] | | | |
| 0x0E | LDO_EN | R/W | 0x00 | REG_RST | EN_SEL | Rev. | | LDOx_EN [3:0] | | | |
| 0x0F | SEQ_C | R/W | 0x00 | SEQ_SPEED [1:0] | | SEQ_CTRL [1:0] | | SEQ_ ON | SEQ_COUNT [2:0] | | |
| 0x10 | ILIMT_ COAR | R/W | 0x00 | LDO4_COA_IL[1:0] | | LDO3_COA_IL[1:0] | | LDO2_COA_IL[1:0] | | LDO1_COA_IL[1:0] | |

***Note:*** Rev.—Reserve, keep “0”.

- **0x00 CHIPID Register---- Indicates the device ID.**

  Chip_ID[7:0] Indicates the device ID(0x0A for ET5924A). Read only

- **0x01 ILIMIT Register ----LDO Current Limit Selection**

  Defined the typical value of current limit threshold value for LDOs.
  The detail current limit value are shown in the table as below:
  LDO1/2 Current Limit is overall increase or decrease:

| LDO1_ILA | LDO1_ILS | Action |
|---|---|---|
| 0(default) | 0(default) | NA. |
| 0 | 1 | LDO1 Current Limit is overall decrease about 25% |
| 1 | 0 | LDO1 Current Limit is overall increase about 25% |
| 1 | 1 | NA. |

| LDO2_ILA | LDO2_ILS | Action |
|---|---|---|
| 0(default) | 0(default) | NA. |
| 0 | 1 | LDO2 Current Limit is overall decrease about 25% |
| 1 | 0 | LDO2 Current Limit is overall increase about 25% |
| 1 | 1 | NA. |

LDO1/2 Current Limit fine tuning Table 1:

| LDO12_IL[1:0] | LDO1 Current Limit(mA) | LDO2 Current Limit(mA) |
|---|---|---|
| 00(default) | 2100 | 1500 |
| 01 | 2000 | 1400 |
| 10 | 2200 | 1600 |
| 11 | 2300 | 1700 |

LDO1/2 Current Limit coarse tuning Table 2:

| LDO1/2_COA_IL[1:0] | 00(default) | 01 | 10 | 11 |
|---|---|---|---|---|
| LDO1/2 ilimit | Current Limit*100% | Current Limit *85% | Current Limit *130% | Current Limit *115% |

LDO3/4 Current Limit fine tuning Table 3:

| LDO34_IL[1:0] | Current Limit(mA) | Short Current Limit(mA) |
|---|---|---|
| 00(default) | 680 | 50 |
| 01 | 580 | 43 |
| 10 | 850 | 64 |
| 11 | 670 | 57 |

LDO3/4 Current Limit coarse tuning Table 4:

| LDO3/4_COA_IL[1:0] | 00(default) | 01 | 10 | 11 |
|---|---|---|---|---|
| LDO3/4 ilimit | Current Limit*100% | Current Limit *60% | Current Limit *170% | Current Limit *135% |

***Note:*** The current limit values are design guaranteed, and the default current limit is tested by FT.

- **0x02 RDIS Register ----Discharge Resistor Selection**

Each LDO regulators output discharge resistor enable control.
Bit0 for LDO1, Bit1 for LDO2, Bit2 for LDO3, Bit3 for LDO4
1=Enable, 0=Disable.

***Note:***

(1) When use the Discharge Function by Register Control, should set Bit7 =”1”.
When set Bit7 =”1”, EN=”0”, Discharge Resistor Selection[3:0]=0x0, All LDOs Discharge Function Disable.
When set Bit7 =”1”, EN=”0”, Discharge Resistor Selection[3:0]=0xF, All LDOs Discharge Function Enable.

(2) When use the Discharge Function by EN port Control, should set Bit7 =”0”.
When set Bit7 =”0”, EN=”0”, all LDOs discharge Function Enable.
When set Bit7 =”0”, EN=”1”, all LDOs discharge Function disable.

- **0x03 DVO1 Register ---- DVO1 output voltage setting register**
- **0x04 DVO2 Register ---- DVO2 output voltage setting register**

The register LDO1/2_VSET [7:0] set the voltage of DVO1/ DVO2, it have 256 steps, shown as below table, the formula is VDVO =0.6V+ LDO1/2_VSET *0.006V.

| DVO1/DVO2 Output Voltage set by LDO1/2_VSET [7:0] | | |
|---|---|---|
| **Dec** | **Binary** | **Output Voltage(V)** |
| 0 | 00000000 | 0.600 |
| 1 | 00000001 | 0.606 |
| 2 | 00000010 | 0.612 |
| 3 | 00000011 | 0.618 |

| | | |
|---|---|---|
| 4 | 00000100 | 0.624 |
| 5 | 00000101 | 0.630 |
| …… | …… | …… |
| **100** | **01100100(default)** | **1.200** |
| 101 | 01100101 | 1.206 |
| 102 | 01100110 | 1.212 |
| ~255 | …… | …… |

- **0x05~0x06 AVO1~2 Register ---- AVO1~2output voltage setting register**

The registers LDO3/4_VSET [7:0] set the voltage of AVO1/AVO2, each voltage have 256 steps, shown as below table, the formula is VAVO1~AVO2=1.2V+ LDO3/4_VSET [7:0] *0.0125V.

| **AVO1~2 Output Voltage set by LDO3/4_VSET [7:0]** | | |
|---|---|---|
| **Dec** | **Binary** | **Output Voltage(V)** |
| 0 | 00000000 | 1.2000 |
| 1 | 00000001 | 1.2125 |
| 2 | 00000010 | 1.2250 |
| 3 | 00000011 | 1.2375 |
| 4 | 00000100 | 1.2500 |
| 5 | 00000101 | 1.2625 |
| …… | …… | …… |
| **128** | **10000000(default)** | **2.8000** |
| 129 | 10000001 | 2.8125 |
| 130 | 10000010 | 2.8250 |
| …… | …… | …… |
| 250 | 11111010 | 4.3250 |
| 251 | 11111011 | 4.3375 |
| 252 | 11111100 | 4.3500 |
| 253 | 11111101 | 4.3625 |
| 254 | 11111110 | 4.3750 |
| 255 | 11111111 | 4.3875 |

- **0x0A~0x0B SEQ1~2 Register ---- Power sequence setting register**

Power sequence setting register. there are 4 time slots defined as following table. The power-up sequence is start from slot1 to slot7 and shut down start from slo7 to slot1. Power-up and shut down of each LDO regulator can be set at any one of the slots.

| **Register Value** | **VOUTX** |
|---|---|
| 0000 | Controlled by $I^2C$ register LDOx_EN[3:0] |
| x001 | Slot1 |
| x010 | Slot2 |

| | |
|---|---|
| x011 | Slot3 |
| x100 | Slot4 |
| x101 | Slot5 |
| x110 | Slot6 |
| x111 | Slot7 |

- **0x0E LDO_EN Register ----LDOs Chip enable control register**

Chip enable control register(bit3~bit0) by I²C while the register value of LDOx_SEQ[3:0] are set to be default "0000". This register can be written to enable or disable the corresponding LDO regulator. Bit0 for LDO1, Bit1 for LDO2, Bit2 for LDO3,Bit3 for LDO4.

EN_SEL(bit6) bit is EN pin function select register:

(1) When EN_SEL=0, EN port function is shown as below:

1) EN=H, four LDOs output fixed value, LDO1/2 output 1.2V, LDO3/4 output 2.8V, it can't change any LDO output value or disable any LDO by I²C.

2) EN=L, any LDO output voltage and LDO enable signal can be set by I²C.

(2) When EN_SEL=H, EN port function is shown as below:

1) EN=H, any LDO enable signal and output voltage can be set by I²C.

2) EN=L, all LDOs will be disable, the enable and output voltage setting by I²C are ignored.

REG_RST(bit7) bit is a software reset bit, all the register will be reset to default value if this bit is set to "1".

- **0x0F SEQ_C Register ---- Power sequence setting and status register**

SEQ_SPEED[1:0] define the slot period as following. (Read/Write)

| Register Value | Slot period(ms) |
|---|---|
| 00 | 2.00 |
| 01 | 1.00 |
| 10 | 0.50 |
| 11 | 0.25 |

SEQ_CTRL[1:0] enables power-up or shut down of SEQ .(Read/Write)

| Register Value | SEQ Status |
|---|---|
| x0 | Shutdown |
| x1 | Power-up |

SEQ_ON indicates the activation signal of SEQ. (Read only)

| Register Value | SEQ Status |
|---|---|
| 0 | Shutdown |
| 1 | Power-up |

SEQ_COUNT[2:0] indicates the slot number of SEQ at the moment. (Read only)

| Register Value | SEQ Counter |
|---|---|
| 000 | No LDO starts. |
| 001 | Slot1 starts |
| 010 | Slot2 starts |

| | |
|---|---|
| 011 | Slot3 starts |
| 100 | Slot4 starts |
| 101 | Slot5 starts |
| 110 | Slot6 starts |
| 111 | Slot7 starts and stop counting |

- **0x10 ILIMIT Register ----LDO Current Limit Selection**

Provide more step current limit selection for each LDO if customer need, shown as above Table1/2.

## Absolute Maximum Ratings

| Item | | Rating | Unit |
|---|---|---|---|
| IN Voltage (AVIN, DVIN) | | -0.3 to 6.5 | V |
| Other Pin Voltage | | -0.3 to $V_{IN}$+0.3 | V |
| LDO1/2 Maximum Load Current | | 1500/1200 | mA |
| LDO3/4 Maximum Load Current | | 400 | mA |
| Maximum Power Consumption | | 1800 | mW |
| Operating Junction Temperature | | -40 to 150 | °C |
| Storage Temperature | | -65 to 150 | °C |
| Lead Temperature (Soldering, 10 sec) | | 300 | °C |
| ESD Capacity | HBM | ±2000 | V |
| | CDM | ±1500 | V |

## Recommended Operating Conditions

| Symbol | Item | Rating | Unit |
|---|---|---|---|
| $V_{AVIN}$ | Input Voltage[(1)] | 2.5 to 5.5 | V |
| $V_{DVIN}$ | Input Voltage | 0.6 to 2.2 | V |
| $I_{AVOx}$ | Output Current (400mA LDOs) | 0 to 400 | mA |
| $I_{DVO1}$ | Output Current (1500mA LDO) | 0 to 1500 | mA |
| $I_{DVO2}$ | Output Current (1200mA LDO) | 0 to 1200 | mA |
| $T_A$ | Operating Ambient Temperature | -40 to 85 | °C |
| $C_{AVIN}$ | AVIN Effective Input Ceramic Capacitor Value | 2.2 to 10 | μF |
| $C_{DVIN}$ | DVIN Effective Input Ceramic Capacitor Value | 2.2 to 10 | μF |
| $C_{DVO1}$ | Effective Output Ceramic Capacitor Value (1500mA LDO) | 3.3 to 47 | μF |
| $C_{DVO2}$ | Effective Output Ceramic Capacitor Value (1200mA LDO) | 3.3 to 47 | μF |
| $C_{AVOx}$ | Effective Output Ceramic Capacitor Value (400mA LDO) | 0.68 to 10 | μF |
| ESR | Input and Output Capacitor Equivalent Series Resistance | 5 to 100 | mΩ |

## Electrical Characteristics

(Unless otherwise noted, $V_{AVIN}$=$V_{AVOx}$+1V, $V_{DVIN}$=$V_{DVOx}$+0.3V, $V_{AVIN}$=($V_{DVOx}$+1.6V) or 3.0V whichever greater, $I_{OUT}$=1mA, $C_{DVIN}$=4.7μF, $C_{AVIN}$=4.7μF, $C_{DVOx}$=4.7μF, $C_{AVOx}$=1μF, $T_A$ = -40°C~85°C. Typical values are at $T_A$=25 ºC)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage Range | $V_{DVIN}$ | $V_{DVIN}$>$V_{DVOx}$ | $V_{DVOx}$ + $V_{DROP\_DVOx}$ | | 2.2 | V |
| $V_{AVIN}$ Voltage Range | $V_{AVIN}$ (1) | $V_{DVO}$+1.6V, $V_{AVIN}$>2.5 | 2.5 | | 5.5 | V |
| Under-voltage lock-out | $V_{UVLO}$ | $V_{AVIN}$ falling | 1.5 | 1.9 | 2.3 | V |
| Hysteresis | $V_{UVLO\_HYS}$ | Under-voltage Lock-out Hysteresis | | 0.2 | | V |
| $V_{AVIN}$ Current | $I_{Q\_ON}$ | Active mode: $V_{EN}$=$V_{AVIN}$ or Enable chip by $I^2C$, no load | 60 | 85 | 150 | μA |
| | $I_{Q\_OFF}$ | $V_{EN}$=0V or Shutdown by $I^2C$ | | 0.6 | 3 | μA |
| EN Pull-down Current | $I_{EN}$ | $V_{EN}$=5.5V, $V_{AVIN}$=5.5V | | 0.3 | 1 | μA |
| EN Input Voltage High | $V_{ENH}$ | | 0.9 | | | V |
| EN Input Voltage Low | $V_{ENL}$ | | | | 0.4 | V |
| SCL/SDA Input Voltage High | $V_{I2CH}$ | | 0.9 | | | V |
| SCL/SDA Input Voltage Low | $V_{I2CL}$ | | | | 0.4 | V |
| SDA Logic Low Output | $V_{OL}$ | 3mA Sink | | | 0.4 | V |
| SCL Clock Frequency | $F_{SCL}$ | | | | 1000 | kHz |
| Thermal Shutdown Threshold | $T_{TSD}$ (3) | $T_J$ rising | | 150 | | °C |
| Thermal Shutdown Hysteresis | $T_{HYS}$ (3) | $T_J$ falling from shutdown | | 30 | | °C |

### 1500mA LDO1

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage | $V_{DVO1}$ | $I_{OUT}$=1mA~1500mA, $T_A$=25 ºC | -2 | | 2 | % |
| | | $I_{OUT}$=1mA~1500mA, $T_A$ = -40°C~85°C | -2.5 | | 2.5 | |
| Dropout Voltage | $V_{DROP\_DVO1}$ (2) | $I_{OUT}$ = 1000mA, $V_{OUT}$=1.2V | | 100 | 150 | mV |
| | | $I_{OUT}$ = 1500mA, $V_{OUT}$=1.2V | | 150 | 230 | |

## Electrical Characteristics (Continued)

(Unless otherwise noted, $V_{AVIN}$=$V_{AVOx}$+1V, $V_{DVIN}$=$V_{DVOx}$+0.3V, $V_{AVIN}$=($V_{DVOx}$+1.6V) or 3.0V whichever greater, $I_{OUT}$=1mA, $C_{DVIN}$=4.7μF, $C_{AVIN}$=4.7μF, $C_{DVOx}$=4.7μF, $C_{AVOx}$=1μF, $T_A$ = -40°C~85°C. Typical values are at $T_A$=25 ºC)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Current | $I_{OUT\_DVO1}$ | | 1500 | | | mA |
| Current Limit | $I_{LIM\_DVO1}$ | Default Current Limit Register | 1.55 | 2 | 3 | A |
| Short Current Limit | $I_{SHORT\_DVO1}$ | Default Current Limit Register | 200 | 350 | 500 | mA |
| Load Regulation | $Reg_{LOAD\_DVO1}$ | 1mA≤$I_{OUT}$≤1500mA | | 10 | 20 | mV |
| $V_{DVIN}$ Line Regulation | $Reg_{LINE\_DVO1}$ | $V_{DVO1}$+0.3V≤$V_{DVIN}$≤5.5 V ($I_{OUT}$ =10mA) | | 0.02 | 0.2 | %/V |
| $V_{AVIN}$ Line Regulation | | 3.0V or ($V_{DVO1}$+ 1.6 V) whichever greater < $V_{AVIN}$ < 5.5V, ($V_{DVIN}$=$V_{DVO1}$+0.3V, $I_{OUT}$=10mA) | | 0.02 | 0.2 | %/V |
| Power Supply Rejection Ratio | $PSRR\__{DVO1}$[3] (DVIN to DVO1) | $V_{DVIN}$ to $V_{DVO1}$, f=100Hz, $V_{DVIN}$=1.5V, $V_{DVO1}$=1.2V, Ripple 0.2$V_{PP}$, $I_{OUT}$=30mA | | 80 | | dB |
| | | $V_{DVIN}$ to $V_{DVO1}$, f=1kHz, $V_{DVIN}$=1.5V, $V_{DVO1}$=1.2V, Ripple 0.2$V_{PP}$, $I_{OUT}$=30mA | | 80 | | |
| | | $V_{DVIN}$ to $V_{DVO1}$, f=10kHz, $V_{DVIN}$=1.5V, $V_{DVO1}$=1.2V, Ripple 0.2$V_{PP}$, $I_{OUT}$=30mA | | 60 | | |
| | | $V_{DVIN}$ to $V_{DVO1}$, f=100kHz, $V_{DVIN}$=1.5V, $V_{DVO1}$=1.2V, Ripple 0.2$V_{PP}$, $I_{OUT}$=30mA | | 30 | | |
| | | $V_{DVIN}$ to $V_{DVO1}$, f=1MHz, $V_{DVIN}$=1.5V, $V_{DVO1}$=1.2V, Ripple 0.2$V_{PP}$, $I_{OUT}$=30mA | | 40 | | |
| | $PSRR\__{DVO1}$[3] (AVIN to DVO1) | $V_{AVIN}$ to $V_{DVO1}$, f=1kHz, $V_{DVIN}$=1.5V, $V_{DVO1}$=1.2V, Ripple 0.2$V_{PP}$, $I_{OUT}$=30mA | | 80 | | |
| | | $V_{AVIN}$ to $V_{DVO1}$, f=1MHz, $V_{DVIN}$=1.5V, $V_{DVO1}$=1.2V, Ripple 0.2$V_{PP}$, $I_{OUT}$=30mA | | 60 | | |
| Output Noise | $e_{N\_DVO1}$[3] | $V_{DVIN}$=1.5V, $V_{DVO1}$=1.2V, f= 10 Hz to 100 kHz | | 50 | | $\mu V_{RMS}$ |
| Output Resistance of Auto Discharge at Off State | $R_{DIS\_DVO1}$ | $V_{EN}$=0V, or shutdown by $I^2C$, $V_{OUT}$ =0.5V, $V_{AVIN}$=3.8V | 250 | 350 | 450 | Ω |

## Electrical Characteristics (Continued)

(Unless otherwise noted, $V_{AVIN}$=$V_{AVOx}$+1V, $V_{DVIN}$=$V_{DVOx}$+0.3V, $V_{AVIN}$=($V_{DVOx}$+1.6V) or 3.0V whichever greater, $I_{OUT}$=1mA, $C_{DVIN}$=4.7μF, $C_{AVIN}$=4.7μF, $C_{DVOx}$=4.7μF, $C_{AVOx}$=1μF, $T_A$ = -40°C~85°C. Typical values are at $T_A$=25 ºC)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Line Transient | $V_{TRLN\_DVO1}$[3] (DVIN to DVO1) | $V_{OUT}$=1.2V $V_{DVIN}$= $V_{DVO1}$+0.3V to $V_{DVO1}$+1.3V in 10us, $I_{OUT}$=1mA, $T_A$=25°C | | 5 | 30 | mV |
| | | $V_{OUT}$=1.2V $V_{DVIN}$= $V_{DVO1}$+1.3V to $V_{DVO1}$+0.3V in 10us, $I_{OUT}$=1mA, $T_A$=25°C | | 5 | 30 | mV |
| | $V_{TRLN\_DVO1}$[3] (AVIN to DVO1) | $V_{OUT}$=1.2V $V_{AVIN}$=($V_{DVOx}$+1.6V) or 3.0V to 5.5V in 10us, $I_{OUT}$=1mA, $T_A$=25°C | | 5 | 30 | mV |
| | | $V_{OUT}$=1.2V $V_{AVIN}$=5.5V to ($V_{DVOx}$+1.6V) or 3.0V in 10us, $I_{OUT}$=1mA, $T_A$=25°C | | 5 | 30 | mV |
| Load Transient | $V_{TRLD\_DVO1}$[3] | $V_{OUT}$=1.2V $I_{OUT}$=1mA to 1500mA in 10us $V_{DVIN}$= $V_{DVO1}$+0.3V, $T_A$=25°C | | 80 | 160 | mV |
| | | $V_{OUT}$=1.2V $I_{OUT}$=1500mA to 1mA in 10us $V_{DVIN}$= $V_{DVO1}$+0.3V, $T_A$=25°C | | 80 | 160 | mV |
| Turn-On Time | $t_{ON\_DVO1}$[3] | From assertion of $V_{EN}$ to $V_{OUT}$=95%$V_{DVO(NOM)}$ | | 300 | 450 | μs |

## 1200mA LDO2

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage | $V_{DVO2}$ | $I_{OUT}$=1mA~1200mA, $T_A$=25 ºC | -2 | | 2 | % |
| | | $I_{OUT}$=1mA~1200mA, $T_A$ = -40°C~85°C | -2.5 | | 2.5 | |
| Dropout Voltage | $V_{DROP\_DVO2}$[2] | $I_{OUT}$ = 800mA, $V_{OUT}$=1.2V | | 100 | 150 | mV |
| | | $I_{OUT}$ = 1200mA, $V_{OUT}$=1.2V | | 160 | 240 | |
| Output Current | $I_{OUT\_DVO2}$ | | 1200 | | | mA |
| Current Limit | $I_{LIM\_DVO2}$ | Default Current Limit Register | 1.25 | 1.5 | 1.9 | A |
| Short Current Limit | $I_{SHORT\_DVO2}$ | Default Current Limit Register | 100 | 300 | 460 | mA |

## Electrical Characteristics (Continued)

(Unless otherwise noted, $V_{AVIN}$=$V_{AVOx}$+1V, $V_{DVIN}$=$V_{DVOx}$+0.3V, $V_{AVIN}$=($V_{DVOx}$+1.6V) or 3.0V whichever greater, $I_{OUT}$=1mA, $C_{DVIN}$=4.7μF, $C_{AVIN}$=4.7μF, $C_{DVOx}$=4.7μF, $C_{AVOx}$=1μF, $T_A$ = -40°C~85°C. Typical values are at $T_A$=25 ºC)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Load Regulation | $Reg_{LOAD\_DVO2}$ | 1mA≤$I_{OUT}$≤1200mA | | 8 | 20 | mV |
| $V_{DVIN}$ Line Regulation | $Reg_{LINE\_DVO2}$ | $V_{DVO2}$+0.3V≤$V_{DVIN}$≤5.5 V ($I_{OUT}$ =10mA) | | 0.02 | 0.2 | %/V |
| $V_{AVIN}$ Line Regulation | | 3.0V or ($V_{DVO2}$+ 1.6 V) whichever greater < $V_{AVIN}$ < 5.5V, ($V_{DVIN}$=$V_{DVO2}$+0.3V, $I_{OUT}$=10mA) | | 0.02 | 0.2 | %/V |
| Power Supply Rejection Ratio | $PSRR\_{DVO2}$[3] (DVIN to DVO2) | $V_{DVIN}$ to $V_{DVO2}$, f=100Hz, $V_{DVIN}$=1.5V, $V_{DVO2}$=1.2V, Ripple 0.2$V_{PP}$, $I_{OUT}$=30mA | | 80 | | dB |
| | | $V_{DVIN}$ to $V_{DVO2}$, f=1kHz, $V_{DVIN}$=1.5V, $V_{DVO2}$=1.2V, Ripple 0.2$V_{PP}$, $I_{OUT}$=30mA | | 80 | | |
| | | $V_{DVIN}$ to $V_{DVO2}$, f=10kHz, $V_{DVIN}$=1.5V, $V_{DVO2}$=1.2V, Ripple 0.2$V_{PP}$, $I_{OUT}$=30mA | | 60 | | |
| | | $V_{DVIN}$ to $V_{DVO2}$, f=100kHz, $V_{DVIN}$=1.5V, $V_{DVO2}$=1.2V, Ripple 0.2$V_{PP}$, $I_{OUT}$=30mA | | 30 | | |
| | | $V_{DVIN}$ to $V_{DVO2}$, f=1MHz, $V_{DVIN}$=1.5V, $V_{DVO2}$=1.2V, Ripple 0.2$V_{PP}$, $I_{OUT}$=30mA | | 40 | | |
| | $PSRR\_{DVO2}$[3] (AVIN to DVO2) | $V_{AVIN}$ to $V_{DVO2}$, f=1kHz, $V_{DVIN}$=1.5V, $V_{DVO2}$=1.2V, Ripple 0.2$V_{PP}$, $I_{OUT}$=30mA | | 80 | | |
| | | $V_{AVIN}$ to $V_{DVO2}$, f=1MHz, $V_{DVIN}$=1.5V, $V_{DVO2}$=1.2V, Ripple 0.2$V_{PP}$, $I_{OUT}$=30mA | | 60 | | |
| Output Noise | $e_{N\_DVO2}$[3] | $V_{DVIN}$=1.5V, $V_{DVO2}$=1.2V, f= 10 Hz to 100 kHz | | 50 | | $\mu V_{RMS}$ |
| Output Resistance of Auto Discharge at Off State | $R_{DIS\_DVO2}$ | $V_{EN}$=0V, or shutdown by $I^2C$, $V_{OUT}$ =0.5V $V_{AVIN}$=3.8V | 250 | 350 | 450 | Ω |

## Electrical Characteristics (Continued)

(Unless otherwise noted, $V_{AVIN}$=$V_{AVOx}$+1V, $V_{DVIN}$=$V_{DVOx}$+0.3V, $V_{AVIN}$=($V_{DVOx}$+1.6V) or 3.0V whichever greater, $I_{OUT}$=1mA, $C_{DVIN}$=4.7μF, $C_{AVIN}$=4.7μF, $C_{DVOx}$=4.7μF, $C_{AVOx}$=1μF, $T_A$ = -40°C~85°C. Typical values are at $T_A$=25 ºC)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Line Transient | $V_{TRLN\_DVO2}$[3] (DVIN to DVO2) | $V_{OUT}$=1.2V $V_{DVIN}$= $V_{DVO2}$+0.3V to $V_{DVO2}$+1.3V in 10us, $I_{OUT}$=1mA, $T_A$=25°C | | 5 | 30 | mV |
| | | $V_{OUT}$=1.2V $V_{DVIN}$= $V_{DVO2}$+1.3V to $V_{DVO2}$+0.3V in 10us, $I_{OUT}$=1mA, $T_A$=25°C | | 5 | 30 | mV |
| | $V_{TRLN\_DVO2}$[3] (AVIN to DVO2) | $V_{OUT}$=1.2V $V_{AVIN}$=($V_{DVOx}$+1.6V) or 3.0V to 5.5V in 10us, $I_{OUT}$=1mA, $T_A$=25°C | | 5 | 30 | mV |
| | | $V_{OUT}$=1.2V $V_{AVIN}$=5.5V to ($V_{DVOx}$+1.6V) or 3.0V in 10us, $I_{OUT}$=1mA, $T_A$=25°C | | 5 | 30 | mV |
| Load Transient | $V_{TRLD\_DVO2}$[3] | $V_{OUT}$=1.2V $I_{OUT}$=1mA to 1200mA in 10us $V_{DVIN}$= $V_{DVO2}$+0.3V, $T_A$=25°C | | 70 | 140 | mV |
| | | $V_{OUT}$=1.2V $I_{OUT}$=1200mA to 1mA in 10us $V_{DVIN}$= $V_{DVO2}$+0.3V, $T_A$=25°C | | 70 | 140 | mV |
| Turn-On Time | $t_{ON\_DVO2}$[3] | From assertion of $V_{EN}$ to $V_{OUT}$=95%$V_{DVO(NOM)}$ | | 300 | 450 | μs |

## 400mA LDO3/LDO4

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Dropout Voltage | $V_{DROP\_AVOx}$[3] | $I_{OUT}$ = 400mA, $V_{AVOx}$=2.8V | | 120 | 175 | mV |
| | | $I_{OUT}$ = 150mA, $V_{AVOx}$=2.8V | | 45 | 65 | mV |
| Regulated Output Voltage | $V_{AVOx}$ | $I_{OUT}$=1mA~400mA,$T_A$=25°C | -2 | | 2 | % |
| | | $I_{OUT}$=1mA~400mA, $T_A$ = -40°C~85°C | -2.5 | | 2.5 | |
| Output Voltage Line Regulation | $Reg_{LINE\_AVOx}$ | $V_{AVOx}$=2.8V, 3.8V≤$V_{AVIN}$≤5.5V, $I_{OUT}$ = 10mA （$\Delta V_{AVOx}/\Delta V_{AVIN}/V_{AVOx}$） | | 0.01 | 0.2 | %/V |
| Output Voltage Load Regulation | $Reg_{LOAD\_AVOx}$ | $I_{OUT}$ from 1mA to 400mA | | 10 | 40 | mV |

## Electrical Characteristics (Continued)

(Unless otherwise noted, $V_{AVIN}$=$V_{AVOx}$+1V, $V_{DVIN}$=$V_{DVOx}$+0.3V, $V_{AVIN}$=($V_{DVOx}$+1.6V) or 3.0V whichever greater, $I_{OUT}$=1mA, $C_{DVIN}$=4.7μF, $C_{AVIN}$=4.7μF, $C_{DVOx}$=4.7μF, $C_{AVOx}$=1μF, $T_A$ = -40°C~85°C. Typical values are at $T_A$=25 ºC)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Line Transient (The absolute value of the output change) | $V_{TRLN\_AVOx}$(3) | $V_{AVOx}$=2.8V, $I_{OUT}$ =1mA, $V_{AVIN}$ =3.8V to 5.5V in 10us, $T_A$=25°C | | 5 | 20 | mV |
| | | $V_{AVOx}$=2.8V, $I_{OUT}$ = 1mA, $V_{AVIN}$ =5.5V to 3.8V in 10us, $T_A$=25°C | | 5 | 20 | |
| Load Transient (The absolute value of the output change) | $V_{TRLD\_AVOx}$(3) | $V_{AVOx}$=2.8V, $V_{AVIN}$ =3.8V, $I_{OUT}$ from 1mA to 400mA in 10us, $T_A$=25°C | | 30 | 60 | mV |
| | | $V_{AVOx}$=2.8V, $V_{AVIN}$=3.8V, $I_{OUT}$ from 400mA to 1mA in 10us, $T_A$=25°C | | 30 | 60 | |
| Output Current | $I_{OUT\_AVOx}$ | | 400 | | | mA |
| Over Current Limit | $I_{LMT\_AVOx}$ | Default Current Limit Register, $V_{AVIN}$= $V_{LDOx\_VSET}$+1V, $T_A$=25°C | 400 | 600 | 1000 | mA |
| Short Current Limit | $I_{SHORT\_AVOx}$ | Default Current Limit Register, $V_{AVOx}$=0V, $T_A$=25°C | 20 | 50 | 80 | mA |
| Power Supply Rejection Ratio | PSRR_$_{AVO}$(3) | f=100Hz, $I_{OUT}$=20mA, $V_{AVIN}$= $V_{LDOx\_VSET}$+1V, $T_A$=25°C | | 90 | | dB |
| | | f=1kHz, $I_{OUT}$=20mA, $V_{AVIN}$= $V_{LDOx\_VSET}$+1V, $T_A$=25°C | | 90 | | |
| | | f=10kHz, $I_{OUT}$=20mA, $V_{AVIN}$= $V_{LDOx\_VSET}$+1V, $T_A$=25°C | | 75 | | |
| | | f=100Hz, $I_{OUT}$=20mA, $V_{AVIN}$= $V_{LDOx\_VSET}$+1V, $T_A$=25°C | | 65 | | |
| | | f=1MHz, $I_{OUT}$=20mA, $V_{AVIN}$= $V_{LDOx\_VSET}$+1V, $T_A$=25°C | | 40 | | |
| Output Noise | $e_N$(3) | 10Hz to 100kHz, $I_{OUT}$ =30mA, $V_{AVOx}$ =2.8V, $V_{AVIN}$= 3.8V, $T_A$=25°C | | 8 | | $\mu V_{RMS}$ |

## Electrical Characteristics (Continued)

(Unless otherwise noted, $V_{AVIN}$=$V_{AVOx}$+1V, $V_{DVIN}$=$V_{DVOx}$+0.3V, $V_{AVIN}$=($V_{DVOx}$+1.6V) or 3.0V whichever greater, $I_{OUT}$=1mA, $C_{DVIN}$=4.7μF, $C_{AVIN}$=4.7μF, $C_{DVOx}$=4.7μF, $C_{AVOx}$=1μF, $T_A$ = -40°C~85°C. Typical values are at $T_A$=25 ºC)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Resistance of Auto Discharge at Off State | $R_{LOW\_AVOx}$ | $V_{EN}$=0V, or Shutdown by $I^2C$, $V_{AVIN}$=3.8V, $I_{OUT}$=10mA | 250 | 350 | 450 | Ω |
| Output Turn-on Delay Time | $t_{ON\_AVOx}$(3) | From $V_{EN}$> $V_{IH}$ to $V_{OUT}$ = 95% of $V_{OUT(NOM)}$ | | 180 | 300 | μs |

***Note1:*** Here $V_{AVIN}$ means internal circuit can work normal.

If $V_{AVIN}$ <$V_{AVOx}$, Output voltage follow $V_{AVIN}$ ($I_{OUT}$=1mA), circuit is safety.

The minimum AVIN voltage of this chip is 2.5V, if you need better performance, it is recommended that $V_{AVIN}$ ≥ 3V.

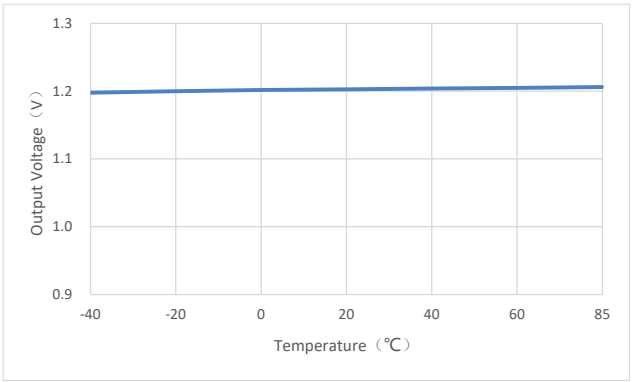
***Note2:*** $V_{DROP\_DVO}$ and $V_{DROP\_AVOx}$ FT test method:

Test the $V_{OUT}$ voltage at $V_{LDOx}$_vset +$V_{DROPMAX}$ with output current.

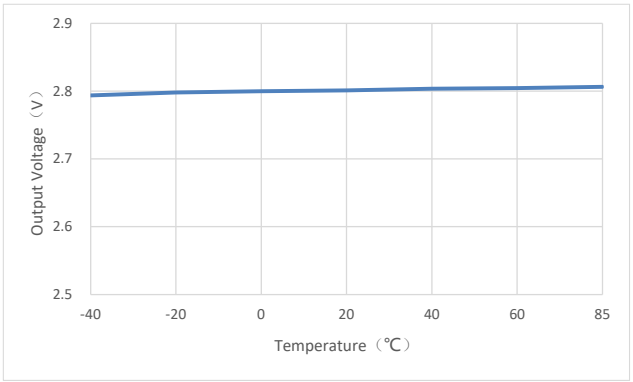
***Note3:*** Guaranteed by design and characterization, not a FT item.

## Typical Characteristics

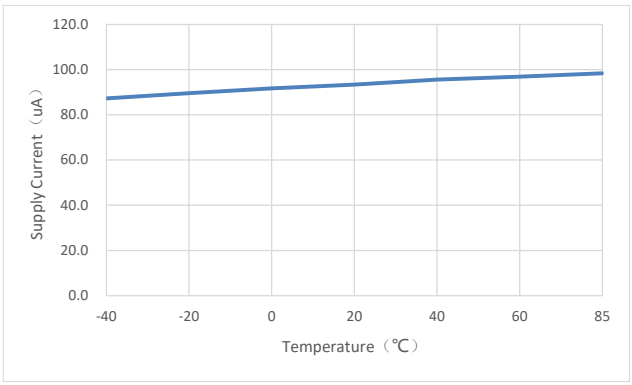
(Unless otherwise noted, $V_{AVIN}$=$V_{AVOx}$+1V, $V_{DVIN}$=$V_{DVOx}$+0.3V, $V_{AVIN}$=($V_{DVOx}$+1.6V) or 3.0V whichever greater, $I_{OUT}$=1mA, $C_{DVIN}$=4.7μF, $C_{AVIN}$=4.7μF, $C_{DVOx}$=4.7μF, $C_{AVOx}$=1μF, $T_A$ = -40°C~85°C. Typical values are at. $T_A$=25 ºC)



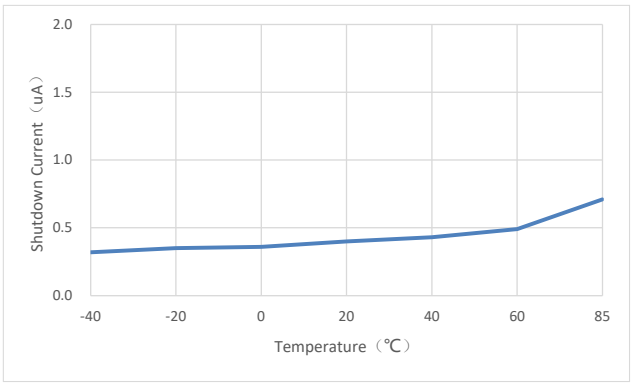

DVO1/2 Output Voltage VS Temperature



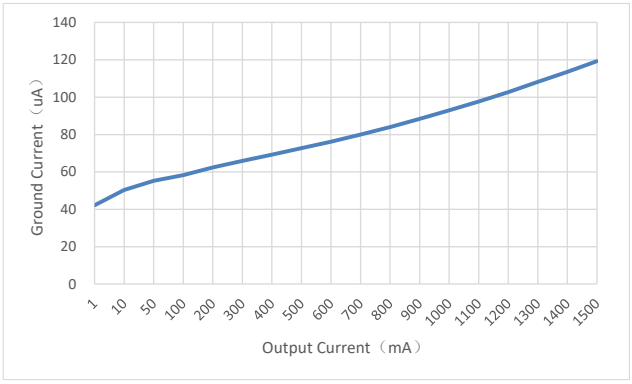

AVO1/2 Output Voltage VS Temperature



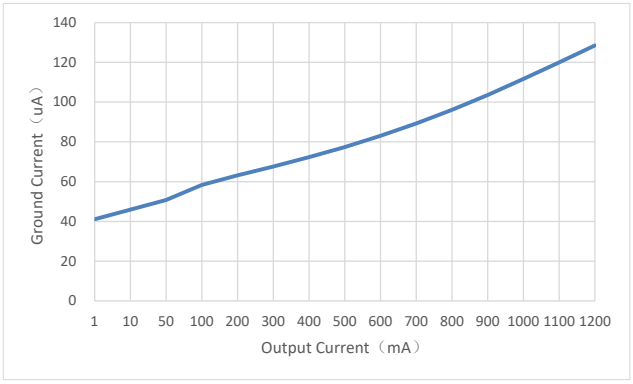

IQ-on VS Temperature




IQ-off VS Temperature

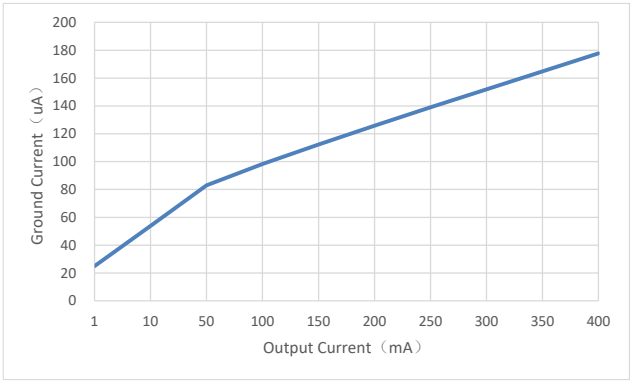



DVO1 $I_{GND}$ VS Temperature

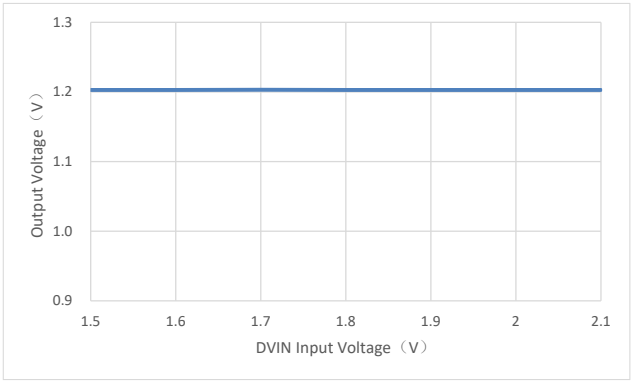



DVO2 $I_{GND}$ VS Temperature

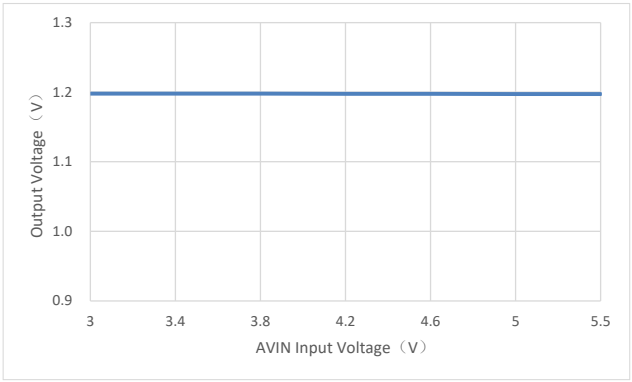
## Typical Characteristics(continued)



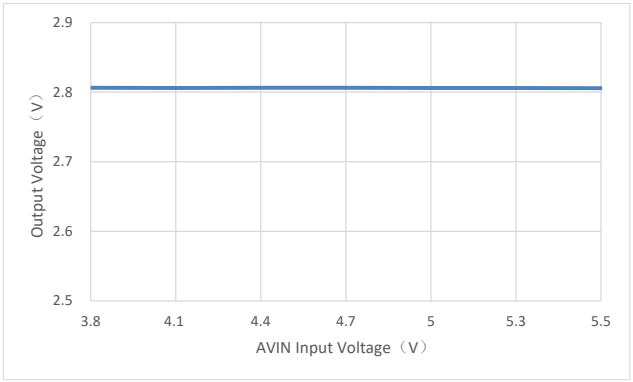

AVO1/2 $I_{GND}$ VS Temperature



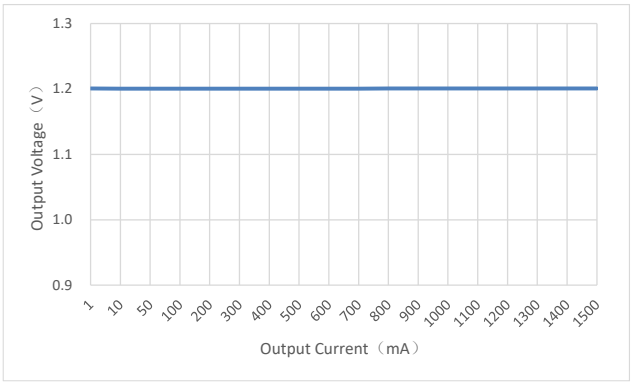

DVO1/2 VS DVIN



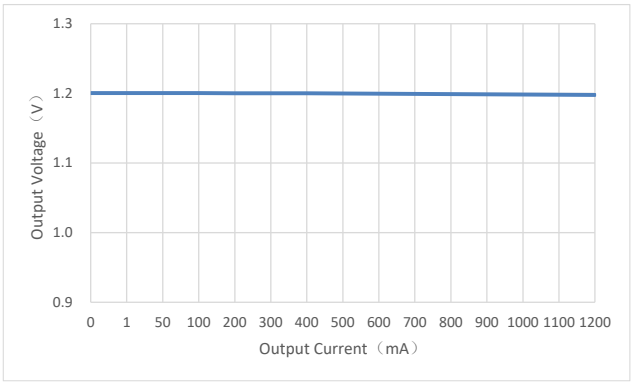

DVO1/2 VS AVIN




AVO1/2 VS AVIN

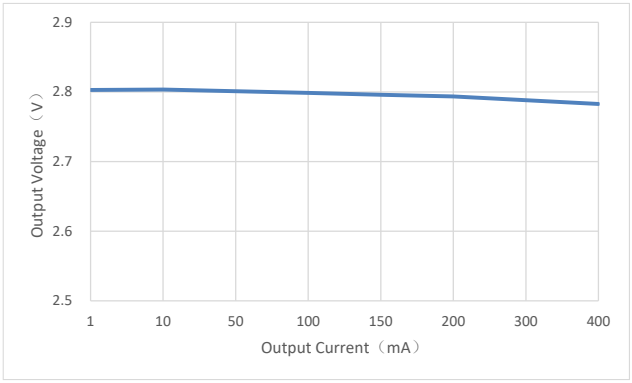



DVO1 VS Output Current

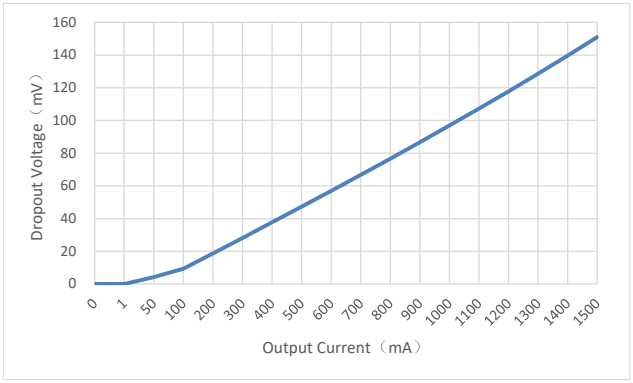



DVO2 VS Output Current

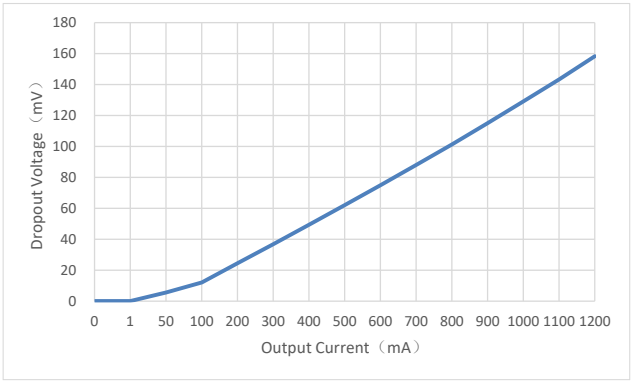
## Typical Characteristics(continued)



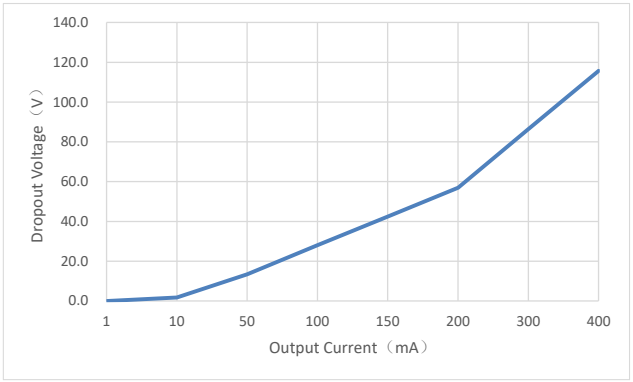

AVO1/2 VS Output Current



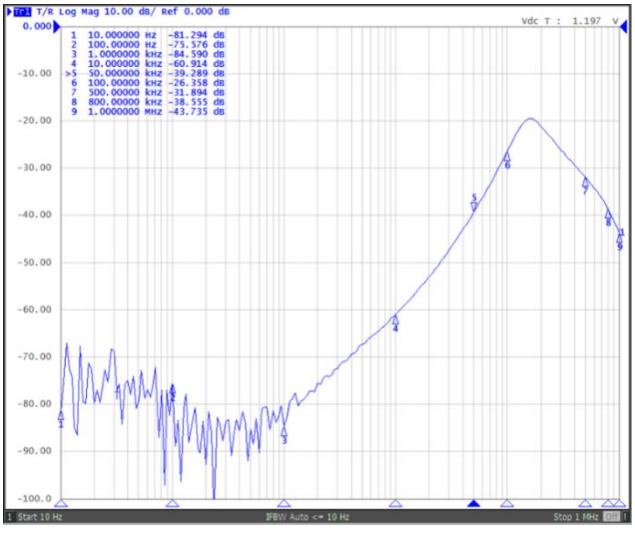

DVO1 Dropout Voltage VS Output Current



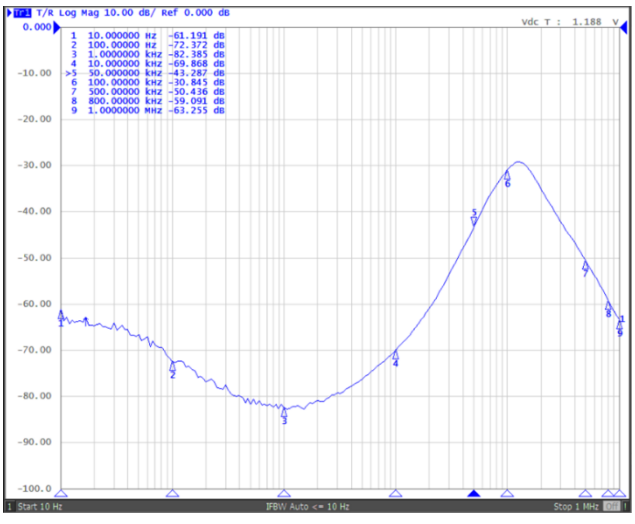

DVO2 Dropout Voltage VS Output Current




AVO1/2 Dropout Voltage VS Output Current

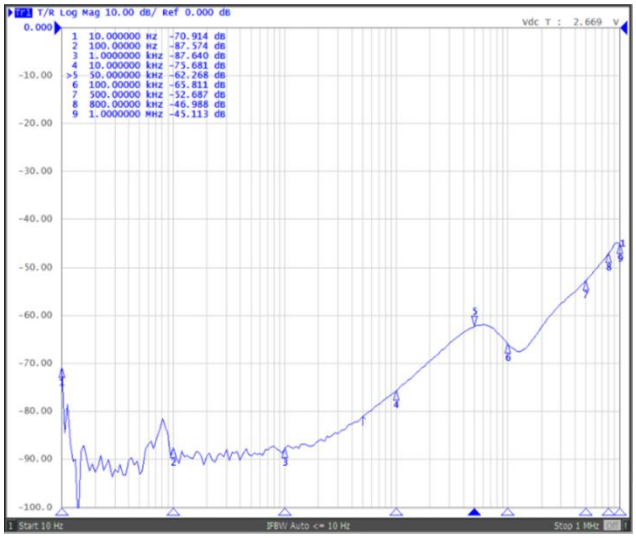



DVO1/2 PSRR-$V_{DVIN}$

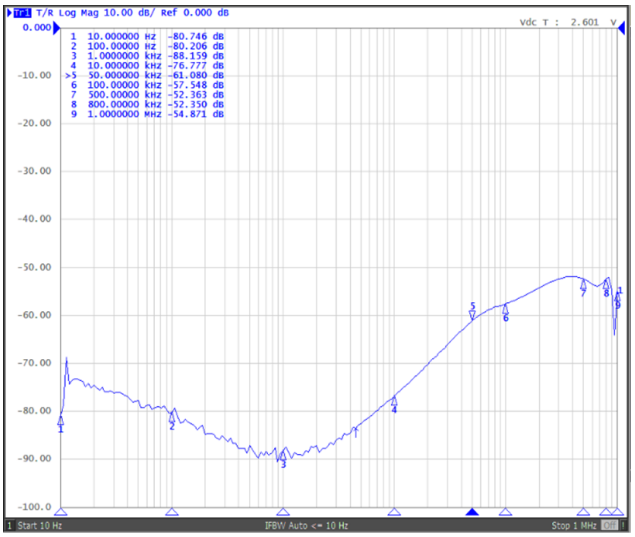



DVO1/2 PSRR-$V_{AVIN}$

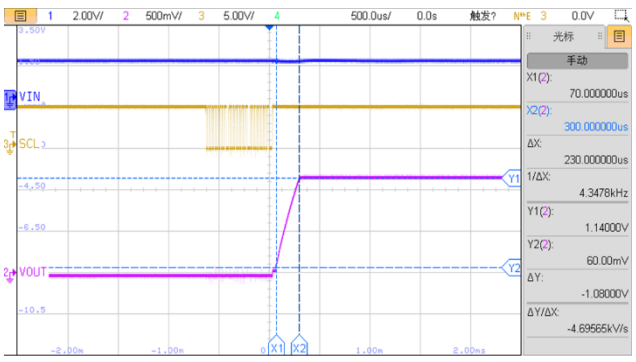
## Typical Characteristics(continued)



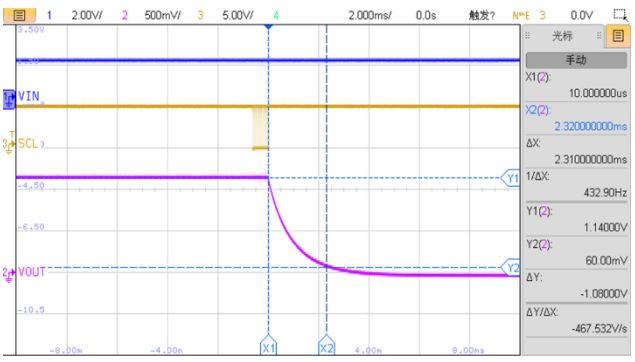
AVO1/2 PSRR-$V_{AVIN}$ （IOUT=20mA）



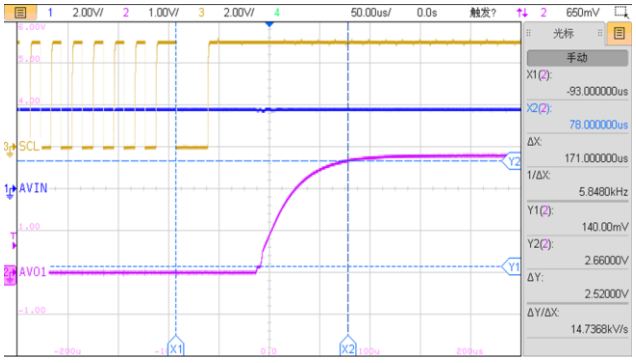
AVO1/2 PSRR-$V_{AVIN}$ （IOUT=100mA）



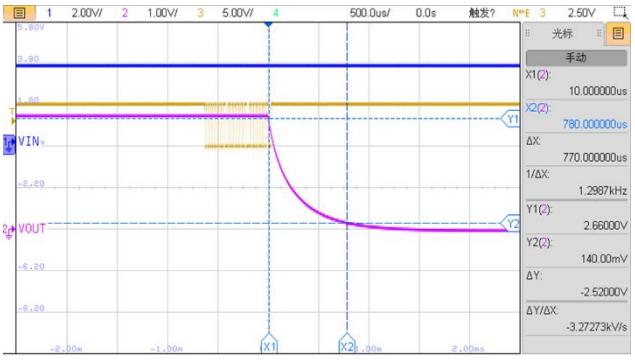
DVO1/2 Ton



DVO1/2 Toff

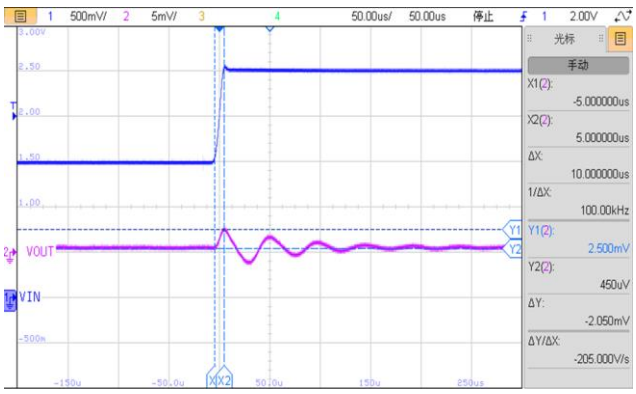


AVO1/2 Ton

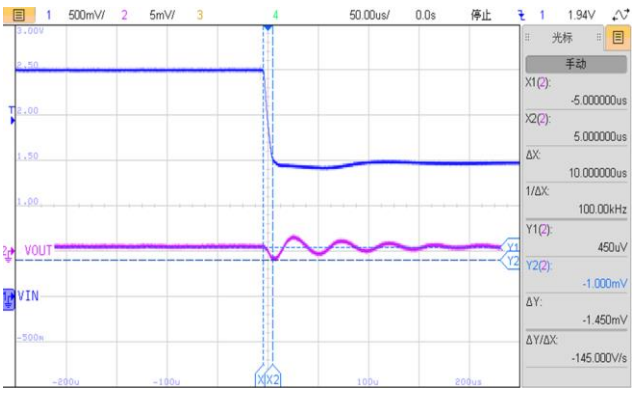


AVO1/2 Toff

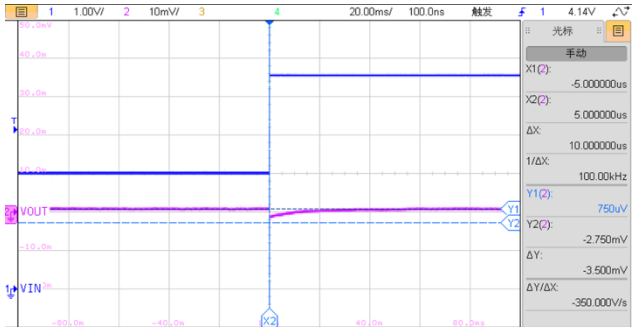
## Typical Characteristics(continued)



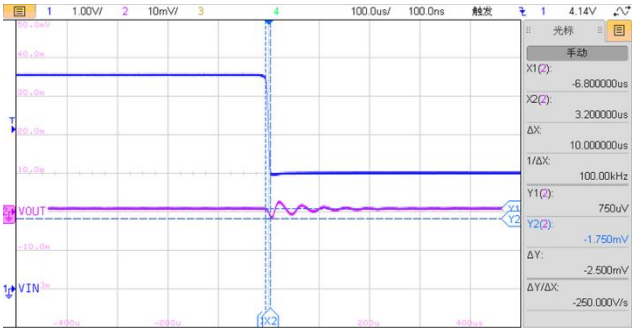

DVO1/2 DVIN=1.5V to 2.5V



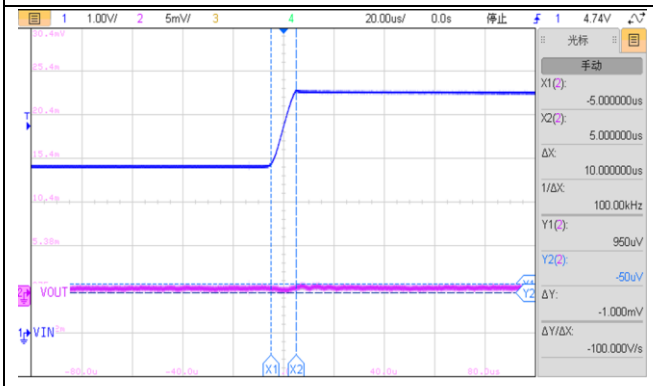

DVO1/2 DVIN=2.5V to 1.5V



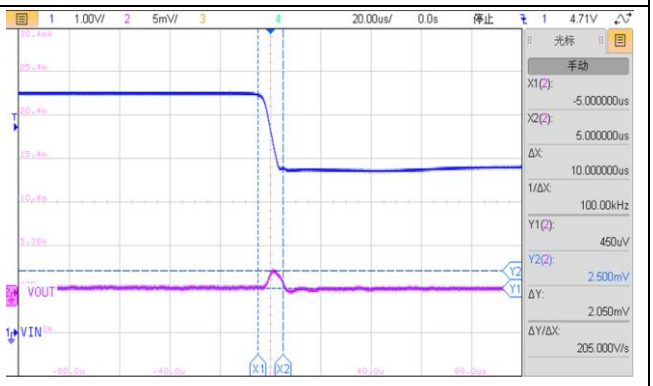

DVO1/2 AVIN=3V to 5.5V



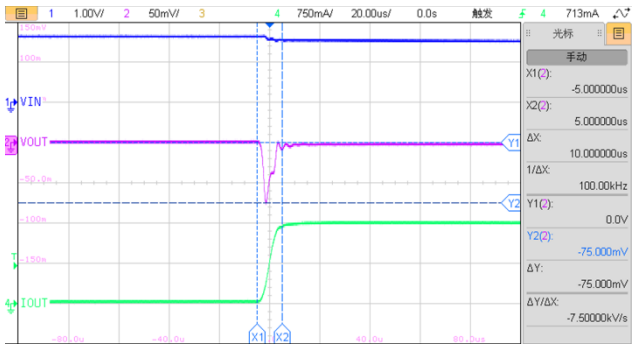

DVO1/2 AVIN=5.5V to 3V



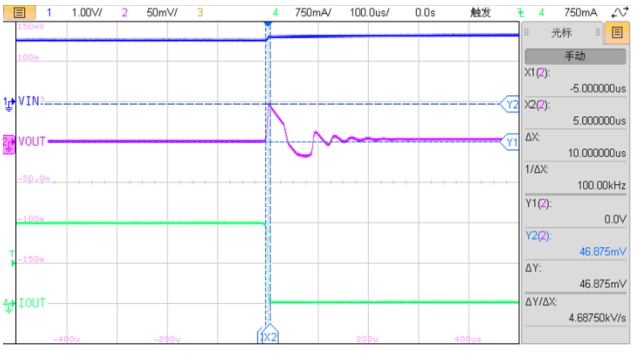

AVO1/2 AVIN=3.8V to 5.5V




AVO1/2 AVIN=5.5V to 3.8V

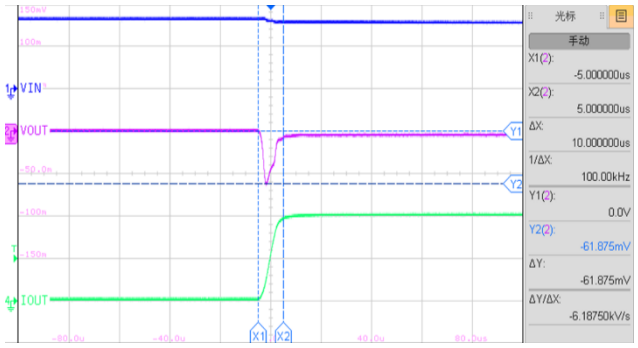



DVO1 IOUT=1mA to 1.5A

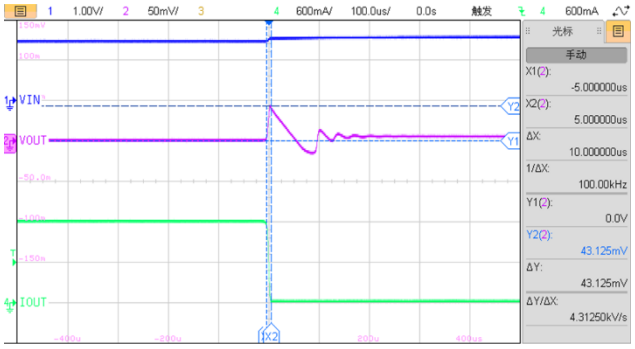



DVO1 IOUT=1.5A to 1mA

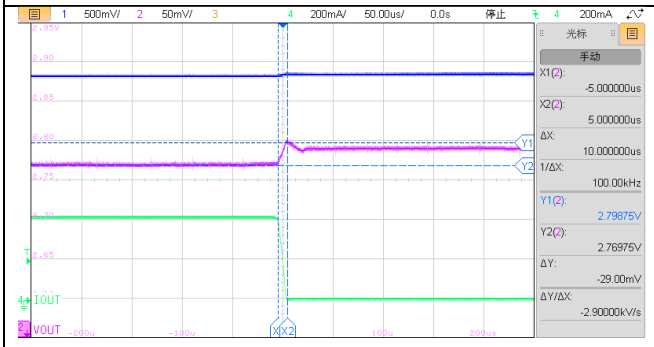
## Typical Characteristics(continued)



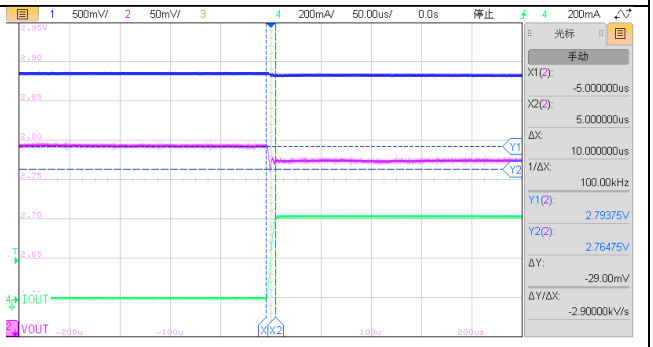

DVO2 IOUT=1mA to 1.2A




DVO2 IOUT=1.2A to 1mA

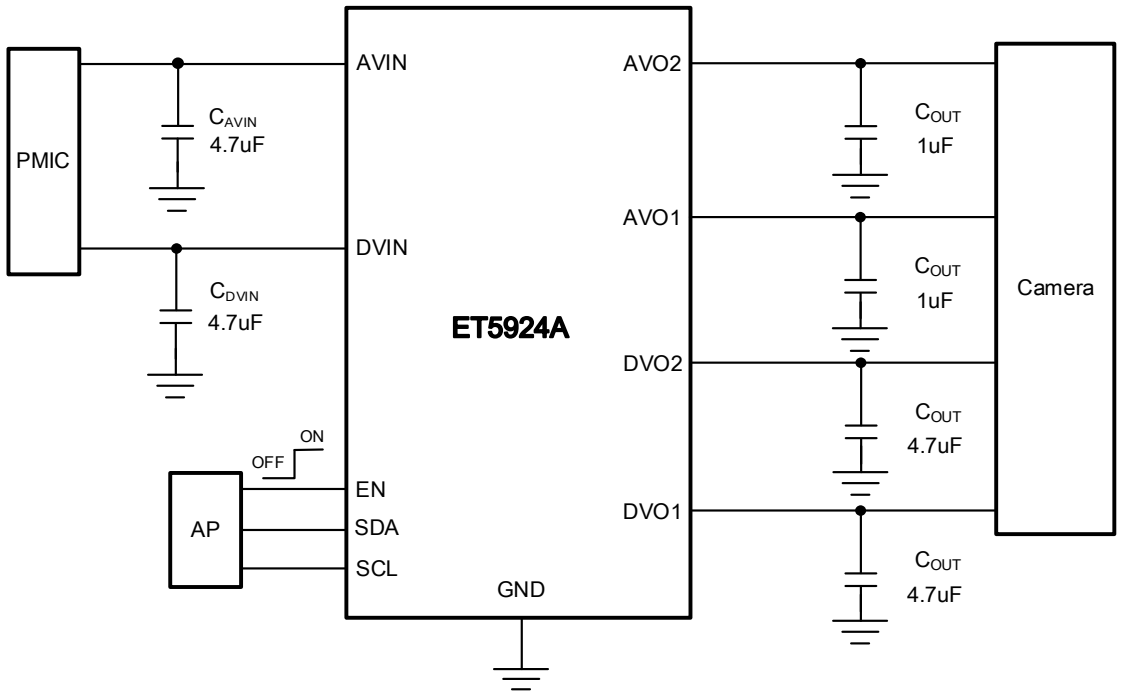



AVO1/2 IOUT=1mA to 400mA

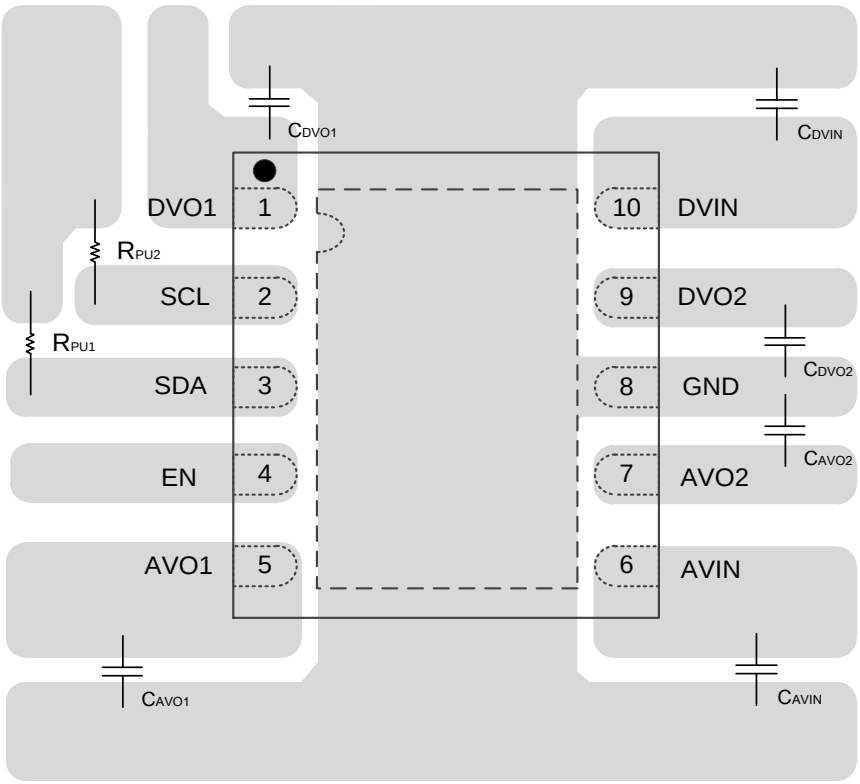



AVO1/2 IOUT=400mA to 1mA

## Application Circuits

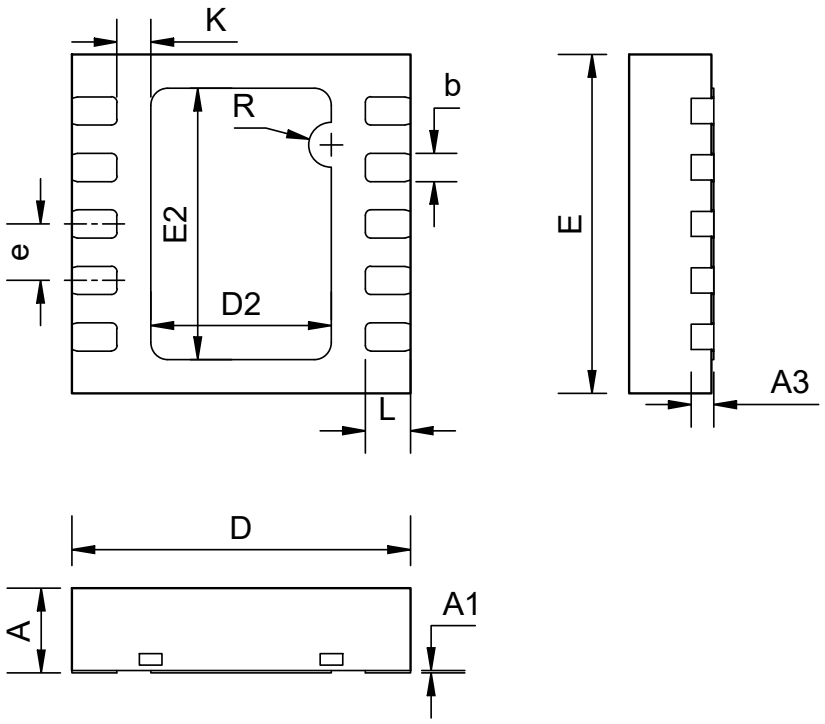



## Recommended PCB Layout



## Package Dimension

DFN10(2×2)

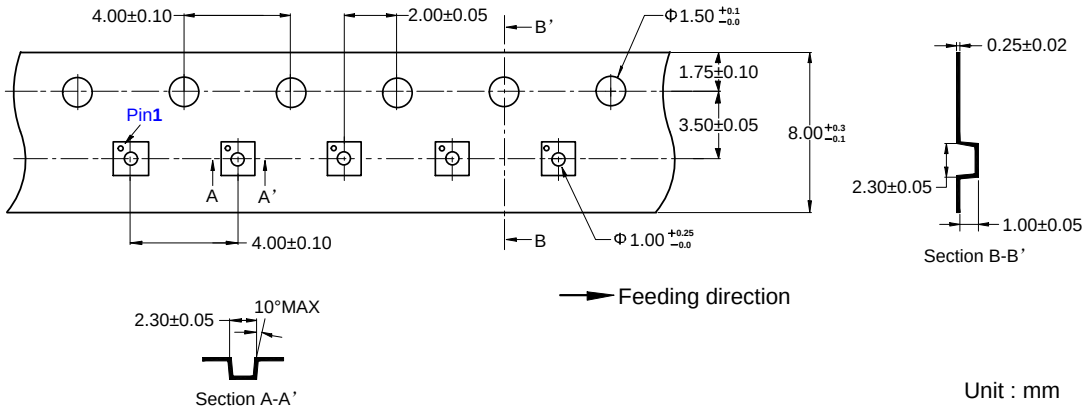



COMMON DIMENSIONS

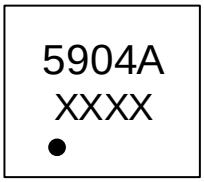
(UNITS OF MEASURE = MILLIMETER)

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20REF | |
| b | 0.15 | 0.20 | 0.25 |
| D | 1.90 | 2.00 | 2.10 |
| E | 1.90 | 2.00 | 2.10 |
| D2 | 0.80 | 0.90 | 1.00 |
| E2 | 1.30 | 1.40 | 1.50 |
| e | 0.30 | 0.40 | 0.50 |
| K | 0.15 | 0.25 | 0.35 |
| L | 0.25 | 0.30 | 0.35 |
| R | | 0.10REF | |

## Tape Information




## Marking




5904A = Part Number

XXXX = Tracking Number

## Revision History and Checking Table

| Version | Date | Revision Item | Modifier | Function & Spec Checking | Package & Tape Checking |
|---|---|---|---|---|---|
| 0 | 2019-10-22 | Preliminary Version | Liu Yi Guo | Liu Yi Guo | Zhu Jun Li |
| 1.0 | 2020-01-02 | Original Version | Liu Yi Guo | Liu Yi Guo | Liu Jia Ying |
| 1.1 | 2020-03-13 | Documents check and formalize | Shib | Shib | Liujy |
| 1.2 | 2020-03-25 | Update $V_{I2CL}$ / $T_{ON\_DVOx}$ /$I_{SHORT\_AVOx}$ /$I_{LMT\_AVOx}$ | Liu Yi Guo | Liu Yi Guo | Liu Jia Ying |
| 1.3 | 2023-02-15 | Update Test date | Yang Zhi | Yang Zhi | Yang Zhi |
| 1.4 | 2024-04-10 | Add Characteristic Curve | Yang Xiao Xu | Yang Zhi | Yang Zhi |
| 1.5 | 2024-06-19 | Update Characteristic Curve | Yang Xiao Xu | Yang Xiao Xu | Liu Jia Ying |
| 1.6 | 2025-01-07 | Update CDVO1/2 range and DVIN range | Yang Xiao Xu | Yang Xiao Xu | Liu Jia Ying |