Slew Rate Controlled Load Switch

General Description

The ET3140 advanced load management switches target applications requiring a highly integrated solution it disconnects loads powered from DC Power Rail (<5.5V) with stringent off-state current targets. Each switch consists of slew-rate controlled low-impedance MOSFET Switch (40mΩ Typ) and other integrated analog features. The slew-rate controlled turn-on characteristic prevents inrush-current and the resulting excessive voltage droop on power rails.

These devices have exceptionally low off-state current drain (<1μA max) which facilitate compliance in very low stand-by power applications. The input voltage range operates from 1.2V to 5.5V DC to fulfill a wide range of applications in consumer, optical, medical, storage, portable, and industrial device power management. Switch control is managed by a logic input (Active HIGH) capable of interfacing directly with low voltage control signal/GPIO with no external pull-down resistor required.

The device is packaged in advanced full-Green FCQFN4 1mm*1mm.

Features

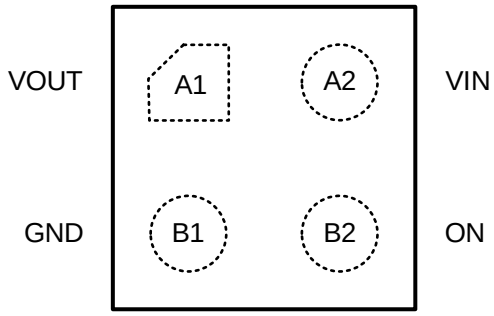
- 1.2V to 5.5V Input Voltage Operating Range
- Typical $R_{DS(ON)}$:
  - -- 40mΩ at V_{IN}=5.5V
  - -- 50mΩ at V_{IN}=3.3V
  - -- 90mΩ at V_{IN}=1.8V
  - -- 180mΩ at V_{IN}=1.2V
- Slew Rate/Inrush Control with t_R: 60us (Typ)
- 2.2A Maximum Continuous Current Capability
- Low<1μA Off Switch Current
- ESD Protected: Above 8kV HBM, 2kV CDM
- Part No. and Package

Part No.	Package	MSL
ET3140	FCQFN4 1mm*1mm*0.55mm	Level 1

Application

- HDD, Storage, and Solid State Memory Devices
- Portable Media Devices, Laptop & MID
- GPS and Navigation Equipment
- Industrial Handheld and Enterprise Equipment

Pin Configuration



Top view Figure 1.

Pin Function

Pin	Name	Description
A1	VOUT	Switch Output
A2	VIN	Supply Input: Input to the Power Switch
B1	GND	Ground
B2	ON	ON/OFF Control, Active HIGH Compatible

Block Diagram

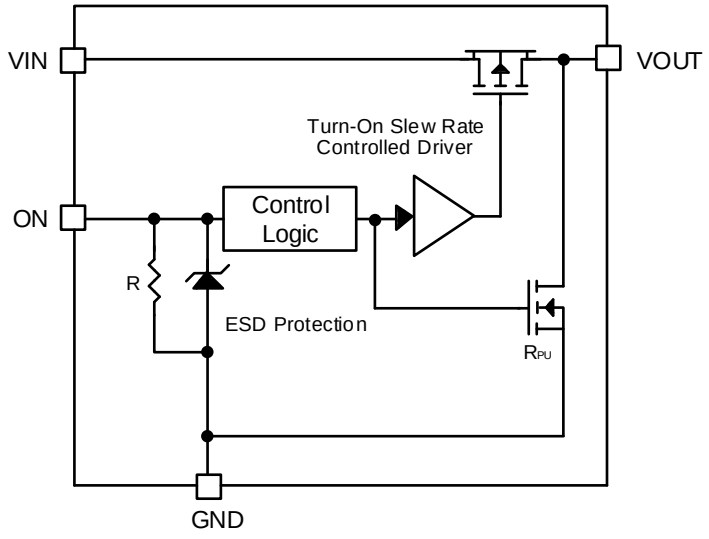


Figure 2. Functional Block Diagram

Functional Description

The ET3140 is low-R_{ON} P-channel load switches with controlled turn-on. The core of each device is a 40mΩ P-channel MOSFET and controller capable of functioning over a wide input operating range of 1.2V～5.5V. The ON pin, an active HIGH GIOP/CMOS-compatible input, controls the state of the switch.

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into a discharged load capacitor or short-circuit, a capacitor must be placed between the VIN and GND pins. A 1μF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher-value C_{IN} can be used to reduce the voltage drop in higher-current applications.

Output Capacitor

A 0.1μF capacitor, C_{OUT}, should be placed between the VOUT and GND pins. This capacitor prevents parasitic board inductance from forcing VOUT below GND when the switch is on. C_{IN} greater than C_{OUT} is highly recommended. C_{OUT} greater than C_{IN} can cause VOUT to exceed VIN when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN.

Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effect that parasitic trace inductance may have on normal and short-circuit operation. Using wide traces or large copper planes for all pins (VIN, VOUT, ON, and GND) helps minimize the parasitic electrical effects along with minimizing the case ambient thermal impedance.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min	Max	Unit
V_{IN}	V_{IN} to GND	-0.3	6.5	V
V_{ON}	V_{ON} to GND	-0.3	6.5	V
V_{OUT}	V_{OUT} to GND	-0.3	6.5	V
I_{SW}	Maximum Continuous Switch Current		2.2	A
P_D	Power Dissipation at T_A=25°C		1	W
θ_{JA}	Thermal Resistance, Junction-to-Ambient		85	°C/W
T_{STG}	Storage Junction Temperature	-65	+150	°C
T_J	Operating Junction Temperature	-40	+150	°C
V_{ESD}	Human Body Model, JESD22-A114	8		kV
	Charged Device Model, JESD22-C101	2		

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	1.2	5.5	V
T_A	Ambient Operating Temperature	-40	+85	°C

Electrical Characteristics

Unless otherwise noted, V_{IN}=1.2 to 5.5V, T_A=-40 to +85°C; typical values are at V_{IN}=3.3V and T_A=25°C.

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
Basic Operation						
V_{IN}	Input Voltage		1.2		5.5	V
$I_{Q(OFF)}$	Off Supply Current	V_{ON}=GND, V_{OUT}=Open		0.1	1.0	μA
I_{SD}	Shutdown Current	V_{ON}=GND, V_{OUT}=GND		0.1	1.0	μA
I_Q	Quiescent Current	I_{OUT}=0mA		0.5	1.2	μA
R_{ON}	On-Resistance	V_{IN}=5.5V,I_{OUT}=200mA ,T_A=25°C		40		mΩ
		V_{IN}=3.3V,I_{OUT}=200mA ,T_A=25°C		50		
		V_{IN}=1.8V,I_{OUT}=200mA ,T_A=25°C		90		
		V_{IN}=1.2V,I_{OUT}=200mA ,T_A=25°C		180		
V_{IH}	ON Input Logic High Voltage	V_{IN}=1.2V to 5.5V	1.0			V
V_{IL}	ON Input Logic Low Voltage	V_{IN}=1.2V to 5.5V			0.55	V
R_{ON_PD}	Pull-Down Resistance at ON pin	T_A=25°C		7.0		MΩ
R_{PD}	OUT pin Discharge Resistance	V_{IN}= 3.3V, EN = 0V, V_{OUT}=1V, T_A=25°C		60		Ω
I_{ON}	On Input Leakage	V_{ON}=V_{IN} or GND，T_A=25°C		0.5	1.0	uA
Dynamic Characteristics: See Definitions Below						
t_{DON}	Turn-On Delay(1,2)	V_{IN} =3.3V, R_L=10Ω, C_L=0.1μF, T_A=25°C		40		us
t_R	V_{OUT} Rise Time(1.2)			60		us
t_{ON}	Turn-On Time(1,3)			100		us
t_{DOFF}	Turn-Off Delay(1,2)	V_{IN} =3.3V, R_L=10Ω, C_L=0.1μF, T_A=25°C		5.5		us
t_F	V_{OUT} Fall Time(1,2)			1.3		us
t_{OFF}	Turn-Off Time(1,4)			6.8		us

Notes:

1. This parameter is guaranteed by design and characterization; not production tested.
2. t_{DON}/t_{DOFF}/t_R/t_F are defined in Figure 3.
3. t_{ON}=t_R + t_{DON}
4. t_{OFF}=t_F + t_{DOFF}

Timing Diagram

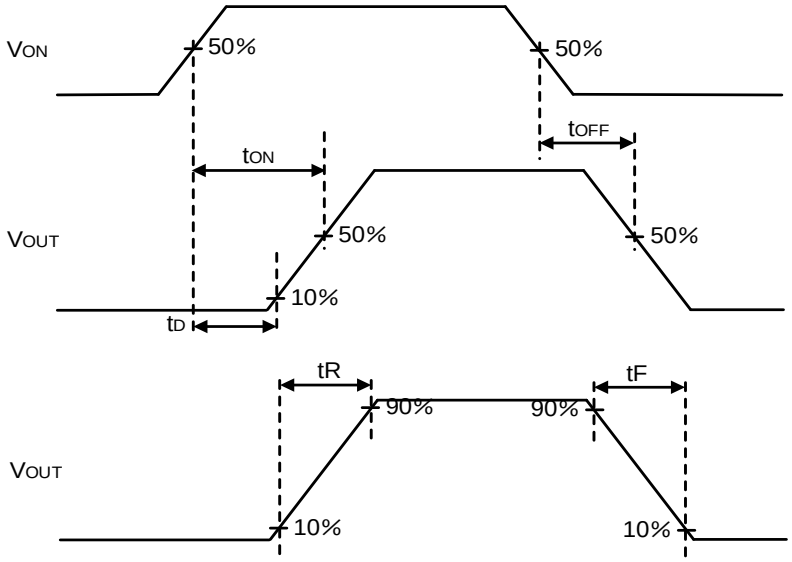


Figure 3.

Application Circuits

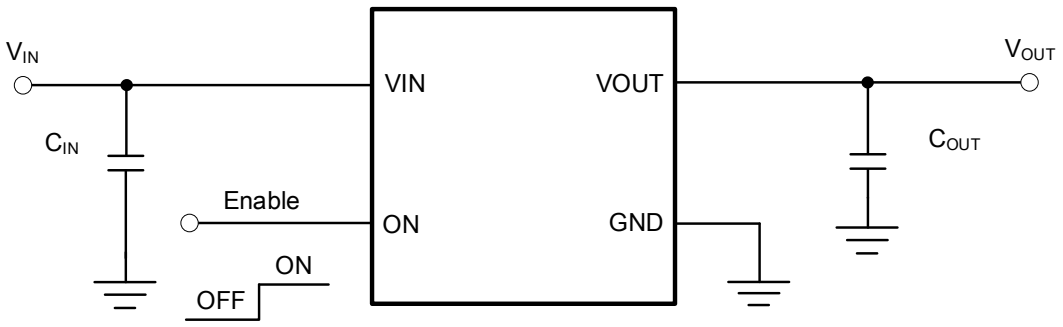
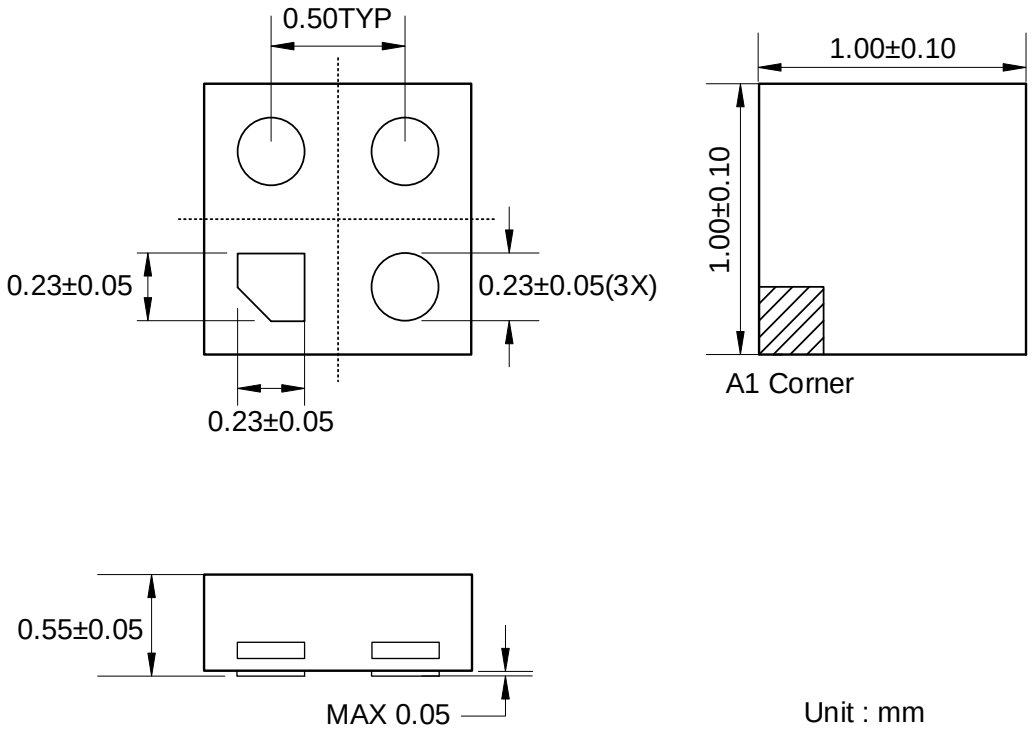


Figure 4. Typical Application

*：This electric circuit only supplies for reference.

Package Dimension

FCQFN4 1mm*1mm*0.55mm



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2019-04-28	Preliminary Version	Luh	Luh	Zhujl
1.0	2020-05-21	Released Version	Luh	Luh	Liujy
1.1	2025-7-8	Update type	Shib	Luh	Liujy