24-bit, 96 kHz Stereo D/A Converter

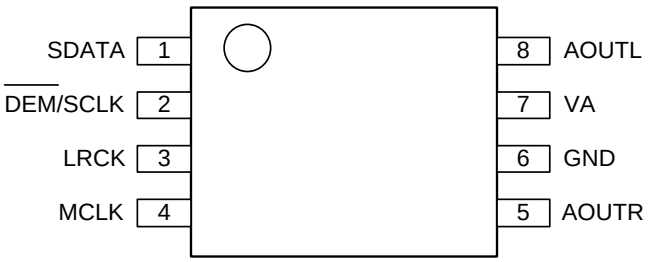
General Description

The ET4334M is a complete stereo digital-to-analog output systems including interpolation, 1-bit D/A conversion and output analog filtering . The ET4334M support all major audio data interface formats, and the individual devices differ only in the supported interface format. The ET4334M is based on ∑−△ modulation, where the modulator output controls the reference voltage input to an ultra-linear analog low-pass filter. This architecture allows for infinite adjustment of sample rate between 2 kHz and 100 kHz simply by changing the master clock frequency.

Features

- Complete Stereo 24-Bit DAC System: Interpolation, D/A, Output Analog Filtering
- 96dB Dynamic Range, -88dB THD+N
- Low Clock Jitter Sensitivity
- Single +5V Power Supply
- Filtered Line Level Outputs
- On-Chip Digital De-emphasis
- Package is SOP8 (ET4334M)

Pin Configuration

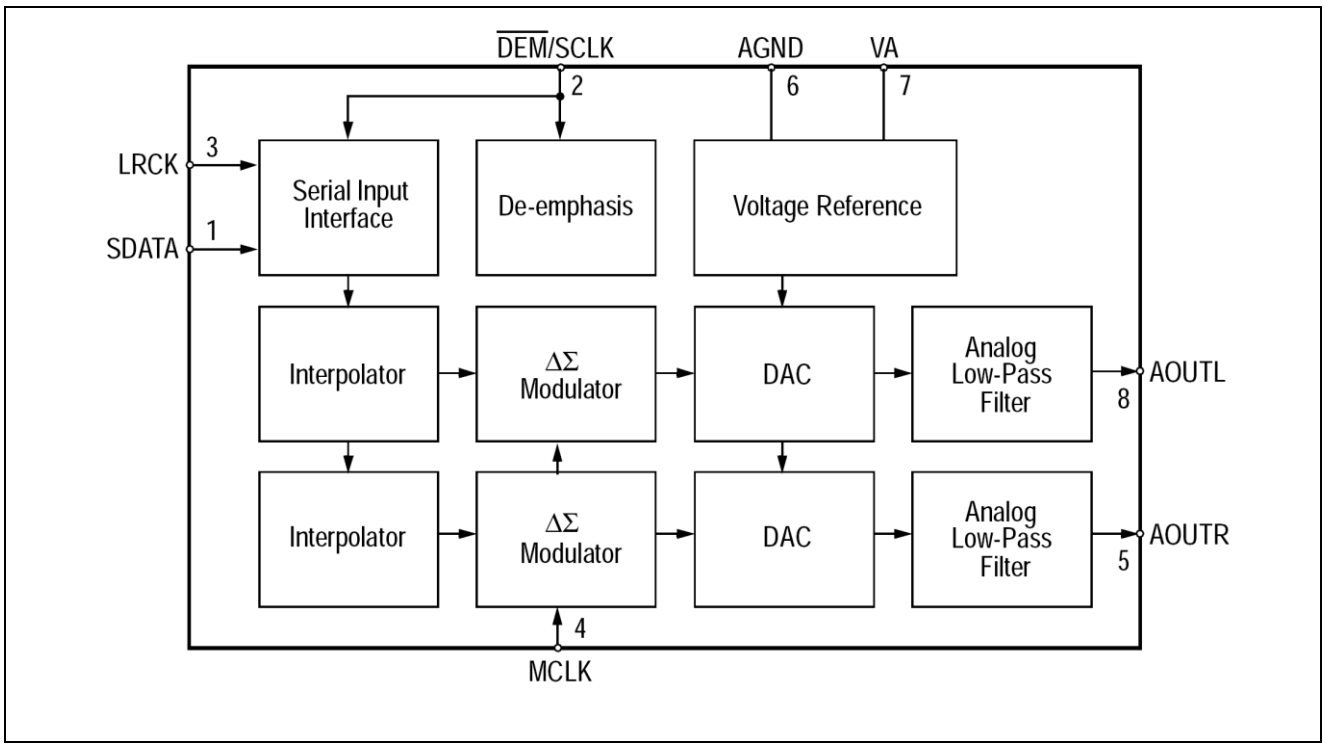


(ET4334M) Top View

Pin Function

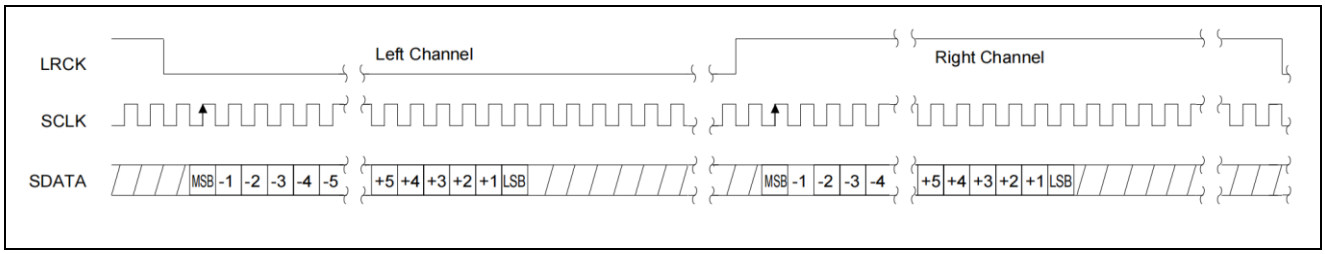
No.	Pin Name	I/O	Pin Function and Description
1	SDATA	I	Serial Audio Data Input.
2	$\overline{\text{DEM}}$/SCLK	I	De-Emphasis/External Serial Clock Input.
3	LRCK	I	Left/Right Clock.
4	MCLK	I	Master Clock.
5	AOUTR	O	Analog Right Channel Output.
6	AGND	I	Analog Ground.
7	VA	I	Analog Power.
8	AOUT	O	Analog Left Channel Output.

Block Diagram



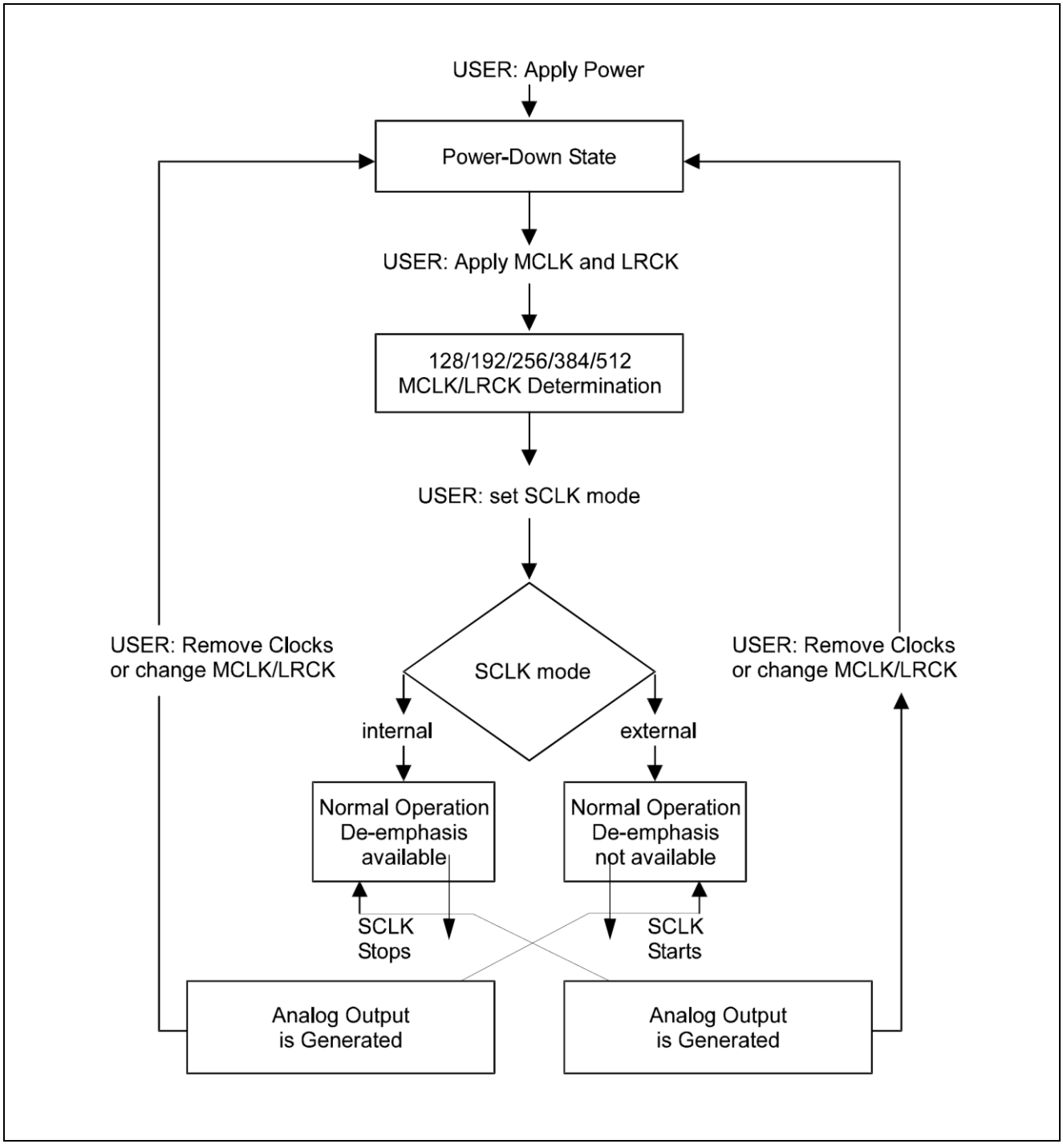
Functions Description

Data Format (I^2S)



Internal SCLK Mode	External SCLK Mode
I^2S, 16-bit data and INT SCLK = 32 Fs if MCLK/LRCK = 512, 256 or 128 I^2S, Up to 24-bit data and INT SCLK = 48 Fs If MCLK/LRCK = 384 or 192	I^2S，up to 24-Bit Data Data Valid on Rising Edge of SCLK

Initialization and Power-Down Sequence



Absolute Maximum Ratings

Parameters	Symbol	Min.	Max	Units
DC Power Supply	V_A	-0.3	6.0	V
Input Current, Any Pin Except Supplies	I_{IND}	-	±10	mA
Digital Input Voltage	V_{IND}	-0.3	V_A+0.4	V
Storage Temperature	T_{STG}	-65	150	˚C

Recommended Operation Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units
DC Power Supply	V_A	4.75	5.0	5.5	V
Ambient Operating Temperature	T_A	-40		85	˚C

Electrical Characteristics

Analog Characteristics

Parameter			Symbol	Base-rate Mode			High-rate Mode			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Dynamic Range	18 to 24bit	Unweighted		85	93	-	-	90	-	dB
		A-weighted		88	96	-	88	96	-	
	16bit	Unweighted		83	91	-	-	88	-	
		A-weighted		86	94	-	86	94	-	
Total Harmonic Distortion + Noise	18 to 24bit	0dB	THD+N	-	-88	-82	-	-88	-82	dB
		-20dB		-	-73	-65	-	-70	-62	
		-60dB		-	-33	-25	-	-30	-22	
	16bit	0dB		-	-86	-70	-	-86	-80	dB
		-20dB		-	-71	-63	-	-68	-60	
		-60dB		-	-31	-23	-	-28	-20	
Inter Channel Isolation		1kHz		-	94	-	-	95	-	dB
Combined Digital and On-chip Analog Filter Response										
Pass band	To -0.5dB corner			0	-	.4780	-	-	-	Fs
	To -0.1dB corner			-	-	-	0	-	.4650	
	To -3dB corner			0	-	.4996			.4982	
Frequency Response 10 to 20kHz				-.01	-	+.08	-.05	-	+.2	dB
Pass Band Ripple				-	-	±.08	-	-	±.2	dB
Stop Band				.5465	-	-	.5770	-	-	Fs
Stop Band Attenuation				50	-	-	55	-	-	dB
Group Delay			tgd	-	9/Fs	-	-	4/Fs	-	s
Passband Group Delay Deviation		0 to 40 kHz		-	±0.36/Fs	-	-	±1.39/Fs	-	s
De-emphasis Error	Fs=32 kHz			-	-	+1.5/+0				dB
	Fs=44. 1kHz			-	-	+.05/-.25				
	Fs=48kHz			-	-	-.2/-.4				

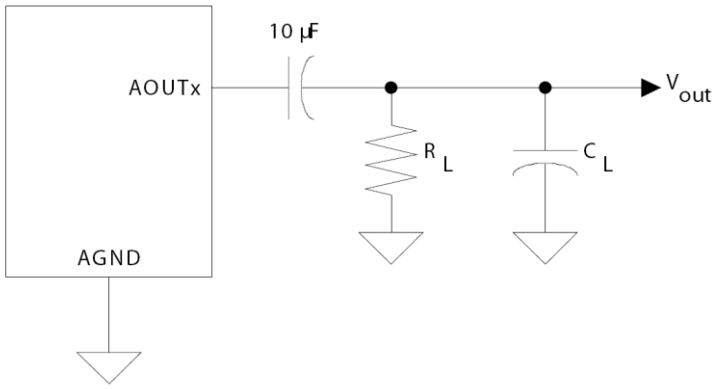
Analog Characteristics (Continued)

Parameters	Symbol	Min.	Typ.	Max.	Units
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	0.4	dB
Gain Error		-	±5	-	%
Gain Drift		-	100	-	ppm/℃
Analog Output					
Full Scale Output Voltage		3.25	3.5	3.75	V_{PP}
Quiescent Voltage	V_Q	-	2.2	-	V_{DC}
Max AC-Load Resistance	R_L	-	3	-	kΩ
Max Load Capacitance	C_L	-	100	-	pF

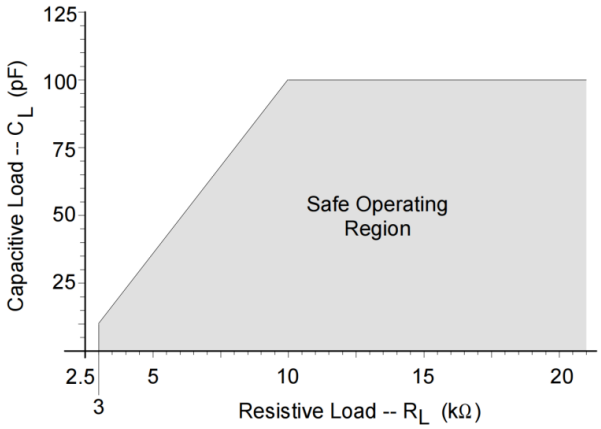
Power and Thermal Characteristics

Parameters		Symbol	Min.	Typ.	Max.	Units
Power Supplies						
Power Supply Current	normal operation	I_A	-	15	19	mA
	power-down state	I_A	-	40	-	μA
Power Dissipation	normal operation		-	75	104	mW
	power-down state		-	0.2	-	mW
Package Thermal Resistance		θ_{JA}	-	110	-	℃/W
Power Supply Rejection Ratio	1kHz	PSRR	-	79	-	dB

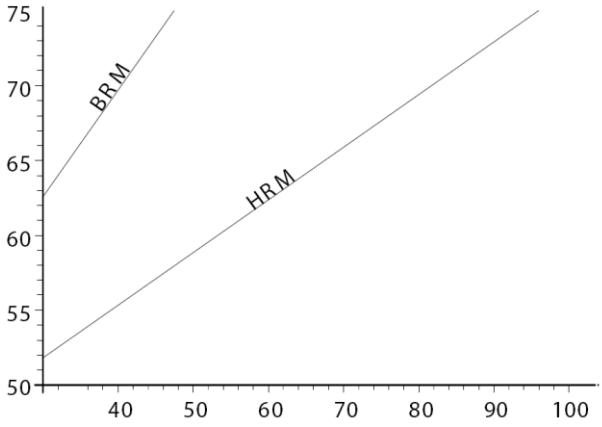
Output Test Load



Maximum Loading



Power vs. Sample Rate



Electrical Characteristics

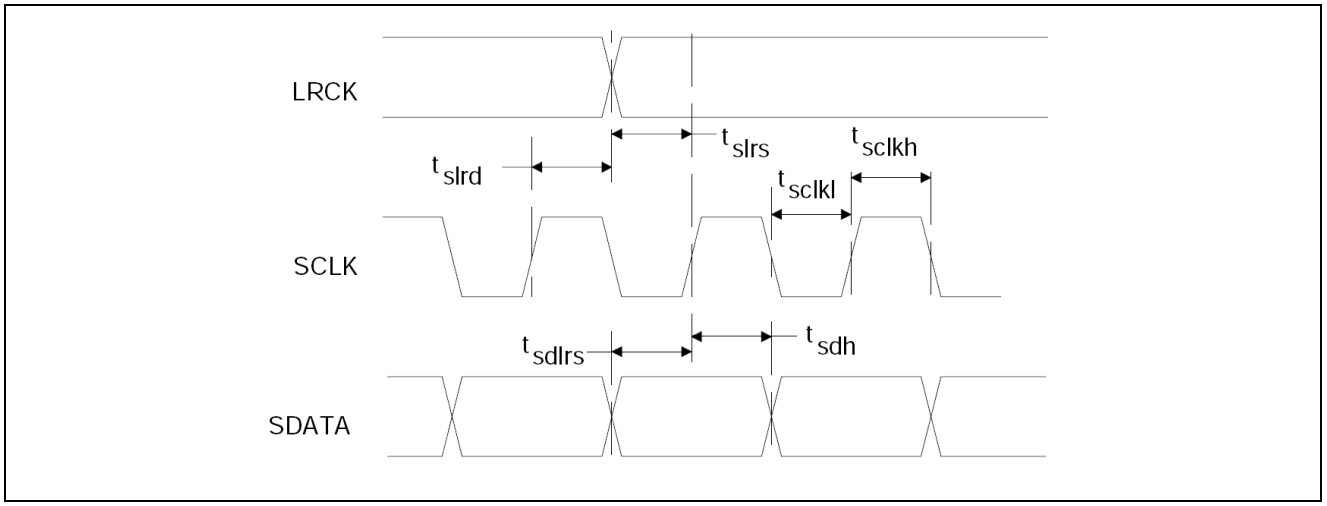
Digital Characteristics（T_A=25℃，V_A=4.75～5.5V）

Parameters	Symbol	Min.	Typ.	Max.	Units
High-Level Input Voltage	V_{IH}	60%VA			V
Low-Level Input Voltage	V_{IL}			30%VA	V
Input Leakage Current	I_{IN}		100		μA
Input Capacitance	C_{IN}	3.25	3.5	3.75	pF

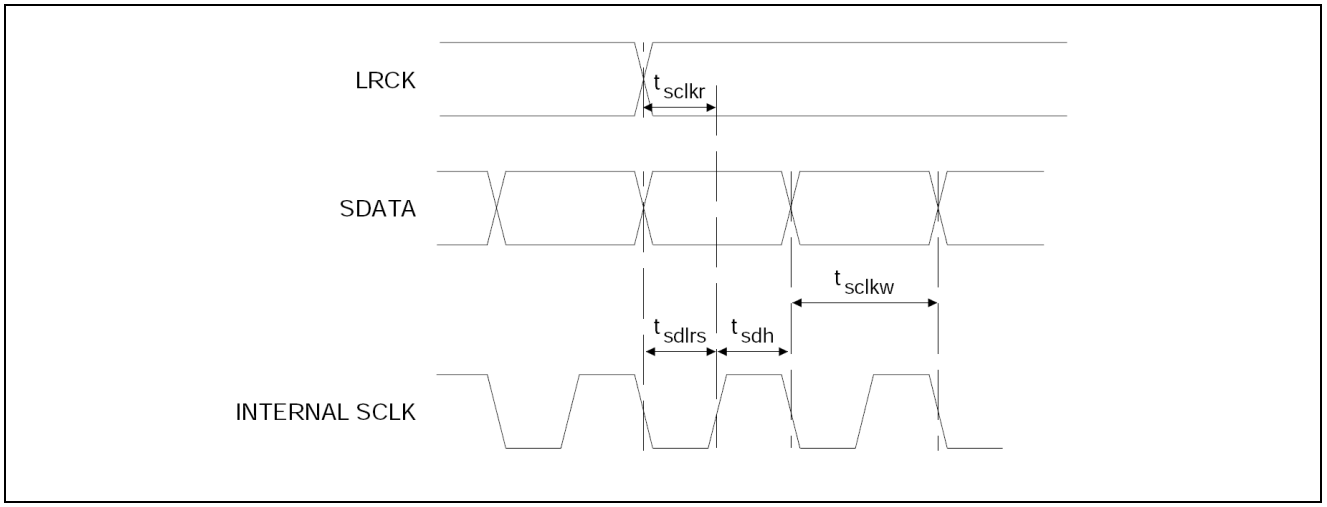
Switching Characteristics (T_A =-40℃～85℃, V_A=4.75～5.5V; Input: Logic=0V, Logic1=V_A, C_L=20pF)

Parameters		Symbol	Min.	Typ.	Max.	Units
Input Sample Rate		Fs	2	-	100	kHz
MCLK Pulse Width High	MCLK/LRCK=512		10	-	1000	ns
MCLK Pulse Width Low	MCLK/LRCK=512		10	-	1000	ns
MCLK Pulse Width High	MCLK/LRCK=384/192		21	-	1000	ns
MCLK Pulse Width Low	MCLK/LRCK=384/192		21	-	1000	ns
MCLK Pulse Width High	MCLK/LRCK=256/128		31	-	1000	ns
MCLK Pulse Width Low	MCLK/LRCK=256/128		31	-	1000	ns
External SCLK Mode						
LRCK Duty Cycle (External SCLK only)			40	50	60	%
SCLK Pulse Width Low		t_{sclkl}	20	-	-	ns
SCLK Pulse Width High		t_{sclkh}	20	-	-	ns
SCLK Period	MCLK/LRCK=512,256/384	t_{sclkw}	$\frac{1}{(128)Fs}$	-	-	ns
SCLK Period	MCLK/LRCK=128/192	t_{sclkw}	$\frac{1}{(64)Fs}$	-	-	ns
SCLK rising to LRCK edge delay		t_{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time		t_{slrs}	20	-	-	ns
SDATA valid to SCLK rising setup time		t_{sdlrs}	20	-	-	ns
SCLK rising to SDATA hold time		t_{sdh}	20	-	-	ns
Internal SCLK Mode						
LRCK Duty Cycle (Internal SCLK only)			-	50	-	%
SCLK Period		t_{sclkw}	$\frac{1}{SCLK}$	--	-	ns
SCLK rising to LRCK edge		t_{sclkr}	-	$\frac{tsclkw1}{2}$	-	μs
SDATA valid to SCLK rising setup time		t_{sdlrs}	$\frac{1}{(512)Fs}+10$	-	-	ns
SCLK rising to SDATA hold time MCLK/LRCK=512,256/128		t_{sdh}	$\frac{1}{(512)Fs}+15$	-	-	ns
SCLK rising to SDATA hold time MCLK/LRCK=384/192		t_{sdh}	$\frac{1}{(384)Fs}+15$	-	-	ns

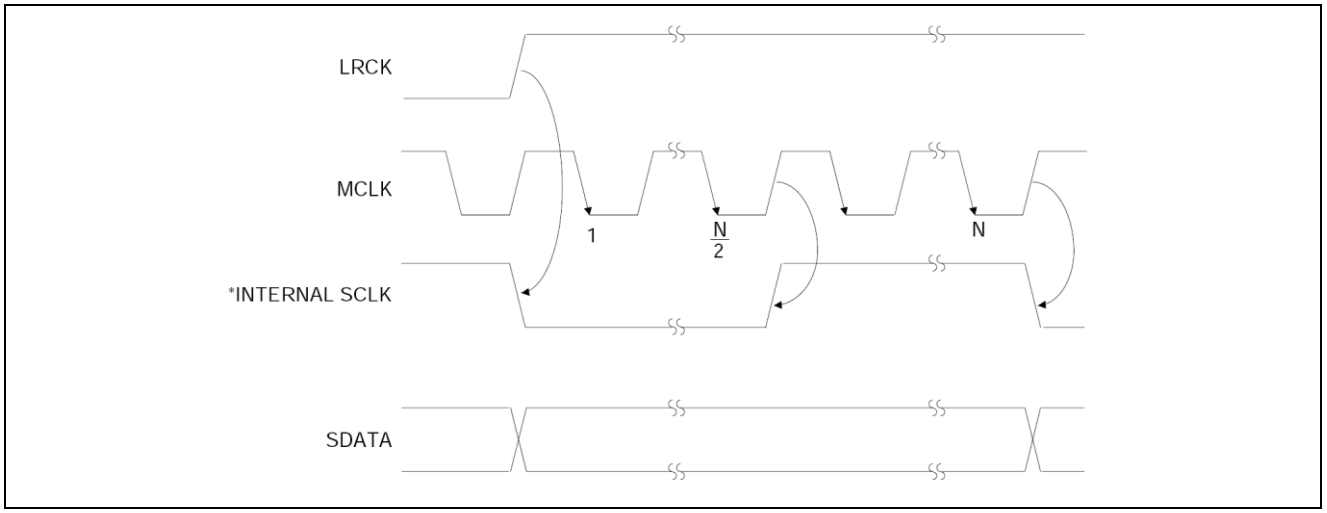
External Serial Mode Input Timing



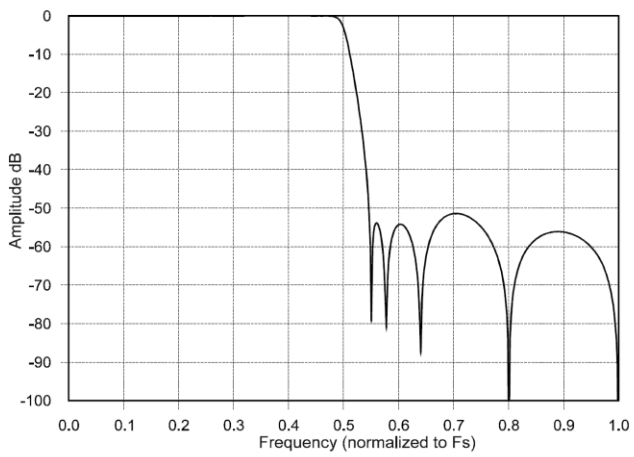
Internal Serial Mode Input Timing



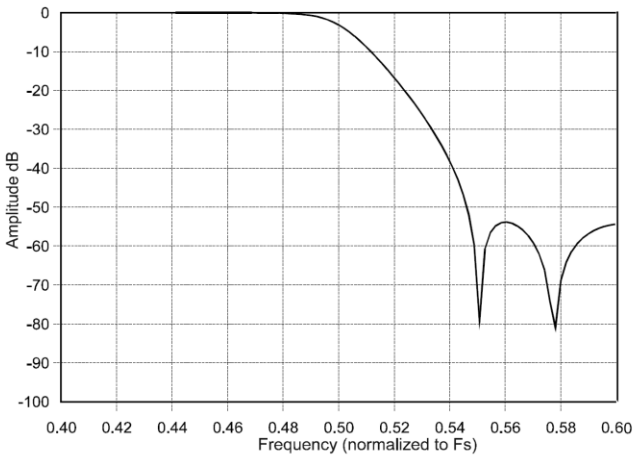
Internal Serial Clock Generation



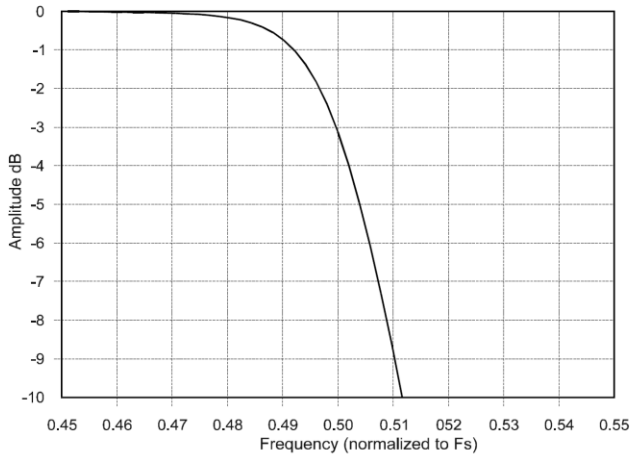
Over Base-rate Frequency Response



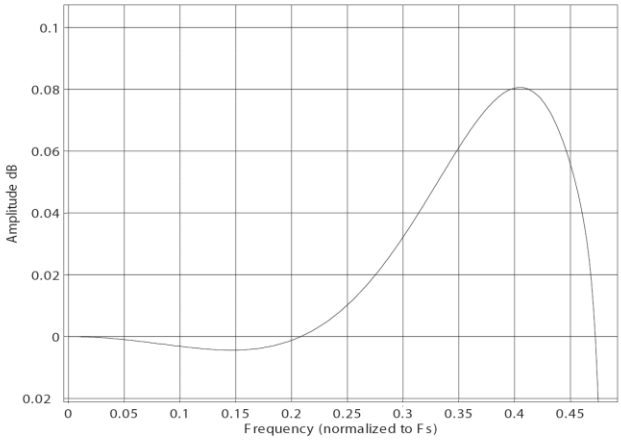
Stopband Rejection



Transition Band

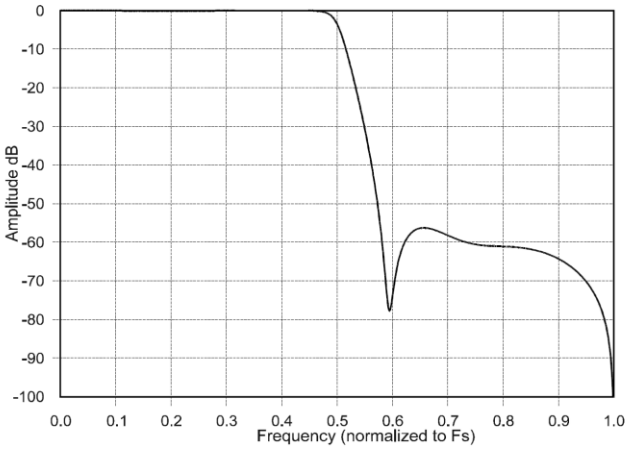


Transition Band

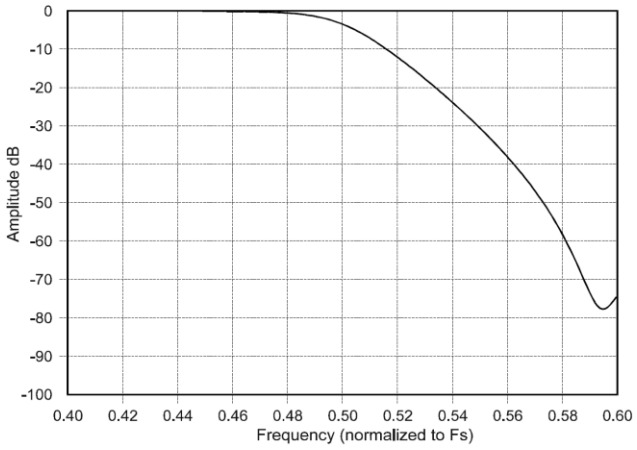


Passband Ripple

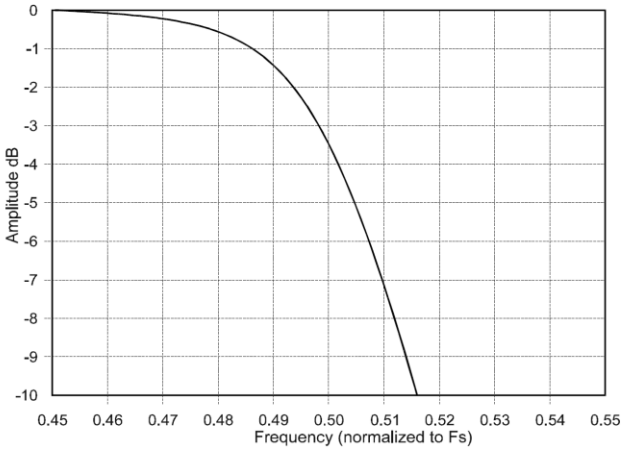
Over High-rate Frequency Response



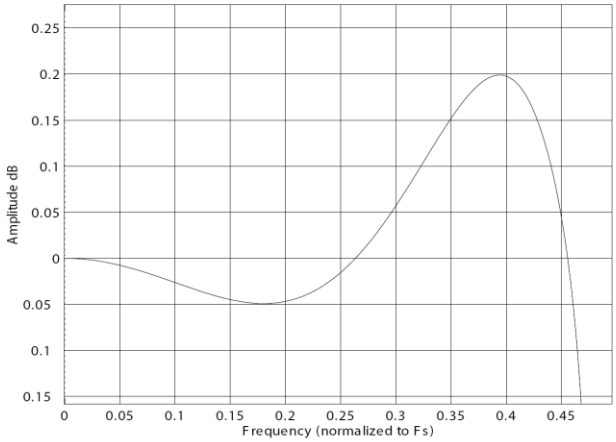
Stopband Rejection



Transition Band

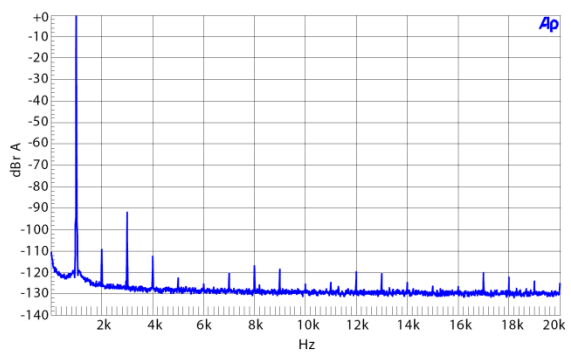


Transition Band



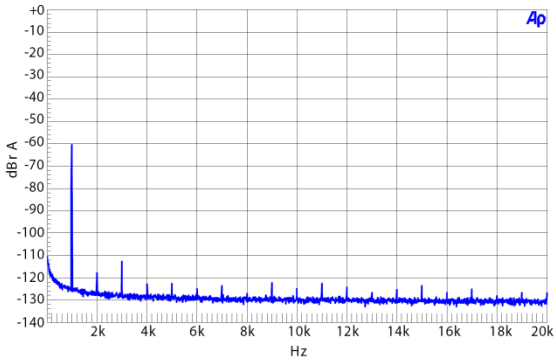
Passband Ripple

Base-rate Mode Performance Plots



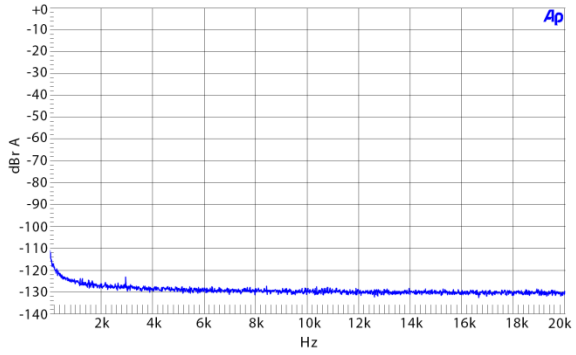
(16k FFT of a 1 kHz input signal)

0 dBFS FFT (BRM)



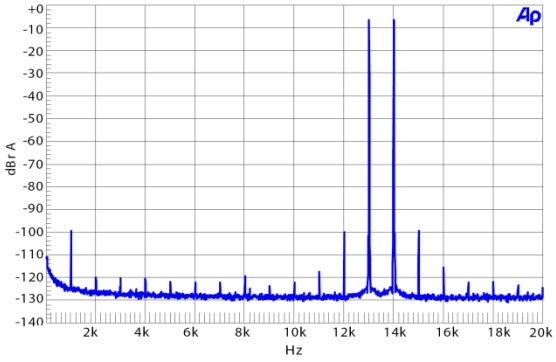
(16k FFT of a 1 kHz input signal)

-60 dBFS FFT (BRM)



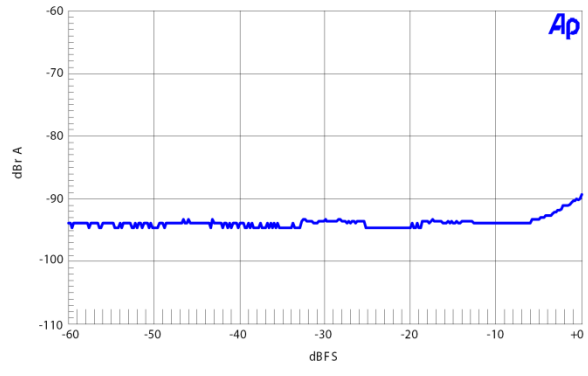
(16k FFT with no input signal)

Idle Channel Noise FFT (BRM)



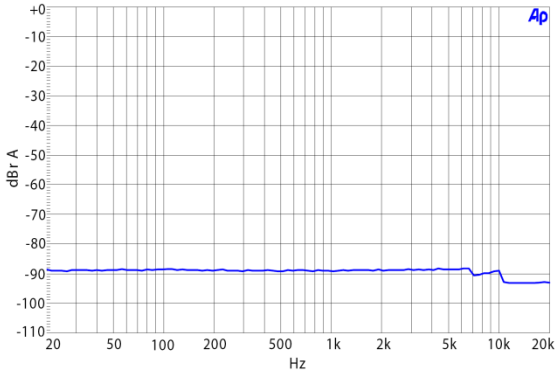
(16k FFT of intermodulation distortion using 13 kHz and 14 kHz input signals)

Twin Tone IMD FFT (BRM)



(THD+N plots measured using a 1kHz 24-bit dithered input signal)

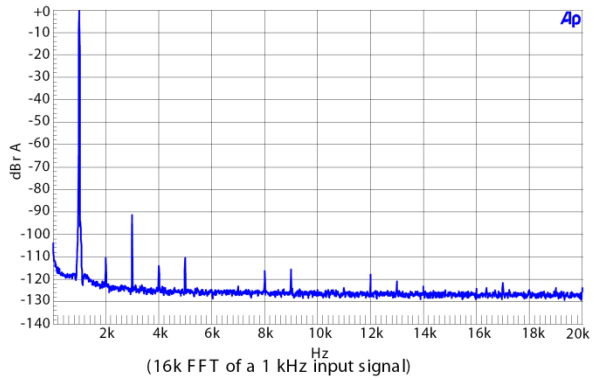
THD+N vs. Amplitude (BRM)



(THD+N plots measured using a 1kHz 24-bit dithered input signal)

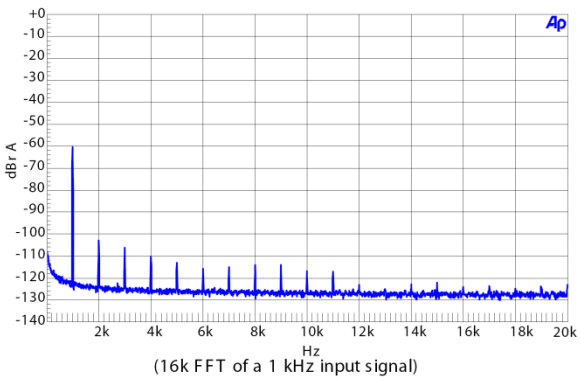
THD+N vs. Frequency (BRM)

High-rate Mode Performance Plots



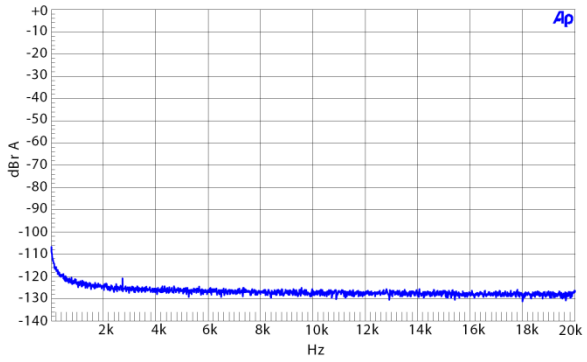
(16k FFT of a 1 kHz input signal)

0 dBFS FFT (HRM)



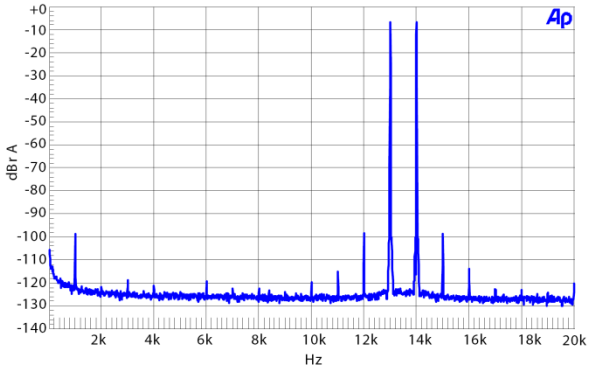
(16k FFT of a 1 kHz input signal)

-60 dBFS FFT (HRM)



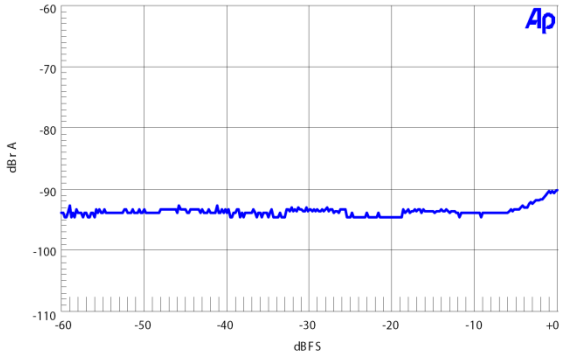
(16k FFT with no input signal)

Idle Channel Noise FFT (HRM)



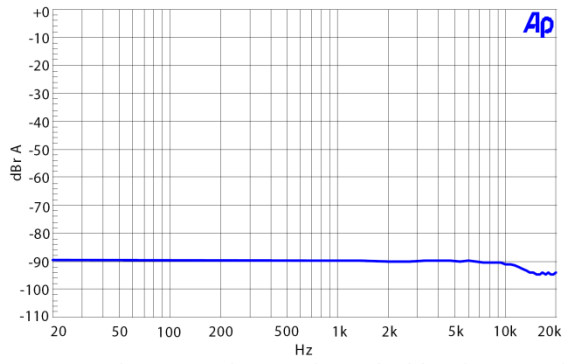
(16k FFT of intermodulation distortion using 13 kHz and 14 kHz input signals)

Twin Tone IMD FFT (HRM)



(THD+N plots measured using a 1kHz 24-bit dithered input signal)

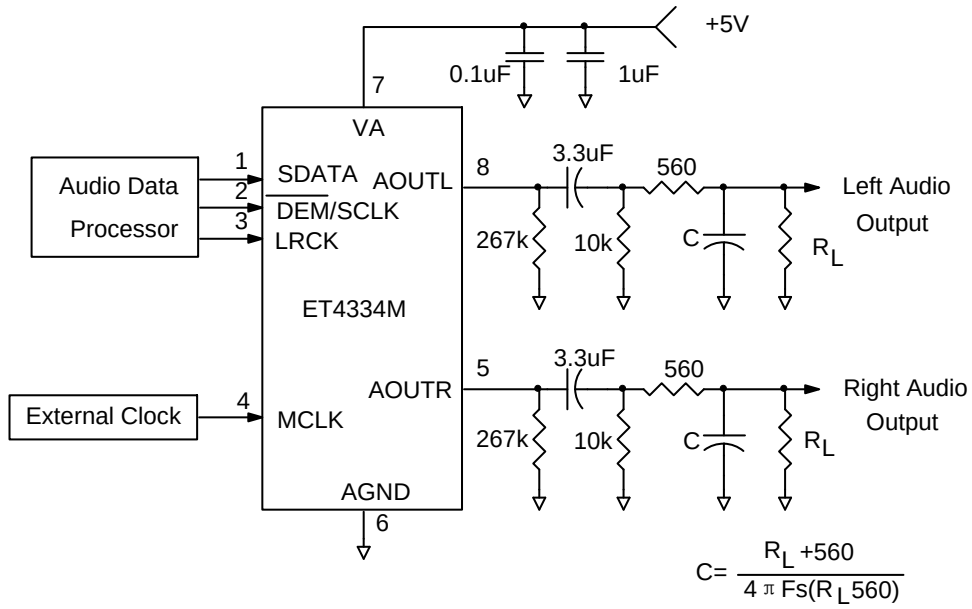
THD+N vs. Amplitude (HRM)



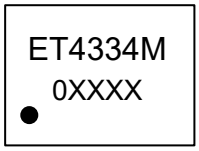
(THD+N plots measured using a 1kHz 24-bit dithered input signal)

THD+N vs. Frequency (HRM)

Application Circuits



Marking Information

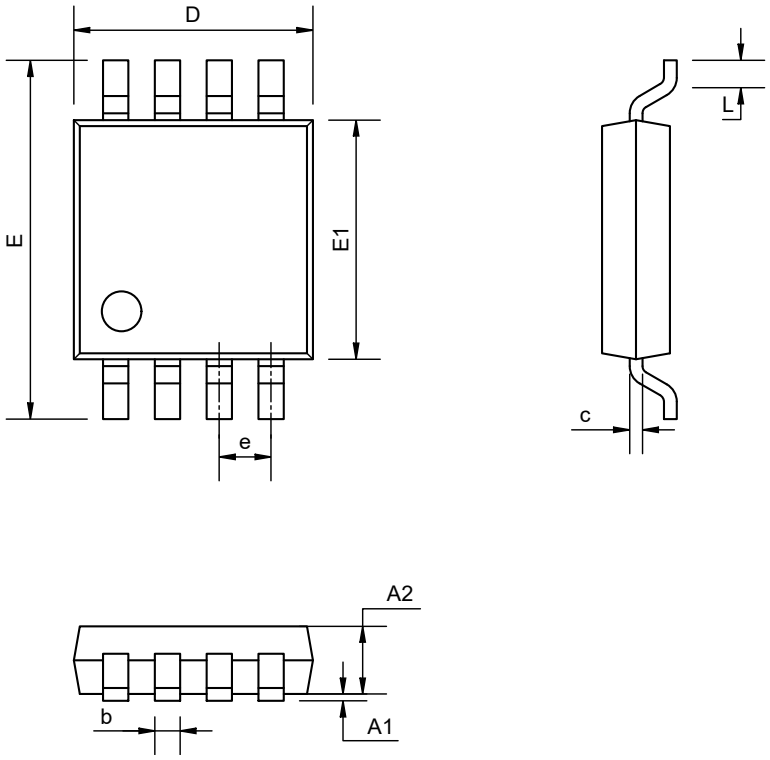


ET4334M - Part Number

0XXXX - Tracking Number

Package Dimensions

SOP8



Dimensions Table (Units:mm)

Symbol	Min	Typ	Max
A1	0.10	0.20	0.30
A2	1.35	1.45	1.55
b		0.40 BSC	
c		0.20 REF	
D	4.76	4.86	4.96
E	5.84	6.04	6.24
E1	3.85	3.95	4.05
e		1.27 BSC	
L	0.35	0.55	0.75

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2016-1-14	Initial Version	Wanggp	Wanggp	Zhujl
1.1	2023-3-08	Updated form	Shi bo	Wanggp	Zhu Jun Li