Spectral Data Acquisition IC with Audio 7 Band Graphic Equalizer

General Description

ET7208 is a spectral data acquisition circuit IC with audio 7 band graphic equalizer. In the audio synchronization mode, 20Hz ~ 20KHz input audio signal is subdivided into seven bands through the built-in band-pass filter, and the average range value of each of the different frequency bands is converted into the corresponding digital signal through the built-in high-precision 8Bit ADC, while the total average range value of the signal sources is calculated. In this mode, different frequency range value of the audio signals can be read out by MCU.

Feature

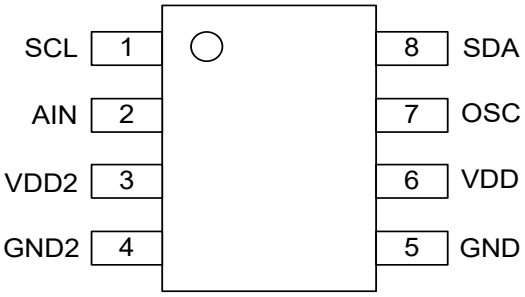
- 2.7V to 5.5V Operation Voltage
- -18dB~+18dB audio input gain adjustable
- 7 band graphic equalizer and a volume data acquisition
- Built-in 8bit ADC
- I^2C bus interface
- Digital signals can be read from ADC through the I^2C interface
- Part No. and Package

Part No.	Package	MSL
ET7208	SOP8	Level 3
ET7208Y	DFN8 (3mm × 3mm)	Level 1

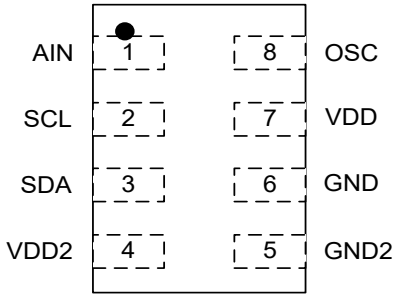
Applications

- Portable Stereos
- Car Stereos
- Hi-Fi Stereos
- Spectrum Analyzers

Pin Configuration



SOP8(ET7208)



DFN8(ET7208Y)

TOP VIEW

Figure 1. Pin Configuration

Pin Function

Pin Number		Pin Name	I/O	Description
SOP8	DFN8			
1	2	SCL	I	clock input for I²C communication
2	1	AIN	I	Audio signal input
3	4	VDD2	-	Power Supply, connect to VDD
4	5	GND2	-	Ground Pin, connect to GND
5	6	GND	-	Ground Pin
6	7	VDD	-	Power Supply
7	8	OSC	I	Oscillator input pin, A resistor and a capacitor is connected to this pin to determine the oscillation frequency
8	3	SDA	I/O	data input/output for I²C communication

Block Diagram

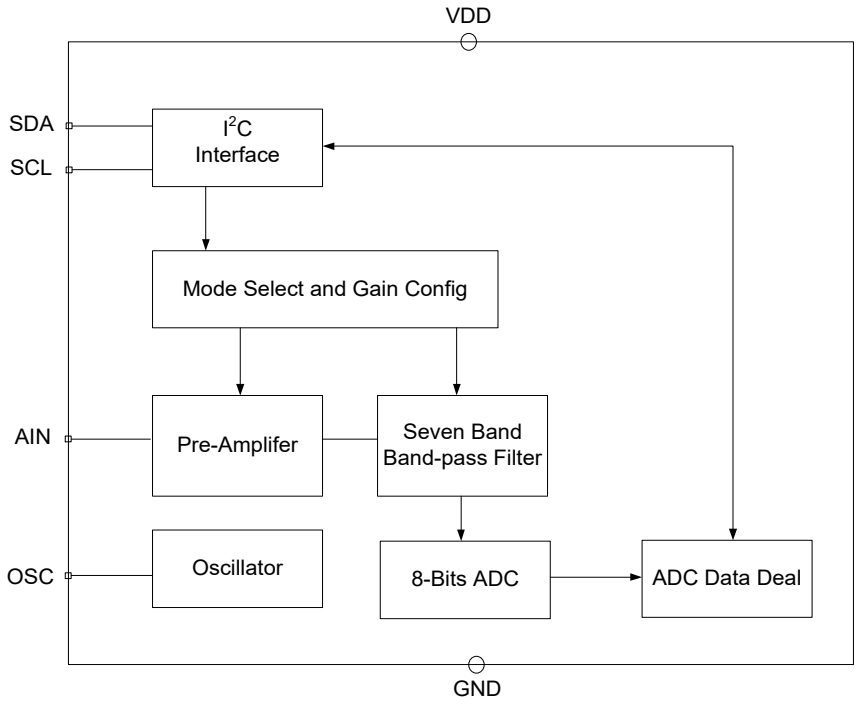


Figure 2. Block Diagram

Functional Description

I. Oscillator—RC Select

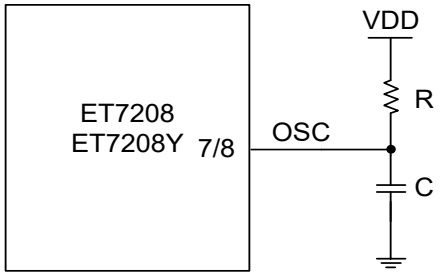


Figure 3. RC Select

OSC value	VDD voltage	R value	C value
2.5MHz	5.0V	18KΩ	33pF
	4.2V	16KΩ	33pF
	3.3V	15KΩ	33pF

II. I²C Bus Description

Bus Interface

MCU can transmit data with ET7208 each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected.

Data Validity

When the SCL signal is HIGH, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

Start (Re-start) and Stop Working Conditions

When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

Byte Format

Each byte of data line contains 8 bits, which contains an acknowledge bit. The first data is transmitted MSB.

Acknowledge

During the writing mode, ET7208 will send a low level response signal with one period width to the SDA port. During the reading mode, ET7208 will not send response signal and the host will send a high response signal one period width to the SDA.

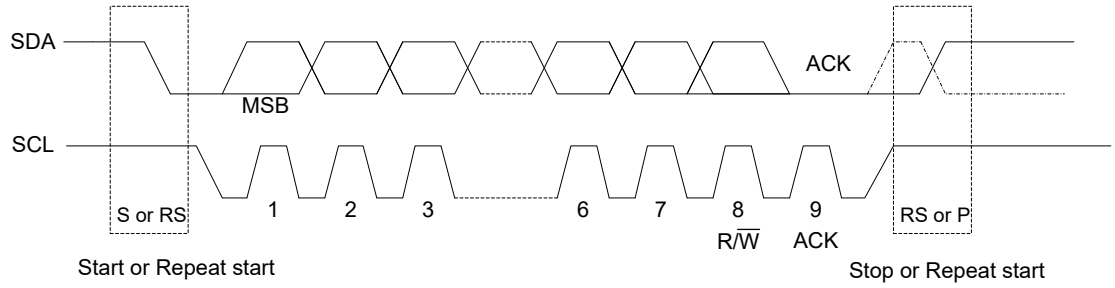


Figure 4. I²C Writing Mode

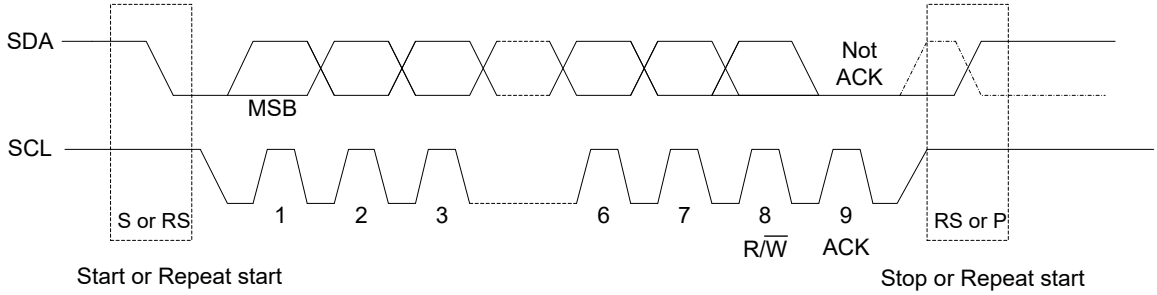


Figure 5. I²C Reading Mode

- ACK=Acknowledge
- NotACK=No Acknowledge
- R/$\overline{W}$ =Reading/Writing Mode
- MSB=Most Significant Bit
- S=Start Conditions RS=Restart Conditions P=Stop Conditions
- Fastest Transmission Speed =100KBits/S
- Re-Start (RS): SDA-level turnover as expressed by the dashed line waveform

I²C Interface Protocol

Writing Command Register Interface Protocol：

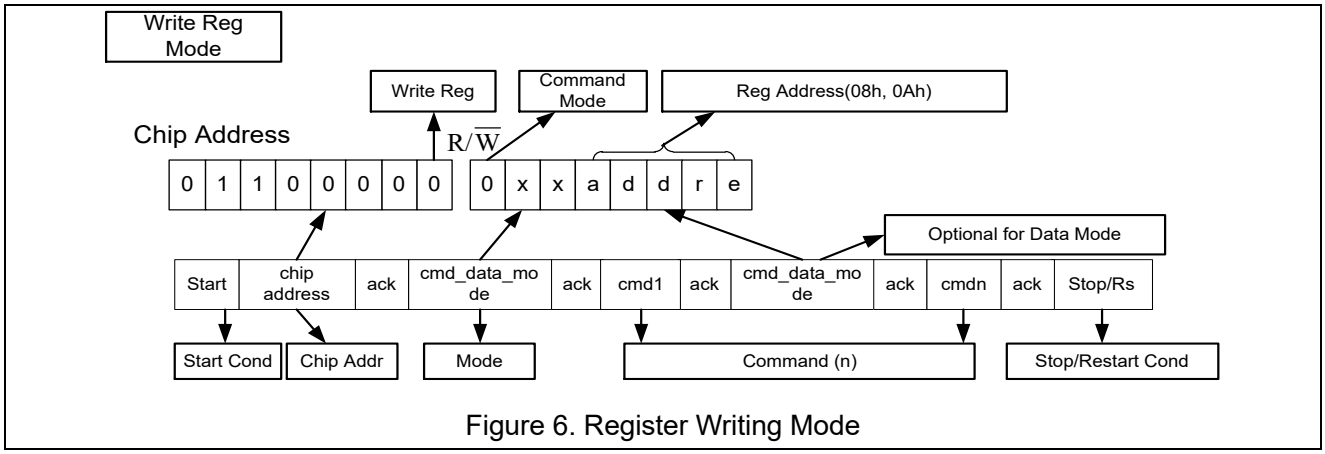


Figure 6. Register Writing Mode

- Start Cond=Start Conditions
- Chip Addr=Chip Address=0110000b
- R/$\overline{W}$ = Reading/Writing control bit= Write Reg=0b
- ACK=Acknowledge=0b
- Mode Byte=Command Mode bit=0b +don't care bit=xx + Command Register Address=addre
- ACK= Acknowledge
- Command(n)=Data for Command Register
- Stop/Restart Cond=Stop/Restart conditions

Reading Command Register Interface Protocol：

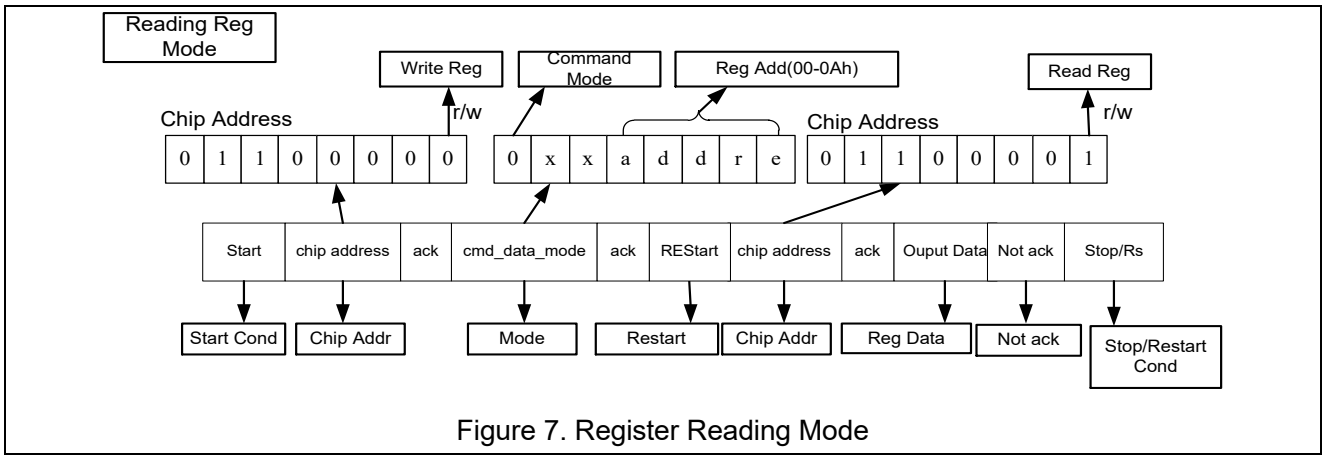


Figure 7. Register Reading Mode

- Start Cond=Start Conditions
- Chip Addr=Chip Address=0110000b
- R/$\overline{W}$ = Reading/Writing control bit= Write Reg=0b
- ACK=Acknowledge=0b
- Mode Byte=(Command Mode bit=0b +don't care bit=xx + Command Register Address=addre)
- Restart Cond=Restart conditions
- Chip Addr=Chip Address =0110000b
- R/$\overline{W}$ = Reading/Writing control bit= Write Reg=1b
- Reg Data= Data Out from Register (Send Reading Clock)
- NOTACK=No acknowledge(1b)
- Stop/Restart Cond=Stop/Restart conditions

Application Examples：

I²C Writing Command Register

Writing 01H data to register with 08H address，sending command：I²C start conditions 60H(chip address+I²C write reg bit) ,08H(command mode bit + register address) ,01H(data for register), I²C stop conditions。

I²C Reading Command Register

Reading data from register with 00H address，sending command：I²C start conditions 60H(chip address+I²C write reg bit), 00H(command mode bit + register address), I²C restart conditions 61H(chip address+I²C read reg bit) Send Reading Clock (Data Out from Register) I²C stop conditions。

Default Applications：

Data Set Register(addr=08H)=01b

(mdsel＝01b，Reading ADC Data Mode，shutdown＝0，Open)

(setting pre-amplifier gain according to different input audio signal amplitude (gc))

Display Control Register(addr=0AH)=00H

(Display shut down)

III. Register Definition

Table I. ADC Conversion Results Register

Addr: 00h-07h			Adc_one,Adc_two…Adc_eight Register		
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**
00h	7:0	adc_one	00h	R	ADC Conversion Results 63Hz Audio Data ADC Conversion Result
01h	7:0	adc_two	00h	R	ADC Conversion Results 160Hz Audio Data ADC Conversion Result
02h	7:0	adc_three	00h	R	ADC Conversion Results 400Hz Audio Data ADC Conversion Result
03h	7:0	adc_four	00h	R	ADC Conversion Results 1KHz Audio Data ADC Conversion Result
04h	7:0	adc_five	00h	R	ADC Conversion Results 2.5KHz Audio Data ADC Conversion Result
05h	7:0	adc_six	00h	R	ADC conversion Results 6.25KHz Audio Data ADC Conversion Result
06h	7:0	adc_seven	00h	R	ADC Conversion Results 12KHz Audio Data ADC Conversion Result
07h	7:0	adc_eight	00h	R	Volume Data Average of the Results ADC Conversion of 7-band Frequency

Table II. Data Set Register

Addr: 08h		Data Set Register			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	mdsel	00b	R/W	Data Source (Mode Select)	
				00	Reserve
				01	ADC working
				10	Reserve
4:2	gc	000b	R/W	Pre-Amplifier Gain Setting	
				000	0db
				001	6db
				010	12db
				011	18db
				100	-6db
				101	-12db
				110	-18db
				111	X
6:5	xx	xx	xx	Don’t care	
7	shutdown	1b	R/W	0	Operation
				1	Standby

Note：mdsel is a mode setting bit：

(1)00, reserve；(2)10, reserve；(3)01, Users can read the current ADC data to handle。

Table III. Quiescent Current Control Register (**Setting 00H in this circuit**)

Addr: 0Ah		**Display Control Register**			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
6:0	disp_pwm	0000001	R/W	Reserve	
7	disp_con	0b	R/W	0	Low quiescent current
				1	High quiescent current

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	-0.5～+7.0	V
Logic Input Voltage	V_I	-0.5～V_{DD}+0.5	V
Operating Junction Temperature	T_J	-40～+150	°C
Storage Temperature	T_{STG}	-65～+150	°C

Recommended Operating Range

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltag	V_{DD}	2.7	—	5.5	V
Audio Input Voltage(Gain=0dB)	V_{AIN}	0.1		1.0	V_{PP}
High-Level Input Voltage	V_{IH}	2.0	—	V_{DD}	V
Low-Level Input Voltage	V_{IL}	0	—	0.4	V
SCL Clock Frequency	F_{SCL}			400	KHz
Operating Temperature	T_A	-40		85	°C

Electrical Characteristics

(V_{DD}=5V，GND=0V，T_A=25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Voltag	V_{DD}		2.7		5.5	V
High-Level Input Voltage	V_{IH}		2.0	—	V_{DD}	V
Low-Level Input Voltage	V_{IL}		0	—	0.4	V
Oscillation Frequency	F_{OSC}		2.3	2.5	2.7	MHz
I^2C Input Current	I_{IO}				10	nA
Opertion Mode Current (1)	I_{DD}				2	mA
Standby Mode Current	I_S				1	uA

Note1：Test Conditions：Data Set Register =01b(mdsel＝01b，Reading ADC Data Mode)

Quiescent Current Register(addr=0AH)=00H (Low quiescent current)

Application Circuits

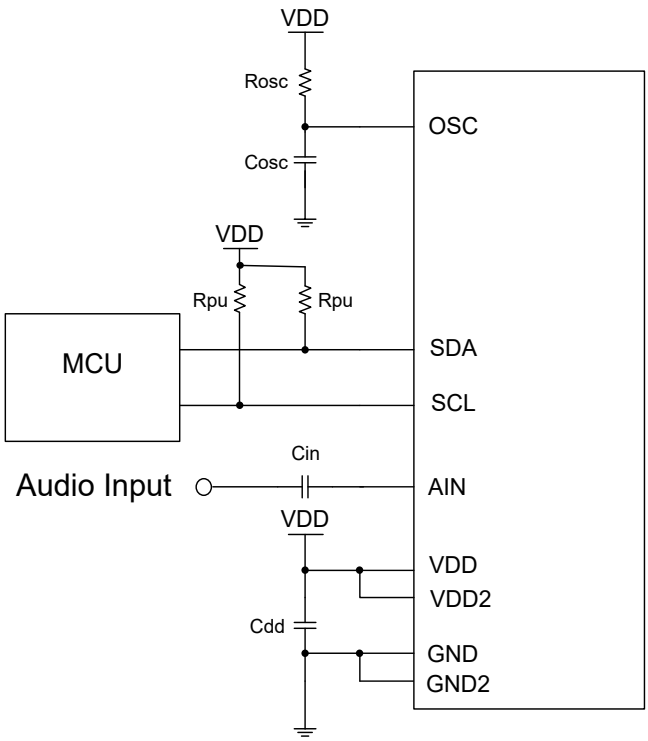


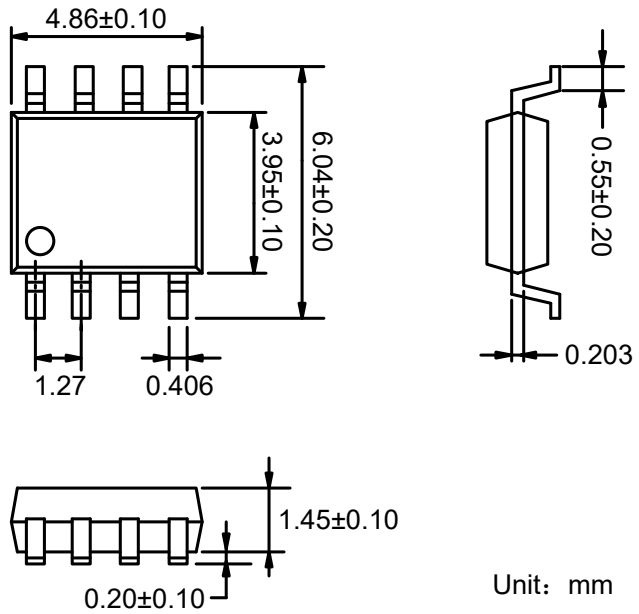
Figure 8. Typical Application Circuits

*：This circuit is for reference only.

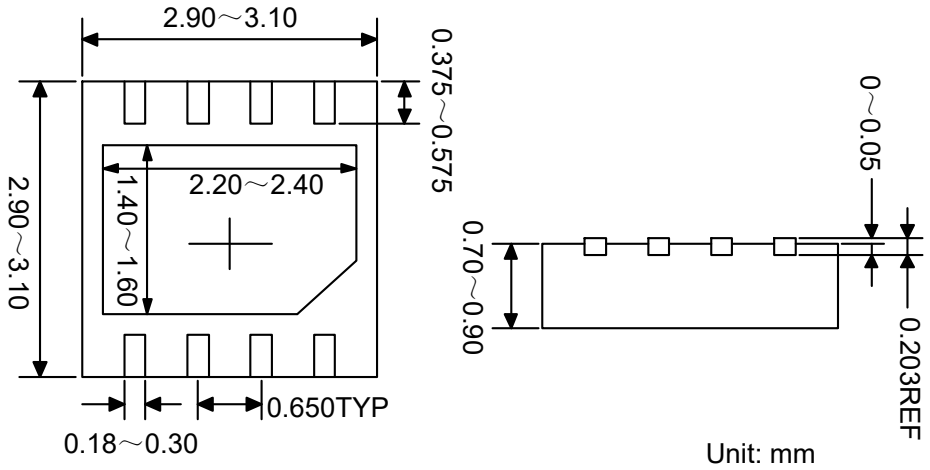
- Rosc /Cosc reference to RC Select table；
- Pup recommended 4.7KΩ～10KΩ；
- Cdd recommended 1uF～10uF；
- Cin recommended 1uF；
- R and L channel can connect together to Audio Input with separate series resistors.

Package Dimension

SOP8



DFN8



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2010-8-16	Original version	Sunsb	Wangb	Zhu Jun Li
1.1	2023-8-8	Updated Typeset	Shibo		Zhu Jun Li