Volume Controller IC

General Description

ET2259BM is an 8-pin 2-channel volume controller which utilizes CMOS technology and incorporates the I²C interface control. The controller features an attenuation range of 0 to -79dB, low noise output, a high degree of stereo separation and requires only a small number of external components. ET2259BM is an essential component for modern audio visual systems.

Features

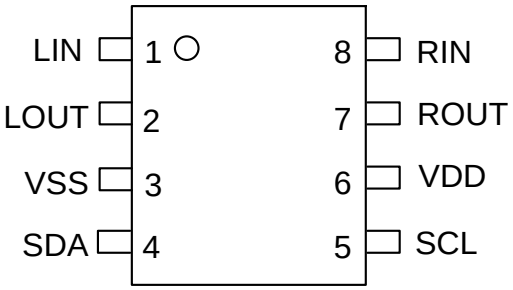
- Attenuation range: 0 to -79dB in 1dB steps
- Operating voltage: 4 to 9V
- Low power consumption
- Low signal noise: S/N > 100dB (A-weighting)
- Stereo separation > 100dB
- Requires few external components
- 2-channel volume individual adjust
- Part No. and package

Part No.	Package	MSL
ET2259BM	SOP8	Level 3

Applications

- Audio/visual surround sound systems
- Car audio systems
- Mini-compo systems
- Computer multi-media speakers
- Other audio applications

Pin Configuration

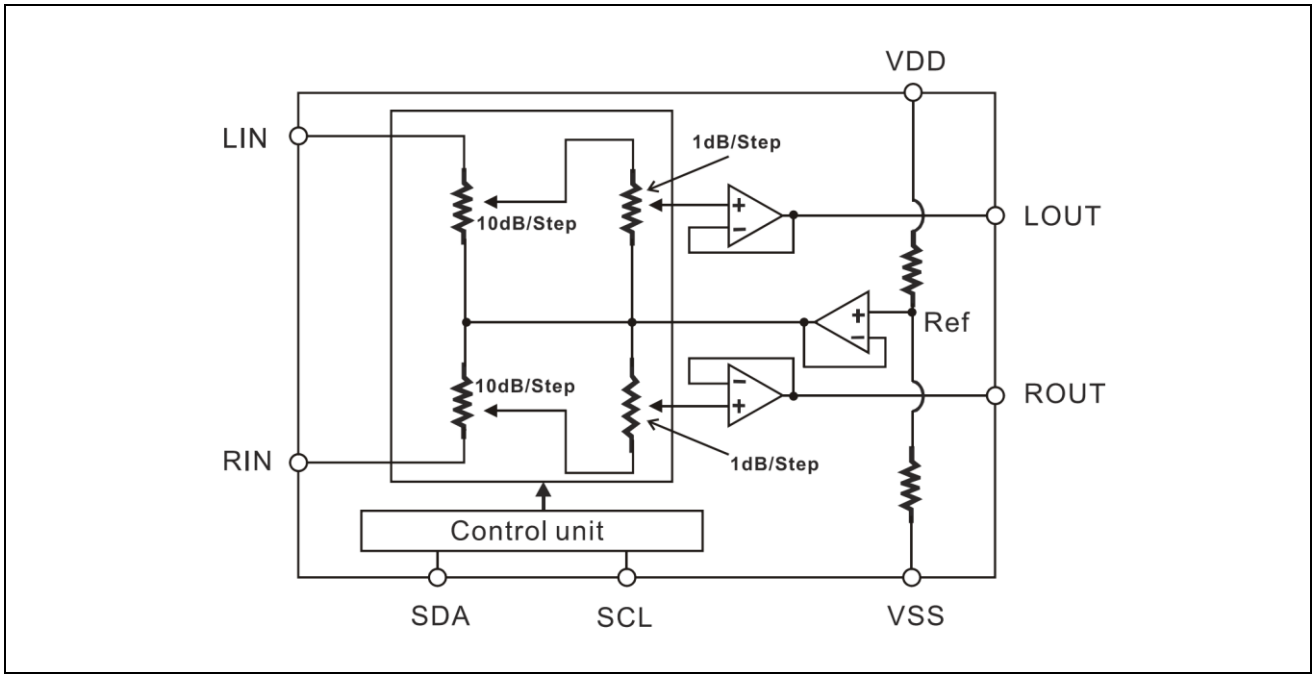


Top View

Pin Function

Pin NO.	Pin Name	I/O	Description
1	LIN	I	Left Channel Input (capacitor coupled to input port)
2	LOUT	O	Left Channel Output (capacitor coupled to output port)
3	VSS	—	Ground
4	SDA	I	I^2C Data Input
5	SCL	I	I^2C Clock Input
6	VDD	—	Power Supply
7	ROUT	O	Right Channel Output (capacitor coupled to input port)
8	RIN	I	Right Input Channel (capacitor coupled to output port)

Block Diagram



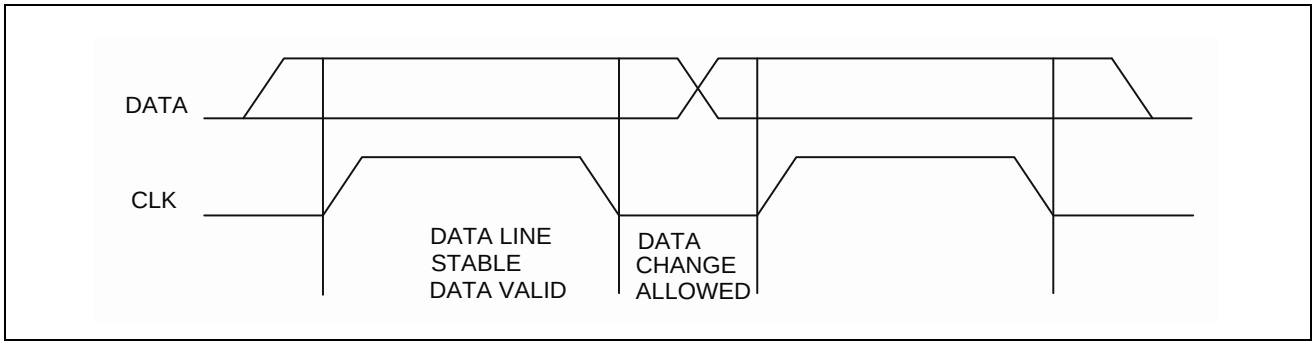
Functional Description

I²C Bus Interface

In ET2259BM the DATA and CLK make up the bus interface through which data is transmitted to and from the microprocessor.

Data Validity

Data on the DATA line is considered valid and stable only when the CLK signal is in the “high” state. In addition, the “high” and “low” states of the DATA line can change only when the CLK signal is in the “low” state. Please refer to the diagram below:

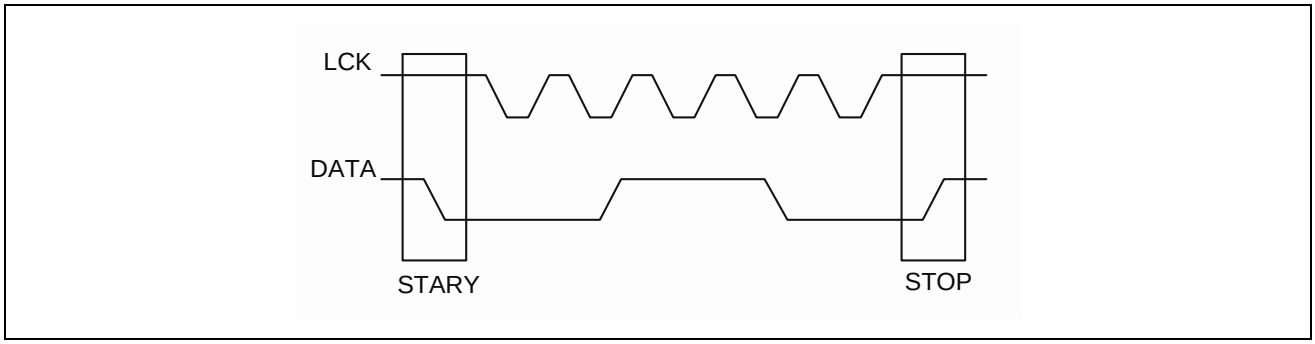


Start and Stop Conditions

A start condition is activated when 1) the CLK signal is set to “high” and 2) the DATA signal shifts from “high” to “low”.

A stop condition is activated when 1) the CLK signal is set to “high” and 2) the DATA signal shifts from “low” to “high”.

Please refer to the timing diagram below:



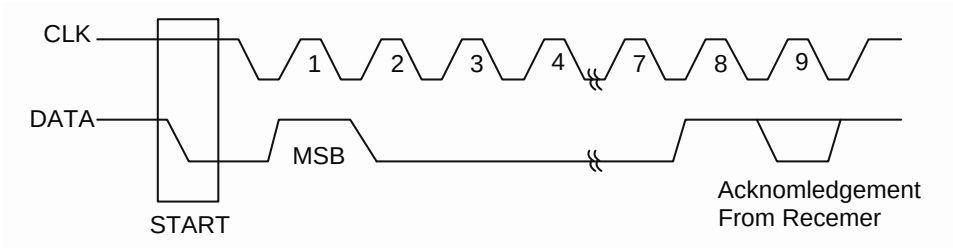
Byte Foemat

Every byte transmitted to the DATA line consists of 8 bits and each byte must be followed by an “acknowledge” bit. The MSB is transmitted first.

Acknowledge Signal

During the ninth clock pulse, the microprocessor puts a resistive “high” level on the DATA line. If the peripheral audio processor (ET2259BM) acknowledges, it will pull the DATA line from a “high” state to a “low” state during this acknowledge clock phase so that the DATA line is in a stable “low” state during this clock

pulse. Please refer to the diagram below.



The audio processor that has been address (ET2259BM) must generate an “acknowledge” signal after receiving each byte or the DATA line will remain at the “high” level during the ninth clock pulse.

Transmission without Acknowledge

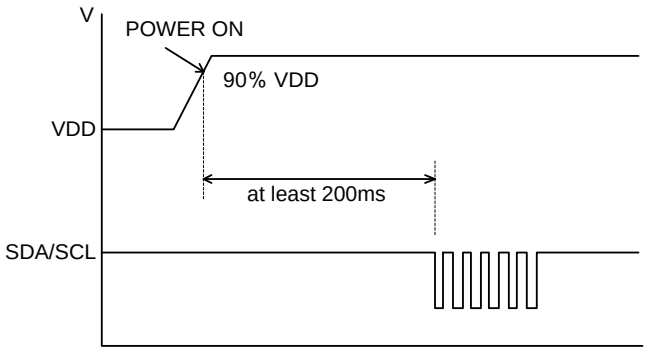
If you do not wish the audio processor (ET2259BM) to detect the “acknowledge” signal, a simpler microprocessor transmission method can be used: after ET2259BM has received a byte wait for one clock pulse and do not acknowledge it. If this approach is used, however, there is a greater chance for faulty operations to occur and noise immunity will be decreased.

Address Select

ET2259BM Address is 88H.

I²C Start Time

When ET2259BM is powered on, a short period must elapse before voltage becomes stable. After the power is turned on, ET2259BM must wait at least 200ms before it is able to send an I²C control signal otherwise control efficacy and normal operation will be comprised. Please refer to the diagram below:

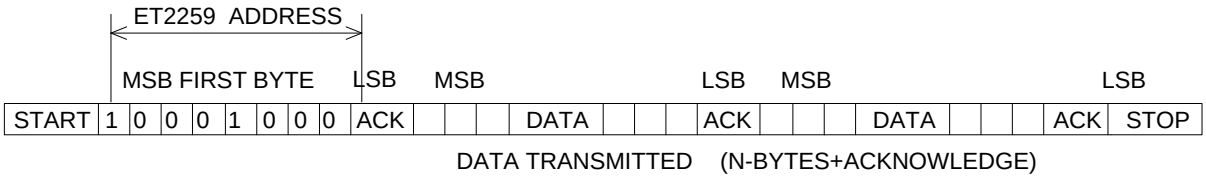


Interface Protocol

The interface protocol consists of the following:

- A start condition
- The ET2259BM address byte followed by an “acknowledge” signal
- A data sequence (n-bytes and an “acknowledge” signal)
- A stop condition

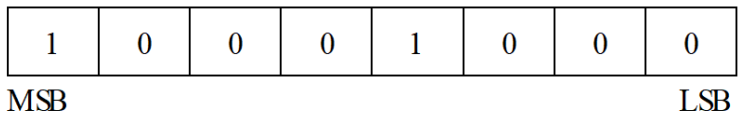
Please refer to the following diagram:



Note: ACK=ACKNOWLEDGE, Max Clock Speed = 100K BITS/S

Software Specification

ET2259BM address is shown below:



Data Bytes Description

1.Function Bits

MSB							LSB	Function
1	1	0	1	A3	A2	A1	A0	2-channel, -1dB/step
1	1	1	0	B3	B2	B1	B0	2-channel, -10dB/step
1	0	1	0	A3	A2	A1	A0	Left channel, -1dB/step
1	0	1	1	B3	B2	B1	B0	Left channel, -10dB/step
0	0	1	0	A3	A2	A1	A0	Right channel, -1dB/step
0	0	1	1	B3	B2	B1	B0	Right channel, -10dB/step
1	1	1	1	0	0	0	0	Clear register
0	1	1	1	0	1	C1	C0	Mute select

2.Mute Function Bits

C0	C1	Function
0	0	Mute OFF
0	1	Right channel mute ON
1	0	Left channel mute ON
1	1	Left and right channel mute ON

3.Attenuation Unit Bits

A3/B3	A2/B2	A1/B1	A0/B0	Attenuation (dB)
0	0	0	0	0/0
0	0	0	1	-1/-10
0	0	1	0	-2/-20
0	0	1	1	-3/-30
0	1	0	0	-4/-40
0	1	0	1	-5/-50
0	1	1	0	-6/-60
0	1	1	1	-7/-70
1	0	0	0	-8/-80
1	0	0	1	-9/

ET2259 Control Software Procedure

ET2259 has a built-in Power-On Reset function which clears the function register to zero after power-on. In order to ensure normal operation under any operating voltage, it is recommended an instruction to clear the register must be transmitted. Please refer to the following diagram:

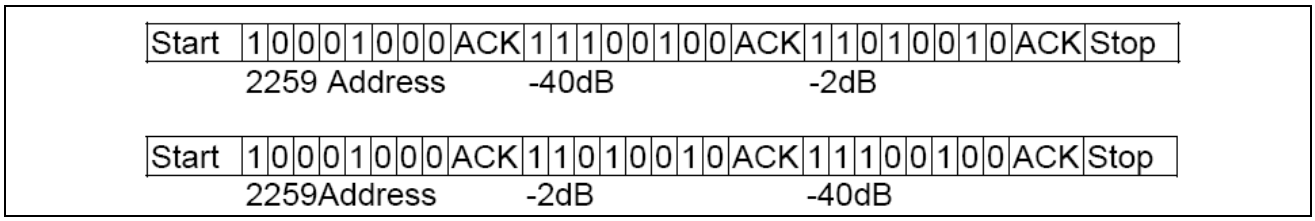
Start	1	0	0	0	1	0	0	0	Ack	1	1	1	1	0	0	0	0	Ack	Stop

ET2259 Address（Example：88H） Clear Registry

The ET2259 function register does not have any default settings. After clearing the register, an initial value must send in order to each register. If a register does has not been set, it is possible that no sound will be output.

When adjusting the volume of ET2259, it is necessary to send a multiple of 10dB followed by a 1dB code to the attenuator in sequence. If this sequence is not followed, or if only a 10dB or 1dB value is sent, the IC may not operate normally. Please refer to the diagram below:

Example: Request volume setting of -42dB:



The two methods above are both acceptable.

WARNING! THE FOLLOWING TRANSMISSION METHODS ARE NOT PERMITTED.

Sending only a 10dB attenuation value:

Start	1	0	0	0	1	0	0	0	Ack	1	1	1	0	0	1	0	0	Ack	Stop

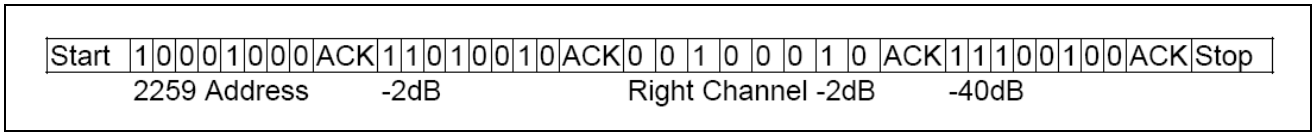
ET2259 Address -40dB

Sending only a 1dB attenuation value:

Start	1	0	0	0	1	0	0	0	Ack	1	1	0	1	0	0	1	0	Ack	Stop

ET2259 Address -2dB

Sending a 10dB code with a 1dB code simultaneously or in combination with other control codes:



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	12	V
Operating Temperature	T_A	-40 ~ +85	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C
Input Voltage	V_I	-0.3 ~ V_{CC} + 0.3	V

Electrical Characteristics

Unless otherwise noted, typical values are at V_{CC}=9V, V_I=1Vrms, f=1kHz, T_A=27°C.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{CC}	Operating Voltage			4	9	12	V
I_{CC}	Operating Current	V_{CC}=9V, V_I=0V			2.5	3	mA
A_{RANGE}	Volume Attenuation Range	Minimum attenuation			0		dB
		Maximum attenuation			-89		
A_{STEP}	Attenuation Step				1		dB
G_{ERR}	Attenuation Step Gain Error				0.5		dB
C_{ERR}	Interchannel Attenuation Gain Error				0.5		dB
V_{OMAX}	Maximum Output Voltage	V_{CC}=9V, Freq=1kHz, Volume Att=0dB, R_{LOAD}=50kΩ, THD<1%		2.0	2.3	2.5	Vrms
THD	Total Harmonic Distortion	f=1kHz, Volume Att=0dB, A-weight R_{LOAD} = 50kΩ	V_{OUT}= 2Vrms		0.07	0.09	%
			V_{OUT}= 200mVrms		0.003	0.005	%
N_O	Noise Output	V_{IN}=GND, Mute=OFF, Volume Att= 0dB, A-weighted			2	3	μVrms
SNR	Signal-to-Noise Ratio	V_{IN}=1Vrms, Att= 0dB	No-weighted	95	100	103	
			A-weighted	110	120	125	dB
CS	Channel Separation	V_{IN}=2.5Vrms, Freq=1kHz, Volume Att= 0dB		100	120	125	dB
MUTE	Mute	V_{IN}=2.5Vrms, Freq=1kHz, Volume Att.= 0dB, A-weighted		90	95	97	dB
FR	Frequency Response	V_{IN}=1Vrms, Volume Att= -10dB			1	1.3	MHz
R_{IN}	Input Impedance	f = 1kHz				33	kΩ
R_{OUT}	Output Impedance	f=1kHz, V_{OUT}= 100mVrms				6	Ω

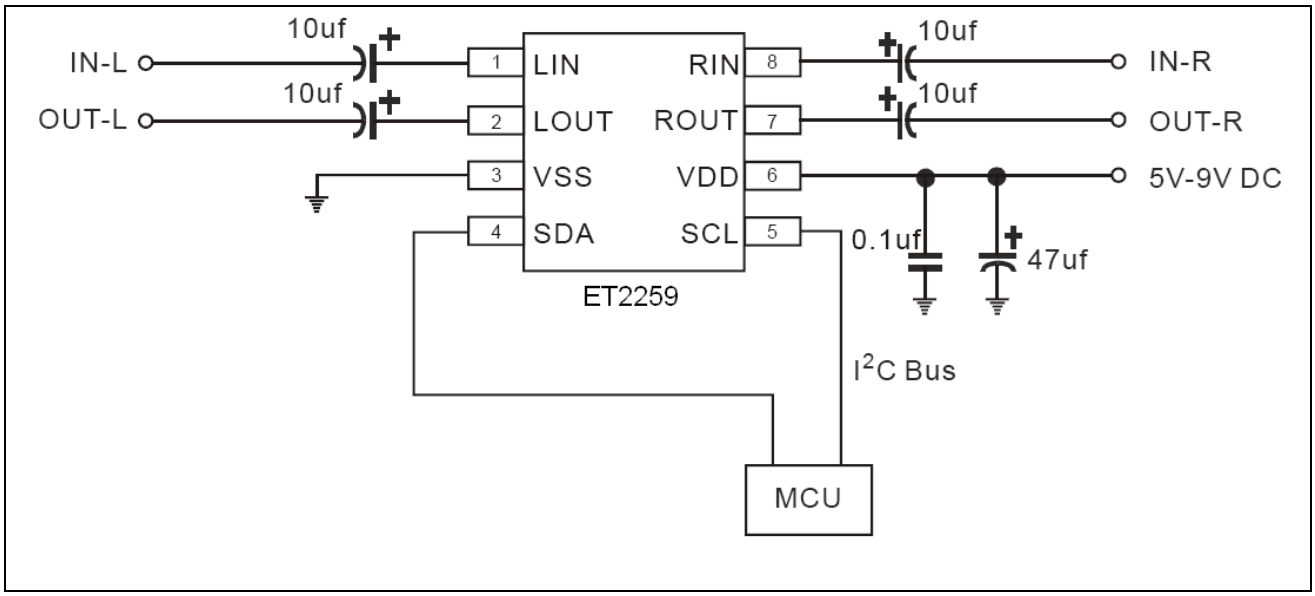
Electrical Characteristics (Continued)

I²C BUS SECTION ELECTRICAL CHARACTERISTICS

Unless otherwise noted, typical values are at V_{CC}=9V, V_I=1Vrms, f=1kHz, T_A=27°C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Bus High Input Level		0.5			V
V_{IL}	Bus Low Input Level				0.2	V

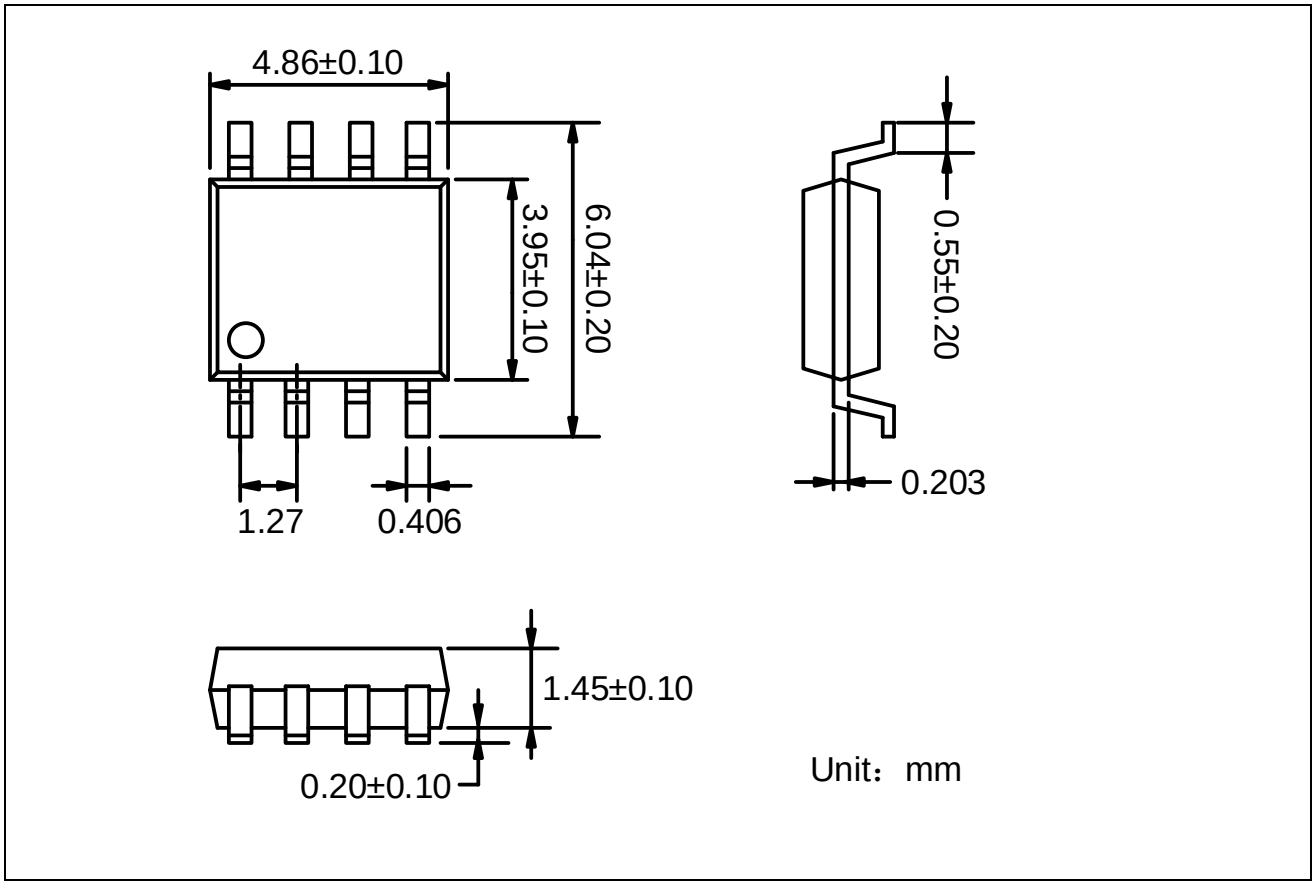
Application Circuits



Note*. This electric circuit only supplies for reference.

Package Dimension

SOP8



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2018-6-15	Original Version	Shi bo	Wang Guo Peng	Liu Jia Ying
1.1	2023-12-22	Update Typeset	Pan Shun Ye	Wang Guo Peng	Liu Jia Ying