Matrix LED Drive Control with Keyboard Scan

General Description

ET6226 is a specific LED drive control circuit with a keyboard scanning interface circuit. Internal integrated MCU digital interface input and output, data latches, LED drives, keyboard scanning, brightness adjustment and so on. The chip performance is stable, reliable quality, anti-interference ability, can be adapted to work in 24 hours of continuous long-term applications.

Features

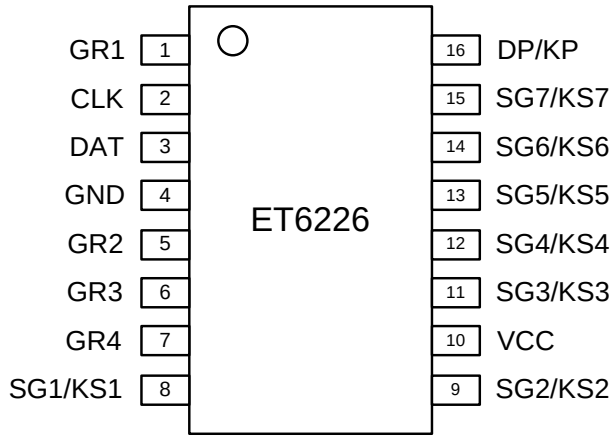
- Supports 3.0V～5.5V supply voltage
- Display matrix mode: 8×4 or 7×4
- Provide 8 step brightness control
- Keyboard scanning: 7×4bit
- High-speed two-wire serial interface (DAT,CLK)
- Built-in oscillator circuit
- Built-in power-on reset circuit
- Part No. and Package

Part No.	Package
ET6226P	DIP16
ET6226M	SOP16
ET6226S	SSOP16

Application

- small household appliances
- set-top box
- Device digital tube indication

Pin Configuration



TOP VIEW

Pin Description

Symbol	Pin name	Description
SG1/KS1～SG7/KS7	Segment drive output /keyboard scanning input	LED segment high side drive output, Also used as key scan input, active high, internal pull-down
GR1～GR4	Bit/keyboard scanning output	LED low side drive output,Also used as key scan output
DP/KP	Segment/Bit output	LED segment output, also output for keyboard symbol
CLK	Clock input	Clock input, internal pull-up resistor
DAT	Data output/input	Data input and output, built-in drain mode pull-on
VCC	Supply voltage	3V~5.5V Power Supply pin
GND	Ground	Ground pin

Functional Description

Two-wire Bus Interface

The ET6226 and MCU can transmit signal by DAT and CLK serial signal. DAT and CLK constitute two-wire interface.

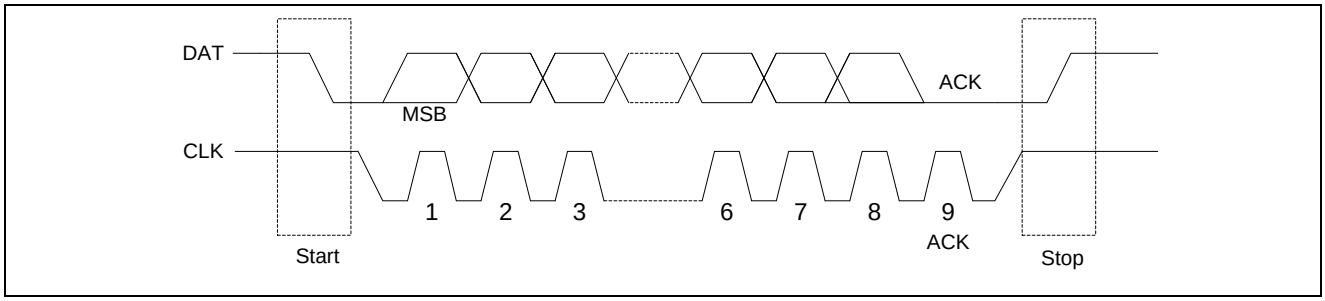
Data signal

When CLK signal is high, DAT signal must be stable. The high or low state of the DAT signal can only change when the CLK signal is low.

Start and stop condition

When the CLK signal is high，DAT signal from high to low transition, This situation indicates serial signal transmission start.

When the CLK signal is high，DAT signal from low to high transition, This situation indicates serial signal transmission stop. As show blow：



Command signal format

DAT format of the command signal has 8 bit, after each command signal the need for a confirmation signal, and the maximum signal bit "MSB" headed sent.

Format of acknowledge signal

DAT bus is set to high impedance state by the MCU during the ninth clock cycle, if ET6226 confirm this signal, then the DAT will be pulled low by the ET6226, the DAT bus to maintain a stable low state.

The ET6226 will produce a confirmation signal after received each command signal, or in the ninth clock will remain high level.

No acknowledge signal transmission

If you want to omit the ET6226 to acknowledge signal detection, you can use a simple transmission. The way for ET6226 in receiving a command signal, wait for a clock pulse, not to acknowledge. If you use this method will likely result in transmission errors, and will reduce the anti-jamming capability.

Control Program Format

ET6226 control program format as show below, under the command of SYSON show:

	B7	B6	B5	B4	B3	B2	B1	B0		B7	B6	B5	B4	B3	B2	B1	B0		
Start	0	1	0	0	1	0	0	0	Ack	0	0	0	0	0	0	0	1	Ack	Stop

Status Control Command Format

High 8 bits data:48H

B7	B6	B5	B4	B3	B2	B1	B0
0	1	0	0	1	0	0	0

Low 8 bits data is follow:

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
0								Don't care	Please set to 0
	0	0	0					8 steps brightness adjust	8 step（highest brightness）
	0	0	1						1 step（lowest brightness）
	…	…	…						…
	1	1	1						7step
				1				Mode selection	7 segment
				0					8 segment (DP/KP) as SG output
					1			Sleep command	Sleep mode
					0				Operation mode

						0		Don't care	Please set to 0
							1	Display switch	Display ON
							0		Display OFF

For example: "48H,X1H" is 8 segment mode, "X" is brightness step; "48H,X9H" is 7 segment mode; "48H,04H" is sleep mode.

Note: D0 and D2 cannot be "1" at the same time.

Note: when the circuit operate at 7 segment mode or 8 segment mode, DP/KP ports working condition is different, and need the peripheral circuit is also different.

Display Data Command

High 8-bit	Display Data (Low 8-bit)								
	DP/KP	**SG7/KS7**	**SG6/KS6**	**SG5/KS5**	**SG4/KS4**	**SG3/KS3**	**SG2/KS2**	**SG1/KS1**	
68H	B7	B6	B5	B4	B3	B2	B1	B0	**GR1**
6AH	B7	B6	B5	B4	B3	B2	B1	B0	**GR2**
6CH	B7	B6	B5	B4	B3	B2	B1	B0	**GR3**
6EH	B7	B6	B5	B4	B3	B2	B1	B0	**GR4**

Key Code Command

High 8-bit	Return Key Codes (Low 8-bit)							
4FH	B7	B6	B5	B4	B3	B2	B1	B0

	GR1	GR2	GR3	GR4
SG1/KS1	44H	45H	46H	47H
SG2/KS2	4CH	4DH	4EH	4FH
SG3/KS3	54H	55H	56H	57H
SG4/KS4	5CH	5DH	5EH	5FH
SG5/KS5	64H	65H	66H	67H
SG6KS6	6CH	6DH	6EH	6FH
SG7/KS7	74H	75H	76H	77H

Absolute Maximum Ratings（T_A= 25℃）

Symbol	Parameter	Range	Unit
V_{CC}	Power supply	-0.5 ～ +6.5	V
V_I	I/O port Input voltage	-0.5～V_{CC} + 0.5	V
I_{CC}	Max power input current	150	mA
T_{STG}	Storage temperature	-65 ～ +150	ºC
T_J	Operating junction temperature	-40 ～ +150	ºC
T_A	Operating ambient temperature	-40 ～ +85	ºC

Electrical Characteristics

Test Condition：T_A = 25℃，V_{CC} = 5V

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply voltage	3.0	5.0	5.5	V
I_Q	Quiescent current（CLK、DAT、KP is high）		0.3	0.6	mA
I_{Q_OFF}	Sleep current（CLK、DAT、KP is high）		0.05	0.1	mA
V_{IL}	CLK and DAT pin low level input voltage	-0.5		0.2V_{CC}	V
V_{IH}	CLK and DAT pin high level input voltage	0.6V_{CC}		V_{CC}+0.5	V
I_{OHSG1}	SG/KS pin high level input current（V_O=V_{CC}-2V）	-25	-40	-50	mA
I_{OHSG2}	SG/KS pin high level input current（V_O=V_{CC}-3V）	-35	-50	-60	mA
I_{OLGR}	GR pin low level input current（V_O=0.3V）	40	50		mA
V_{RESET}	The default power-on reset threshold voltage		2.5		V

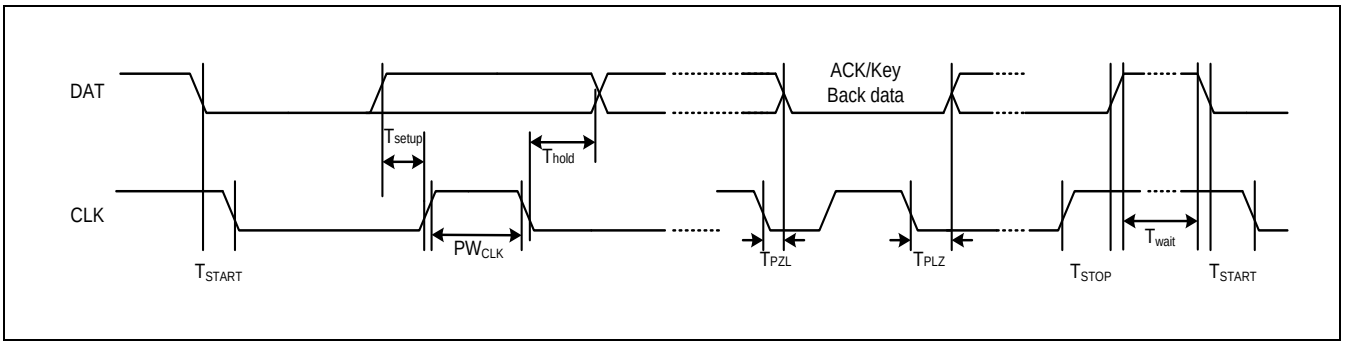
Internal Timing Parameters

Test Condition：T_A = 25℃，V_{CC} = 5V

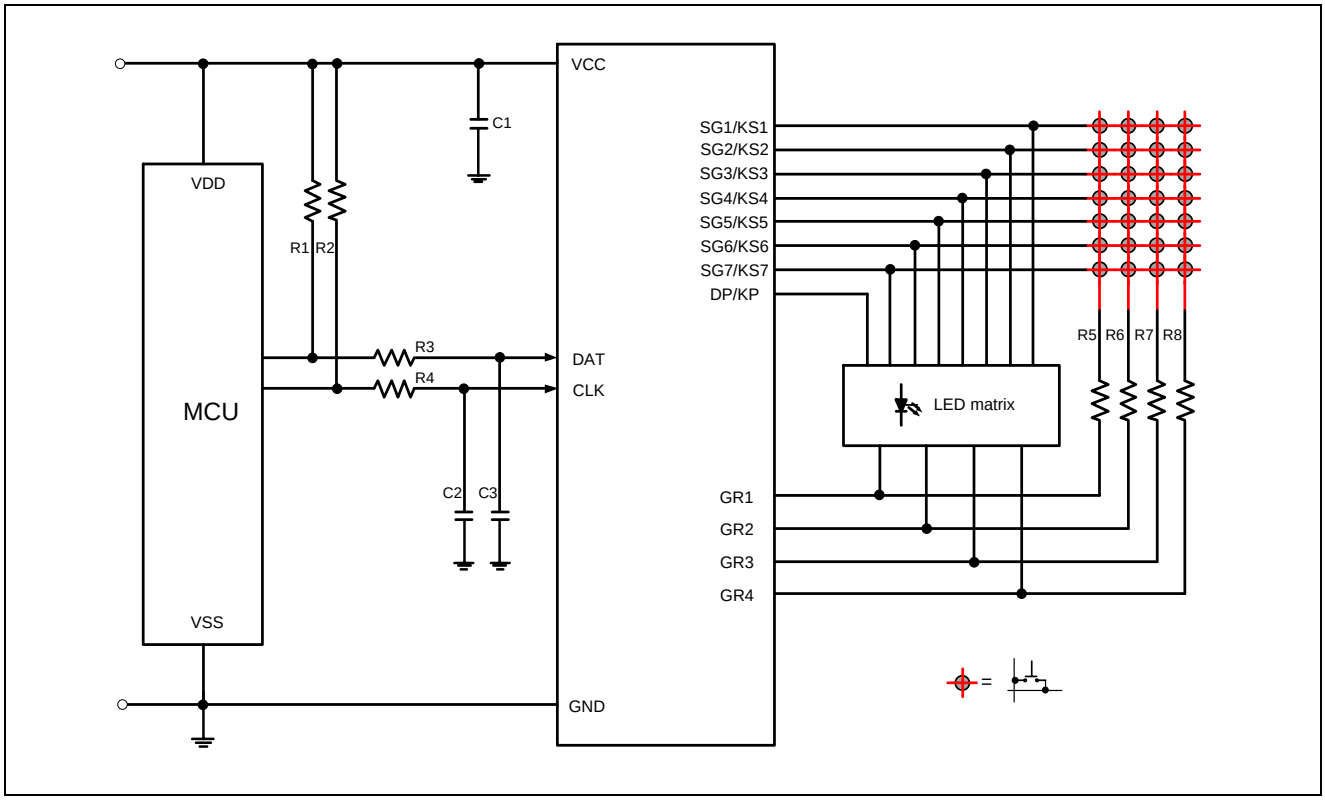
Symbol	Parameter	Min	Typ	Max	Unit
T_{START}	DAT holding time of the falling edge start signal	100	-	-	ns
T_{STOP}	DAT holding time of the rising edge stop signal	100	-	-	ns
PW_{CLK}	Clock Pulse Width	400	-	-	ns
T_{SETUP}	Data setup Time	100	-	-	ns
T_{HOLD}	Data Hold Time	100	-	-	ns
T_{PZL}	DAT effectively data delays the falling edge of CLK	2	-	30	ns
T_{PLZ}	DAT Invalid data delays the falling edge of CLK	2	-	40	ns
T_{WAIT}	waiting time, CLK↑→CLK↓	1	-	-	us
Rate	Average Data Transfer Rate	0		400	Kbps

Note: this table is built-in clock cycle timing parameters of multiple, built-in clock frequency with the power supply voltage decreases

Interface Timing Waveform



Typical Application



Note:

1. This application circuit is only for reference.

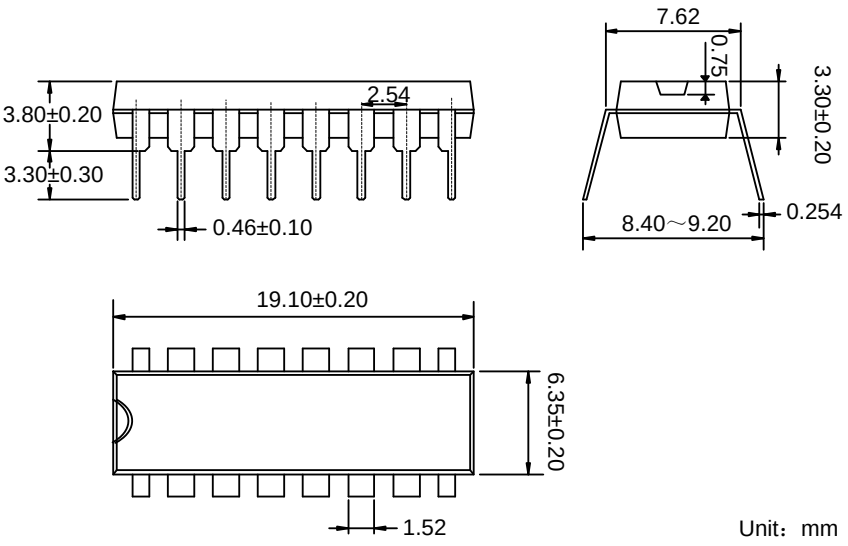
2. C1=1uF and should be placed as close as possible to the VCC.

3. R1,R2 = 4.7kΩ; R3,R4 = 100Ω; C2,C3 = 100pF; R5~R8 = 2kΩ.

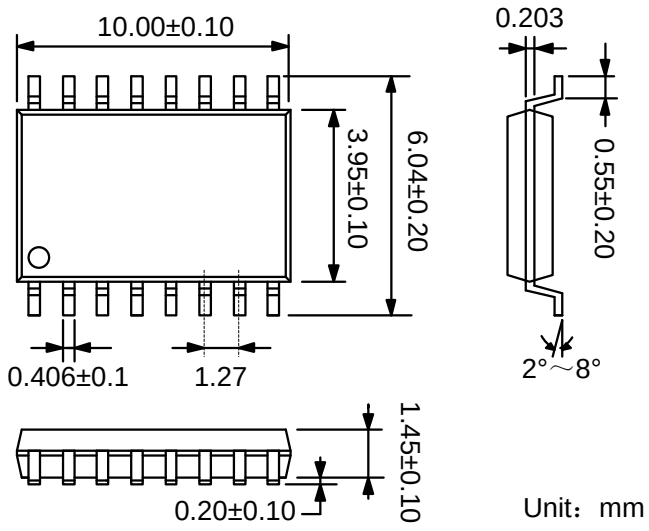
4. The series resistance of the communication port and the capacitor for GND should be placed as close as possible to ET6226, and the resistance value and capacitance value should be adjusted according to the actual anti-interference requirements and verification results.

Package Information

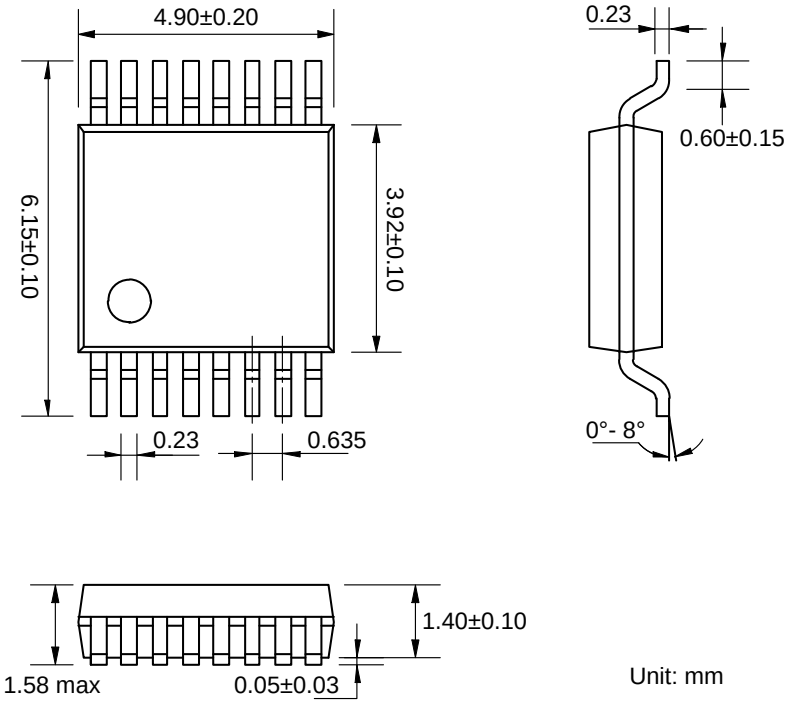
DIP16



SOP16



SSOP16



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2016-04-05	Original version	Shilj	Shi Liang Jun	Zhu Jun Li
1.1	2020-4-23	Document check	Shibo	Shilj	Liujy
1.2	2023-7-13	Update Typeset	Shibo	Shilj	Liujy
1.3	2025-9-8	Add SSOP16 EC table updated to CH version	Shibo	Shib	Liujy