8-bit Parallel-out Serial Shift Registers

General Description

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear $\overline{CLR}$ input. The gated serial (A and B) inputs permit complete control over incoming data; a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock (CLK) pulse. A high-level input enables the other input, which then determines the state of the first flip-flop.

Data at the serial inputs can be changed while CLK is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of CLK.

Features

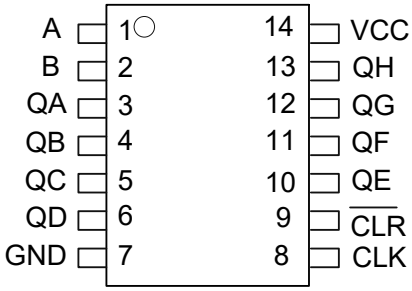
- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear
- Part No. and Package Information

Product Name	Package	MSL
74HC164V	TSSOP14	Level 3

Applications

- Memory Chip Select Decoding
- Data Transmission System

Pin Configuration



TOP VIEW

Figure1. Pin Configuration

Pin Function

Pin Number	Pin Name	Function
1	A	Serial Data Input
2	B	Serial Data Input
3	QA	Data Output
4	QB	Data Output
5	QC	Data Output
6	QD	Data Output
7	GND	Ground
8	CLK	Clock Pulse – Positive Edge Triggered
9	$\overline{CLR}$	Master Reset - Asynchronous
10	QE	Data Output
11	QF	Data Output
12	QG	Data Output
13	QH	Data Output
14	VCC	Supply Voltage

Function Table

Input Pin				Output Pin			
$\overline{CLR}$	CLK	A	B	QA	QB	…	QH
L	X	X	X	L	L		L
H	L	X	X	QA0	QB0		QH0
H	↑	H	H	H	QAn		QGn
H	↑	L	X	L	QAn		QGn
H	↑	X	L	L	QAn		QGn

Notes:

- QA0, QB0, QH0 = the level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established.
- QAn, QGn = the level of QA or QG before the most recent ↑ transition of CLK: indicates a 1-bit shift.

Block Diagram

Logic symbol

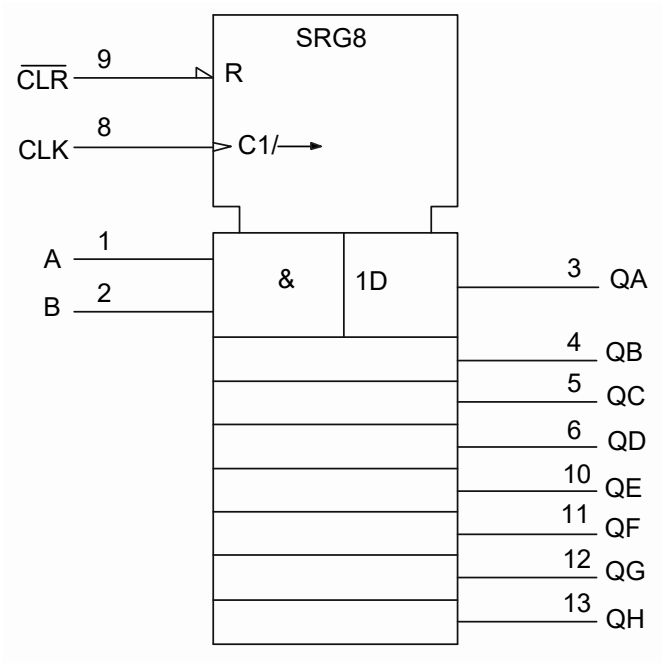


Figure2. Block Diagram

Logic Diagram

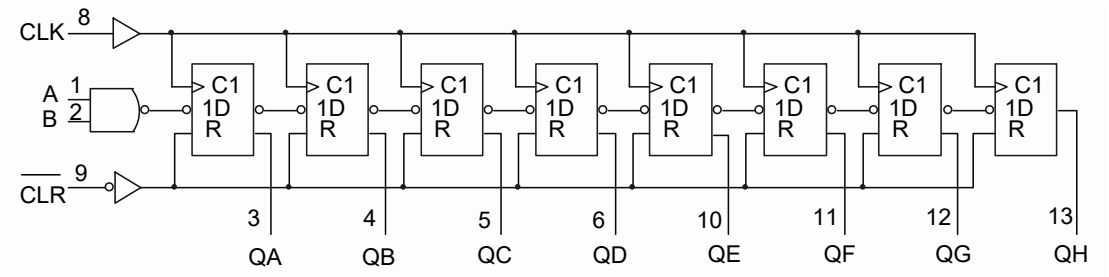


Figure3 Logic Diagram

Functions Description

Typical Clear, Shift, and Clear Sequence

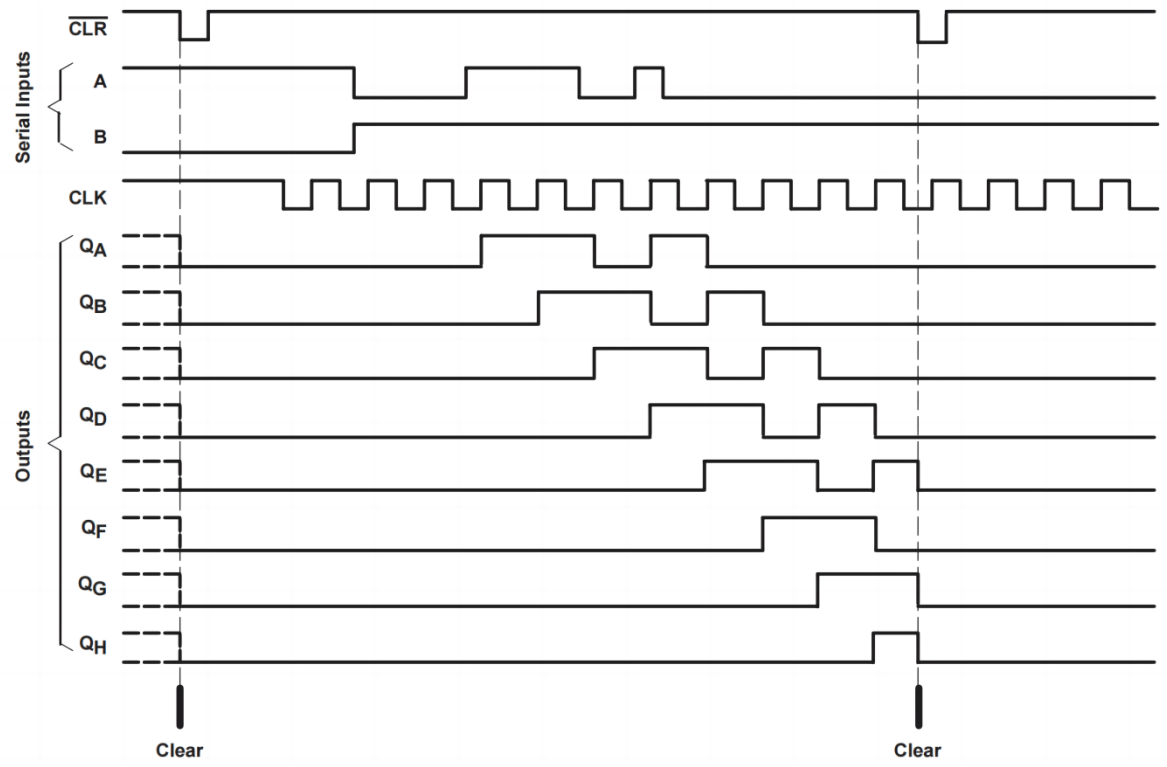


Figure4. Typical Sequence

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage(1)	V_{CC}	-0.5~7.0	V
Input Clamp Current	I_{IK}	±20	mA
Output Clamp Current	I_{OK}	±20	mA
Continuous Output Current	I_O	±25	mA
Continuous Current Through VCC Or GND	I_{CC}	±50	mA
Package Thermal Impedance(2)	θ_{JA}	140	°C/W
Storage Temperature	T_{STG}	-65~150	°C

Notes:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

Recommended operating conditions

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Supply Voltage	V_{CC}		2	5	6	V
High-Level Input Voltage	V_{IH}	V_{CC} = 2V	1.5			V
		V_{CC} = 4.5V	3.15			
		V_{CC} = 6V	4.2			
Low-Level Input Voltage	V_{IL}	V_{CC} = 2V	0		0.5	V
		V_{CC} = 4.5V	0		1.35	
		V_{CC} = 6V	0		1.8	
Input Voltage	V_I		0		V_{CC}	V
Output Voltage	V_O		0		V_{CC}	V
Input Transition (Rise And Fall) Time	t_t	V_{CC} = 2V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6V	0		400	
Operating Free-Air Temperature	T_A		-40		85	°C

Note:

If this device is used in the threshold region (from V_{IL_MAX} = 0.5V to V_{IH_MIN} = 1.5V), there is a potential to go into the wrong state from induced grounding, causing double clocking.

Operating with the inputs at tt = 1000ns and V_{CC} = 2V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

Electrical Characteristics

Symbol	Test Condition		V_{CC}(V)	T_A = 25°C			T_A = -40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
V_{OH}	V_I = V_{IH} or V_{OH}	I_{OH} = 20μA	2	1.9	1.998		1.9		V
			4.5	4.4	4.499		4.4		
			6	5.9	5.999		5.9		
		I_{OH} = -4mA	4.5	3.98	4.3		3.84		
		I_{OH} = -5.2mA	6	5.48	5.8		5.34		
V_{OL}	V_I = V_{IH} or V_{OH}	I_{OL} = 20μA	2		0.002	0.1		0.1	V
			4.5		0.001	0.1		0.1	
			6		0.001	0.1		0.1	
		I_{OL} = 4mA	4.5		0.17	0.26		0.33	
		I_{OL} = 5.2mA	6		0.15	0.26		0.33	
I_I	V_I = V_{CC} or 0		6		±0.1	±100		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O =0		6			8		80	μA
C_I			2~6		3	10		10	pF

Timing Characteristics

Symbol	Characteristic		V_{CC}(V)	T_A = 25°C		T_A = -40°C to +85°C		Unit
				Min	Max	Min	Max	
F_{CLOCK}	Clock Frequency		2	0	6	0	5	MHz
			4.5	0	31	0	25	
			6	0	36	0	28	
t_W	Pulse Duration	$\overline{CLR}$ Low	2	100		125		ns
			4.5	20		25		
			6	17		21		
		CLK High or Low	2	80		100		
			4.5	16		20		
			6	14		18		
t_{SU}	Setup Time Before CLK	Data	2	100		125		ns
			4.5	20		25		
			6	17		21		
I_{CC}		$\overline{CLR}$ Inactive	2	100		125		
			4.5	20		25		
			6	17		21		
t_h	Hold Time, Data After CLK		2	5		5		ns
			4.5	5		5		
			6	5		5		

Switching characteristics (C_L = 50pF)

Symbol	From (Input)	To (Output)	V_{CC}(V)	T_A = 25℃			T_A = -40℃ to +85℃		Unit
				Min	Typ	Max	Min	Max	
F_{MAX}			2	6	10		5		MHz
			4.5	31	54		25		
			6	36	62		28		
t_{PHL}	$\overline{CLR}$	Any Q	2		140	205		255	ns
			4.5		28	41		51	
			6		24	35		46	
t_{pd}	CLK	Any Q	2		115	175		220	
			4.5		23	35		44	
			6		20	30		38	
t_t			2		38	75		95	ns
			4.5		8	15		19	
			6		6	13		16	

Operating characteristics (T_A = 25°C)

Symbol	Characteristic	Test Conditions	Typ	Unit
C_{pd}	Power Dissipation Capacitance	No Load	135	pF

Parameter Measurement Information

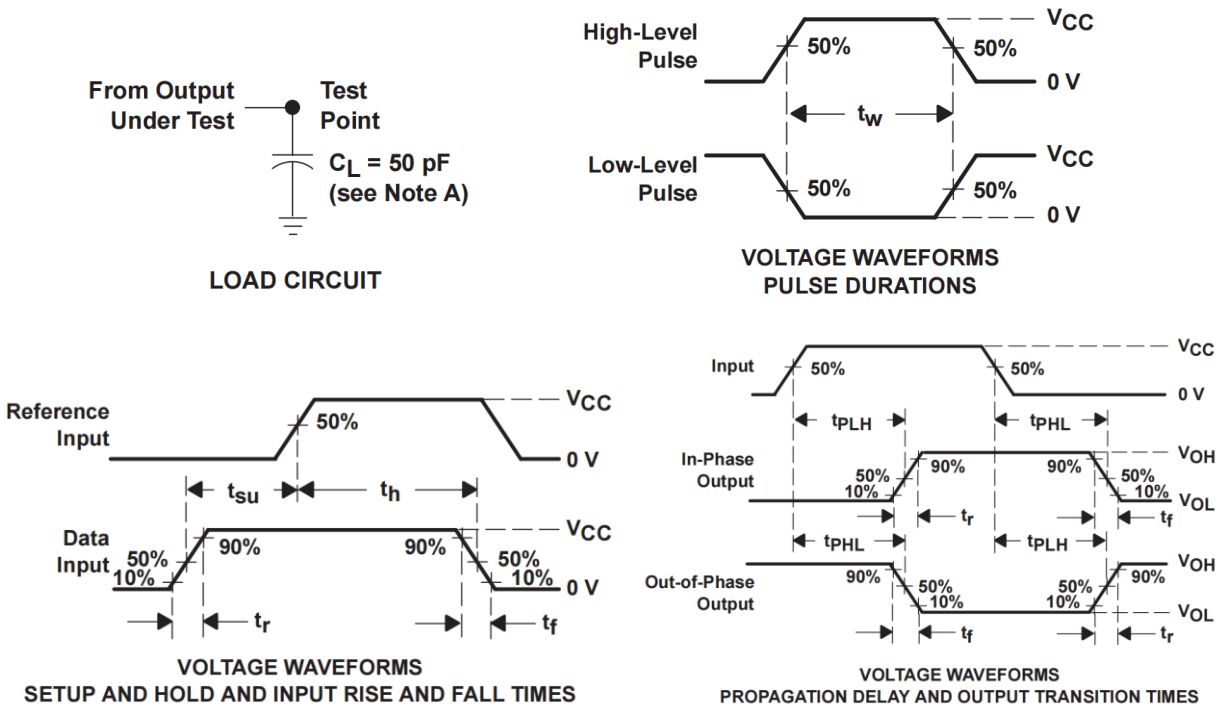
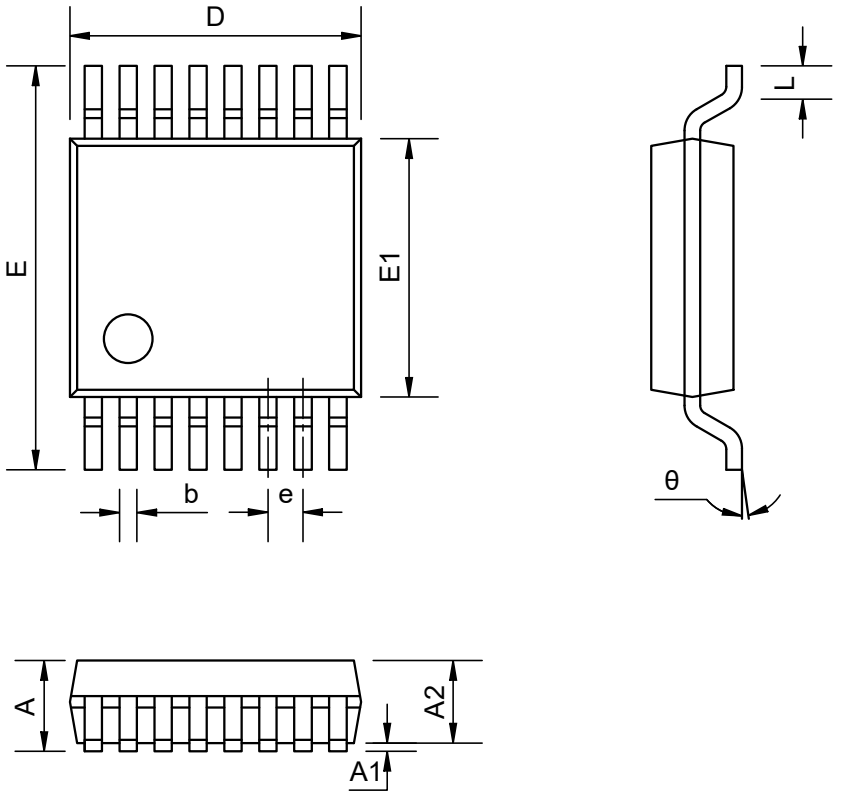


Figure5. Test Waveform

Note：

When using the circuit, in order to strengthen the anti-jamming ability, a capacitor of 100pF should be connected between the $\overline{CLR}$ and VCC or GND.

Package Dimension

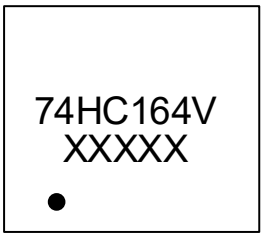


COMMON DIMENSIONS

(Units: mm)

SYMBOL	MIN	NOM	MAX
A	--	--	1.20
A1	0.05	--	0.15
A2	0.90	--	1.05
b	0.20	--	0.28
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
θ	0°	--	8°

Marking



74HC164V = Part Number

XXXXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2022-07-19	Original Version	Shi Bo	Shi Liang Jun	Shi Bo
1.1	2023-07-24	Update EC Table	Shi Bo	Ge Hao	Shi Bo
1.2	2024-08-12	Update EC Table	Shi Bo	Ge Hao	Shi Bo
1.2.a	2025-11-19	Add Marking	Yang Xiao Xu	Ge Hao	Liu Jia Ying