Dual-Bit, Dual Supply Voltage Level Translator/Transceiver; 3-State

General Description

The ET74AVCH2T45 is a dual-bit, dual-supply transceiver that enables bidirectional level translation. It features two data input-output ports (nA and nB), a direction control input (DIR) and dual-supply pins (VCC(A) and VCC(B)). Both VCC(A) and VCC(B) can be supplied at any voltage between 0.8V and 3.6V making the device suitable for translating between any of the low voltage nodes (0.8V, 1.2V, 1.8V and 3.3V). Pins nA and DIR are referenced to VCC(A) and pins nB are referenced to VCC(B). A HIGH on DIR allows transmission from nA to nB and a LOW on DIR allows transmission from nB to nA.

The device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In Suspend mode when either VCC(A) or VCC(B) are at GND level, both A and B are in the high-impedance OFF-state.

The ET74AVCH2T45 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

Features

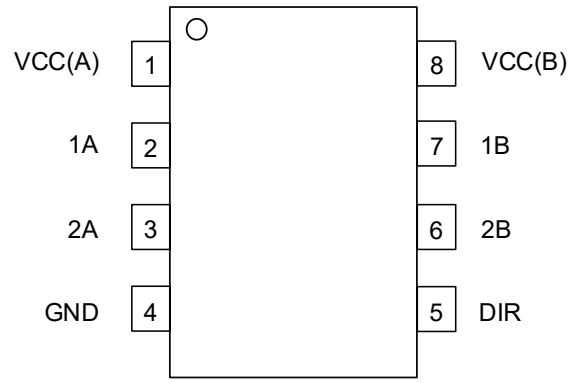
- Wide Supply Voltage Range:
  -- $V_{CC(A)}$: 0.8V to 3.6V
  -- $V_{CC(B)}$: 0.8V to 3.6V
- High Noise Immunity
- Maximum Data Rates:
  -- 500Mbit/s (1.8V to 3.3V Translation)
  -- 320Mbit/s (<1.8V to 3.3V Translation)
  -- 320Mbit/s (Translate to 2.5V or 1.8V)
  -- 280Mbit/s (Translate to 1.5V)
  -- 240Mbit/s (Translate to 1.2V)
- Bus Hold on Data Inputs
- Suspend Mode
- Over-voltage Tolerant Inputs Accept Voltages to 3.6V
- Low Noise Overshoot and Undershoot < 10% of V_{CC}
- I_{OFF} Circuitry Provides Partial Power-down Mode Operation
- ESD Protection Complies with JESD22 Standard
  -- HBM: ±4000V Pass (JEDEC JS-001)
  -- CDM: ±1500V Pass (JEDEC JS-002)
- Latch-up Performance Exceeds ±100mA per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET74AVCH2T45U	MSOP8 (3.0mm × 3.0mm)	Tape and Reel, 4K/Reel	3
ET74AVCH2T45U1	VSSOP8 (2.0mm × 2.3mm)	Tape and Reel, 3K/Reel	3

Applications

- Personal Electronic
- Industrial Equipment
- Enterprise Infrastructure
- Telecom Equipment

Pin Configuration



MSOP8/VSSOP8

Figure1. Pin Configuration

Pin Function

Pin		I/O	Description
Pin Name	Pin Number		
VCC(A)	1	-	Supply Voltage Pin of A Side (Referenced to Pin 1A, 2A and DIR)
1A	2	I/O	Data Input or Output
2A	3	I/O	Data Input or Output
GND	4	-	Ground (0V)
DIR	5	I	Direction Control
2B	6	I/O	Data Input or Output
1B	7	I/O	Data Input or Output
VCC(B)	8	-	Supply Voltage Pin of B Side (Referenced to Pin 1B and 2B)

Functional Diagram

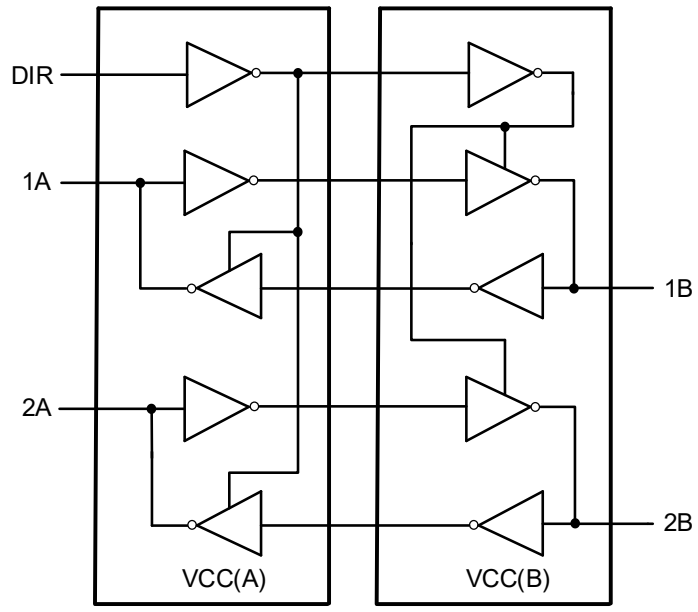


Figure2. Logic symbol

Function table

Supply Voltage	Input	Input/Output[1]	
$V_{CC(A)}$, $V_{CC(B)}$	DIR[2]	nA	nB
0.8V to 3.6V	L	nA = nB	Input
0.8V to 3.6V	H	Input	nB = nA
GND[3]	X	Hi-Z	Hi-Z

Note1: The input circuit of the data I/O is always active.

Note2: The DIR input circuit is referenced to VCC(A).

Note3: If at least one of VCC(A) or VCC(B) is at GND level, the device goes into suspend mode.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Value	Unit
$V_{CC(A)}$	Supply Voltage A Side (VCC(A) Pin)		-0.5~4.6	V
$V_{CC(B)}$	Supply Voltage B Side (VCC(B) Pin)		-0.5~4.6	V
I_{IK}	Input Clamping Current	V_I < 0V	-50	mA
V_I	Input Voltage[4]		-0.5~4.6	V
I_{OK}	Output Clamping Current	V_O < 0V	-50	mA
V_O	Output Voltage	Active Mode[4][5][6]	-0.5~V_{CCO} + 0.5	V
		Suspend or 3-state Mode[4]	-0.5~4.6	
I_O	Output Current	V_O = 0V to V_{CCO}	±50	mA
I_{CC}	Supply Current	Per VCC(A) or VCC(B) Pin	100	mA
I_{GND}	Ground Current	Per GND Pin	-100	mA
$T_{J(MAX)}$	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65~150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note4: The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

Note5: V_{CCO} + 0.5V should not exceed 4.6V.

Note6: V_{CCO} is the supply voltage associated with the output port.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	Supply Voltage A Side (VCC(A) Pin)		0.8	3.6	V
$V_{CC(B)}$	Supply Voltage B Side (VCC(B) Pin)		0.8	3.6	
V_I	Input Voltage		0	3.6	V
V_O	Output Voltage	Active State[6]	0	V_{CCO}	V
		Suspend or 3-State	0	3.6	
T_A	Ambient Temperature		-40	125	°C
Δt/ΔV	Input Transition Rise or Fall Rate	V_{CCI} [7] = 0.8V to 3.6V		5	ns/V

Note7: V_{CCI} is the supply voltage associated with the input port.

Electrical Characteristics

Typical static characteristics at T_A = 25°C (Unless otherwise noted)[6][7]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High-level Output Voltage	$V_I = V_{IH}$ or V_{IL} I_O = -1.5mA; $V_{CC(A)} = V_{CC(B)}$ = 0.8V		0.69		V
V_{OL}	Low-level Output Voltage	$V_I = V_{IH}$ or V_{IL} I_O = 1.5mA; $V_{CC(A)} = V_{CC(B)}$ = 0.8V		0.07		V
I_I	Input Leakage Current	DIR Input; V_I = 0V or 3.6V; $V_{CC(A)} = V_{CC(B)}$ = 0.8V to 3.6V		±0.025	±0.25	μA
I_{BHL}[8]	Bus Hold LOW Current	A or B port; V_I = 0.42V; $V_{CC(A)} = V_{CC(B)}$ = 1.2V		26		μA
I_{BHH}[8]	Bus Hold HIGH Current	A or B port; V_I = 0.78V; $V_{CC(A)} = V_{CC(B)}$ = 1.2V		-24		μA
I_{BHLO}[8] [9]	Bus Hold LOW Overdrive Current	$V_{CC(A)} = V_{CC(B)}$ = 1.2V		27		μA
I_{BHHO}[8] [9]	Bus Hold HIGH Overdrive Current	$V_{CC(A)} = V_{CC(B)}$ = 1.2V		-26		μA
I_{OZ}	Off-state Output Current	A or B Port; V_O = 0V or V_{CCO}; [6][10] $V_{CC(A)} = V_{CC(B)}$ = 0.8V to 3.6V		±0.5	±2.5	μA
I_{OFF}	Power-off Leakage Current	A Port; V_I or V_O = 0V to 3.6V; $V_{CC(A)}$ = 0V; $V_{CC(B)}$ = 0.8V to 3.6V		±0.1	±1	μA
		B Port; V_I or V_O = 0V to 3.6V; $V_{CC(B)}$ = 0V; $V_{CC(A)}$ = 0.8V to 3.6V		±0.1	±1	μA
C_I	Input Capacitance	DIR Input; V_I = 0V or 3.3V; $V_{CC(B)} = V_{CC(A)}$ = 3.3V		1.0		pF
$C_{I/O}$	Input/Output Capacitance	A and B Port; $V_O = V_{CCO}$ or GND; $V_{CC(A)} = V_{CC(B)}$ = 3.3V		4.0		pF

Electrical Characteristics (Continued)

Static characteristics[6][7]

Symbol	Parameter	Conditions		T_A = -40°C to 85°C		T_A = -40°C to 125°C		Unit
				Min	Max	Min	Max	
V_{IH}	High-level Input Voltage	Data Input[7]						
		V_{CCI} = 0.8V		0.7V_{CCI}		0.7V_{CCI}		V
		V_{CCI} = 1.1V to 1.95V		0.65V_{CCI}		0.65V_{CCI}		
		V_{CCI} = 2.3V to 2.7V		1.6		1.6		
		V_{CCI} = 3.0V to 3.6V		2.0		2.0		
		DIR Input						
		$V_{CC(A)}$ = 0.8V		0.7$V_{CC(A)}$		0.7$V_{CC(A)}$		V
		$V_{CC(A)}$ = 1.1V to 1.95V		0.65$V_{CC(A)}$		0.65$V_{CC(A)}$		
		$V_{CC(A)}$ = 2.3V to 2.7V		1.6		1.6		
		$V_{CC(A)}$ = 3.0V to 3.6V		2.0		2.0		
V_{IL}	Low-level Input Voltage	Data Input[7]						
		V_{CCI} = 0.8V			0.3V_{CCI}		0.3V_{CCI}	V
		V_{CCI} = 1.1V to 1.95V			0.35V_{CCI}		0.35V_{CCI}	
		V_{CCI} = 2.3V to 2.7V			0.7		0.7	
		V_{CCI} = 3.0V to 3.6V			0.9		0.9	
		DIR Input						
		$V_{CC(A)}$ = 0.8V			0.3$V_{CC(A)}$		0.3$V_{CC(A)}$	V
		$V_{CC(A)}$ = 1.1V to 1.95V			0.35$V_{CC(A)}$		0.35$V_{CC(A)}$	
		$V_{CC(A)}$ = 2.3V to 2.7V			0.7		0.7	
		$V_{CC(A)}$ = 3.0V to 3.6V			0.9		0.9	
V_{OH}	High-level Output Voltage	V_I = V_{IH} or V_{IL}[8]						
		I_O = -100µA	$V_{CC(A)}$ = $V_{CC(B)}$ = 0.8V to 3.6V	V_{CCO} - 0.1		V_{CCO} - 0.1		V
		I_O = -3mA	$V_{CC(A)}$ = $V_{CC(B)}$ = 1.2V	0.85		0.85		
		I_O = -6mA	$V_{CC(A)}$ = $V_{CC(B)}$ = 1.4V	1.05		1.05		
		I_O = -8mA	$V_{CC(A)}$ = $V_{CC(B)}$ = 1.65V	1.2		1.2		
		I_O = -9mA	$V_{CC(A)}$ = $V_{CC(B)}$ = 2.3V	1.75		1.75		
		I_O = -12mA	$V_{CC(A)}$ = $V_{CC(B)}$ = 3.0V	2.3		2.3		

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions		T_A = -40°C to 85°C		T_A = -40°C to 125°C		Unit
				Min	Max	Min	Max	
V_{OL}	Low-level Output Voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100μA	$V_{CC(A)}$ = $V_{CC(B)}$ = 0.8V to 3.6V		0.1		0.1	V
		I_O = 3mA	$V_{CC(A)}$ = $V_{CC(B)}$ = 1.2V		0.25		0.25	
		I_O = 6mA	$V_{CC(A)}$ = $V_{CC(B)}$ = 1.4V		0.35		0.35	
		I_O = 8mA	$V_{CC(A)}$ = $V_{CC(B)}$ = 1.65V		0.45		0.45	
		I_O = 9mA	$V_{CC(A)}$ = $V_{CC(B)}$ = 2.3V		0.55		0.55	
		I_O = 12mA	$V_{CC(A)}$ = $V_{CC(B)}$ = 3.0V		0.7		0.7	
I_I	Input Leakage Current	DIR Input; V_I = 0V or 3.6V	$V_{CC(A)}$ = $V_{CC(B)}$ = 0.8V to 3.6V		±1		±1.5	μA
I_{BHL}[(8)]	Bus Hold LOW Current	A or B Port						
		V_I = 0.49V	$V_{CC(A)}$ = $V_{CC(B)}$ = 1.4V	15		15		μA
		V_I = 0.58V	$V_{CC(A)}$ = $V_{CC(B)}$ = 1.65V	25		25		μA
		V_I = 0.70V	$V_{CC(A)}$ = $V_{CC(B)}$ = 2.3V	45		45		μA
		V_I = 0.80V	$V_{CC(A)}$ = $V_{CC(B)}$ = 3.3V	100		90		μA
I_{BHH}[(8)]	Bus Hold HIGH Current	A or B Port						
		V_I = 0.91V	$V_{CC(A)}$ = $V_{CC(B)}$ = 1.4V	-15		-15		μA
		V_I = 1.07V	$V_{CC(A)}$ = $V_{CC(B)}$ = 1.65V	-25		-25		μA
		V_I = 1.60V	$V_{CC(A)}$ = $V_{CC(B)}$ = 2.3V	-45		-45		μA
		V_I = 2.00V	$V_{CC(A)}$ = $V_{CC(B)}$ = 3.3V	-100		-100		μA

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions		T_A = -40°C to 85°C		T_A = -40°C to 125°C		Unit
				Min	Max	Min	Max	
I_{BHLO}[8] [9]	Bus Hold LOW Overdrive Current	A or B port						
		$V_{CC(A)}$ = $V_{CC(B)}$ = 1.4V		125		125		μA
		$V_{CC(A)}$ = $V_{CC(B)}$ = 1.65V		200		200		μA
		$V_{CC(A)}$ = $V_{CC(B)}$ = 2.3V		300		300		μA
		$V_{CC(A)}$ = $V_{CC(B)}$ = 3.3V		500		500		μA
I_{BHHO}[8] [9]	Bus Hold HIGH Overdrive Current	A or B port						
		$V_{CC(A)}$ = $V_{CC(B)}$ = 1.4V		-125		-125		μA
		$V_{CC(A)}$ = $V_{CC(B)}$ = 1.65V		-200		-200		μA
		$V_{CC(A)}$ = $V_{CC(B)}$ = 2.3V		-300		-300		μA
		$V_{CC(A)}$ = $V_{CC(B)}$ = 3.3V		-500		-500		μA
I_{OZ}	Off-state Output Current	A or B Port; V_O = 0V or V_{CCO};	$V_{CC(A)}$ = $V_{CC(B)}$ = 3.6V[6][10]		±5		±7.5	μA
I_{OFF}	Power-off Leakage Current	A Port; V_I or V_O = 0V to 3.6V;	$V_{CC(A)}$ = 0V; $V_{CC(B)}$ = 0.8V to 3.6V		±5		±35	μA
		B Port; V_I or V_O = 0V to 3.6V;	$V_{CC(B)}$ = 0V; $V_{CC(A)}$ = 0.8V to 3.6V		±5		±35	

Note8: '+/-' represents the direction of the current.

Note9: I_{BHL}, I_{BHH} means the bus hold current; I_{BHLO}, I_{BHHO} means the minimum overdrive current to flip the level.

Note10: For I/O ports, the parameter I_{OZ} includes the input leakage current.

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	T_A = -40°C to 85°C		T_A = -40°C to 125°C		Unit
			Min	Max	Min	Max	
I_{CC}	Supply Current	A Port; V_I = 0V or V_{CCI}; I_O = 0mA					
		$V_{CC(A)}$ = 0.8V to 3.6V; $V_{CC(B)}$ = 0.8V to 3.6V		8		11.5	μA
		$V_{CC(A)}$ = 3.6V; $V_{CC(B)}$ = 0V		8		11.5	μA
		$V_{CC(A)}$ = 0V; $V_{CC(B)}$ = 3.6V	-2		-8		μA
		B Port; V_I = 0V or V_{CCI}; I_O = 0mA					
		$V_{CC(A)}$ = 0.8V to 3.6V; $V_{CC(B)}$ = 0.8V to 3.6V		8		11.5	μA
		$V_{CC(A)}$ = 3.6V; $V_{CC(B)}$ = 0V	-2		-8		μA
		$V_{CC(A)}$ = 0V; $V_{CC(B)}$ = 3.6V		8		11.5	μA
		A Plus B Port ($I_{CC(A)}$ + $I_{CC(B)}$); V_I = 0V or V_{CCI}; I_O = 0mA; $V_{CC(A)}$ = 0.8V to 3.6V; $V_{CC(B)}$ = 0.8V to 3.6V		16		23	μA

Switching Characteristics

Typical power dissipation capacitance at $V_{CC(A)}$ = $V_{CC(B)}$ and T_A = 25°C (unless otherwise noted)[(11)(12)]

Symbol	Parameter	Conditions	$V_{CC(A)}$ = $V_{CC(B)}$						Unit
			0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	
C_{PD}	Power Dissipation Capacitance	A Port:(Direction A to B); B Port:(Direction B to A)	1	2	2	2	2	2	pF
		A Port:(Direction B to A); B Port:(Direction A to B)	9	11	11	12	14	17	pF

Note11: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}{}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = sum of outputs.

Note12: f_i = 10MHz; V_I = 0V to V_{CC}; t_r = t_f = 1ns; C_L = 0pF; R_L = ∞Ω.

Switching Characteristics (Continued)

Typical switching characteristics at $V_{CC(A)}$ = 0.8V and T_A = 25°C (unless otherwise noted)

For test circuit, see Figure5; for wave forms, see Figure3 and Figure4

Symbol	Parameter	Conditions	$V_{CC(B)}$				Unit
			0.8V	1.2V	1.8V	3.3V	
t_{pd}	Propagation Delay	A to B	15.8	8.4	8.0	9.5	ns
		B to A	15.8	12.7	12.2	11.8	ns
t_{dis}	Disable Time	DIR to A	23.6	23.6	23.6	23.6	ns
		DIR to B	20.6	15.6	12.7	11.6	ns
t_{en}	Enable Time	DIR to A	43.6	33.2	31	30.2	ns
		DIR to B	44.4	38.1	37.6	39.1	ns

Typical switching characteristics at $V_{CC(B)}$ = 0.8V and T_A = 25°C (unless otherwise noted)

For test circuit, see Figure5; for wave forms, see Figure3 and Figure4

Symbol	Parameter	Conditions	$V_{CC(A)}$				Unit
			0.8V	1.2V	1.8V	3.3V	
t_{pd}	Propagation Delay	A to B	15.8	12.7	12.2	11.8	ns
		B to A	15.8	8.4	8.0	9.5	ns
t_{dis}	Disable Time	DIR to A	23.6	12.4	5.6	3.0	ns
		DIR to B	20.6	19.6	18.6	18.0	ns
t_{en}	Enable Time	DIR to A	43.6	34.6	31.0	30.2	ns
		DIR to B	44.4	27.8	22.4	20.0	ns

Switching Characteristics: -40°C~85°C (Continued) (13)(14)

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			1.2V ± 0.1V		1.8V ± 0.15V		3.3V ± 0.3V		
			Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.1V to 1.3V									
t_{pd}	Propagation Delay	An to Bn	1.0	12.0	0.6	8.8	0.5	7.5	ns
		Bn to An	1.0	12.0	0.7	11.3	0.5	10.5	ns
t_{dis}	Disable Time	DIR to An	2.2	14.0	2.2	14.0	2.2	14.0	ns
		DIR to Bn	2.2	13.0	2.0	10.0	2.4	8.0	ns
t_{en}	Enable Time	DIR to An	-	35.0	-	33.1	-	31.1	ns
		DIR to Bn	-	34.0	-	30.0	-	29.5	ns
$V_{CC(A)}$ = 1.65V to 1.95V									
t_{pd}	Propagation Delay	An to Bn	0.5	11.3	0.5	7.5	0.5	6.5	ns
		Bn to An	0.5	10.0	0.5	7.5	0.5	7.1	ns
t_{dis}	Disable Time	DIR to An	1.6	10.0	1.6	10.0	1.6	10.0	ns
		DIR to Bn	2.0	11.0	1.4	8.0	1.5	6.0	ns
t_{en}	Enable Time	DIR to An	-	34.0	-	32.1	-	30.1	ns
		DIR to Bn	-	28.0	-	26.0	-	24.6	ns
$V_{CC(A)}$ = 3.0V to 3.6V									
t_{pd}	Propagation Delay	An to Bn	0.5	9.8	0.5	7.1	0.5	5.0	ns
		Bn to An	0.5	7.8	0.5	6.5	0.5	5.0	ns
t_{dis}	Disable Time	DIR to An	1.5	6.0	1.5	6.0	1.5	6.0	ns
		DIR to Bn	1.7	9.0	0.6	7.0	1.7	5.5	ns
t_{en}	Enable Time	DIR to An	-	31.0	-	28.0	-	27.1	ns
		DIR to Bn	-	26.0	-	24.0	-	23.7	ns

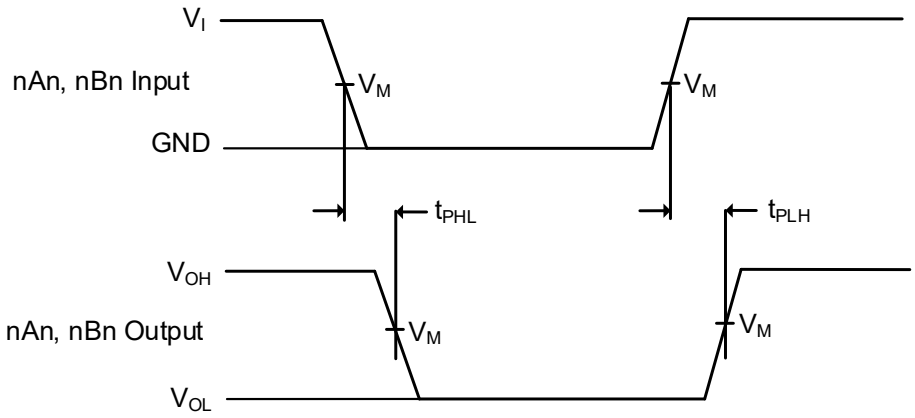
Switching Characteristics: -40°C~125°C (Continued) (13)(14)

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			1.2V ± 0.1V		1.8V ± 0.15V		3.3V ± 0.3V		
			Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.1V to 1.3V									
t_{pd}	Propagation Delay	An to Bn	1.0	12.0	0.6	8.8	0.5	7.5	ns
		Bn to An	1.0	12.0	0.7	11.3	0.5	10.5	ns
t_{dis}	Disable Time	DIR to An	2.2	14.9	2.2	14.9	2.2	14.9	ns
		DIR to Bn	2.2	13.9	2.0	10.9	2.4	8.9	ns
t_{en}	Enable Time	DIR to An	-	35.9	-	33.9	-	31.9	ns
		DIR to Bn	-	34.9	-	30.9	-	30.2	ns
$V_{CC(A)}$ = 1.65V to 1.95V									
t_{pd}	Propagation Delay	An to Bn	0.5	11.3	0.5	7.5	0.5	6.5	ns
		Bn to An	0.5	10.0	0.5	7.5	0.5	7.1	ns
t_{dis}	Disable Time	DIR to An	1.6	10.9	1.6	10.9	1.6	10.9	ns
		DIR to Bn	1.8	11.9	1.4	8.9	1.5	6.9	ns
t_{en}	Enable Time	DIR to An	-	34.9	-	32.9	-	30.9	ns
		DIR to Bn	-	28.9	-	26.9	-	25.4	ns
$V_{CC(A)}$ = 3.0V to 3.6V									
t_{pd}	Propagation Delay	An to Bn	0.5	9.8	0.5	7.1	0.5	5.0	ns
		Bn to An	0.5	7.8	0.5	6.5	0.5	5.0	ns
t_{dis}	Disable Time	DIR to An	1.5	6.9	1.5	6.9	1.5	6.9	ns
		DIR to Bn	1.7	9.9	0.6	7.9	1.7	6.4	ns
t_{en}	Enable Time	DIR to An	-	31.9	-	28.9	-	27.9	ns
		DIR to Bn	-	26.9	-	24.9	-	24.1	ns

Note13: t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

Note14: When testing ten, the An or Bn port needs to change its state after the Bn or An port has changed. When testing t_{dis}, the An or Bn port does not rely on the output state change of the other port to change.

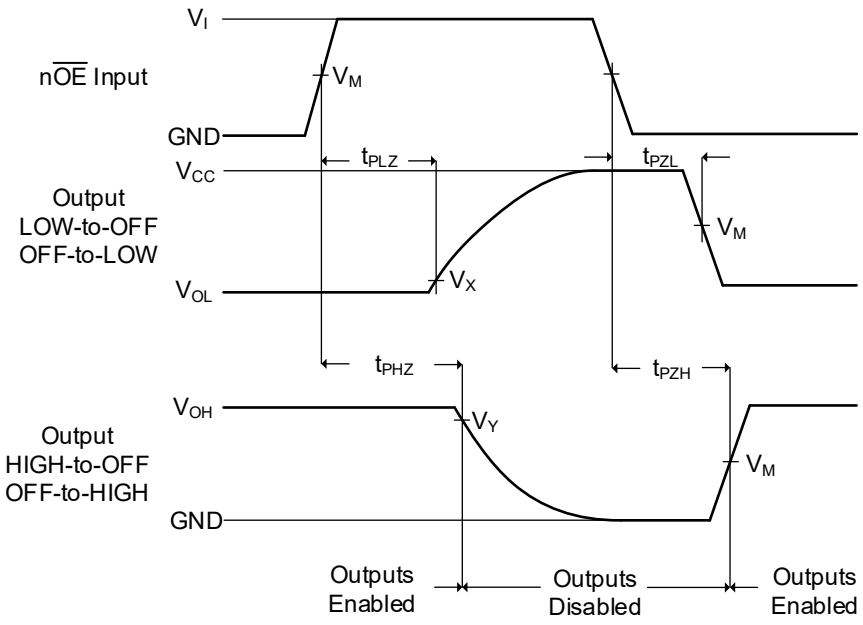
Test Circuit



Measurement points are given in Table 1.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure3. The data input (nAn, nBn) to output (nBn, nAn) propagation delay times



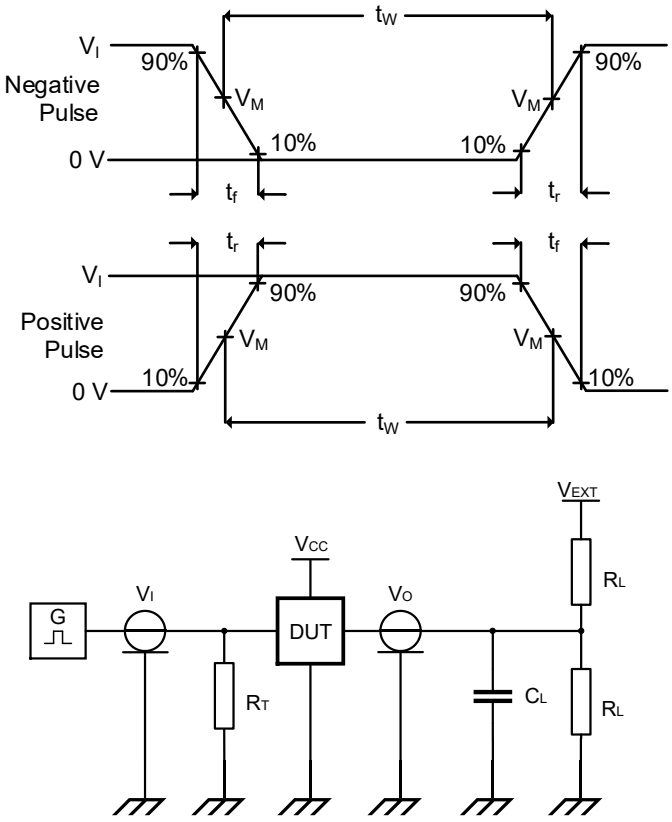
Measurement points are given in Table 1.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure4. Enable and disable times

Table 1. Measurement Points

Supply Voltage	Input	Output		
$V_{CC(A)}$, $V_{CC(B)}$	V_M	V_M	V_X	V_Y
0.8V to 1.6V	0.5 × V_{CCI}	0.5 × V_{CCO}	V_{OL} + 0.1V	V_{OH} - 0.1V
1.65V to 2.7V	0.5 × V_{CCI}	0.5 × V_{CCO}	V_{OL} + 0.15V	V_{OH} - 0.15V
3.0V to 3.6V	0.5 × V_{CCI}	0.5 × V_{CCO}	V_{OL} + 0.3V	V_{OH} - 0.3V



Measurement points are given in Table 2.

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

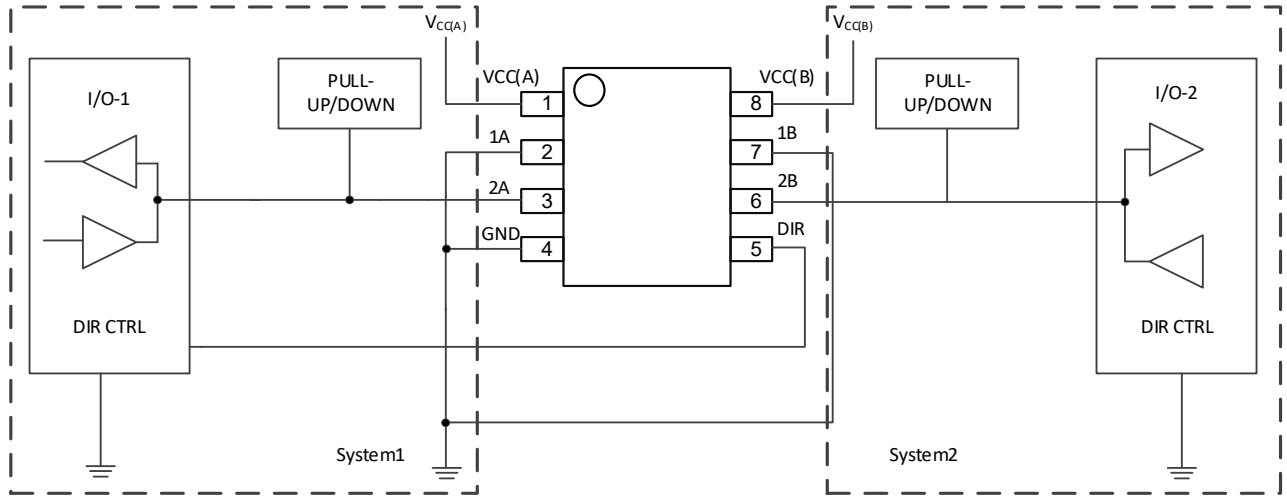
Figure5. Test circuit for measuring switching times

Table 2. Test Data

Supply Voltage	Input		Load		V_{EXT}		
$V_{CC(A)}$, $V_{CC(B)}$	V_I	$\Delta t/\Delta V$[15]	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
0.8V to 1.6V	V_{CCI}	≤ 1.0ns/V	15pF	2kΩ	Open	GND	2 × V_{CCO}
1.65V to 2.7V	V_{CCI}	≤ 1.0ns/V	15pF	2kΩ	Open	GND	2 × V_{CCO}
3.0V to 3.6V	V_{CCI}	≤ 1.0ns/V	15pF	2kΩ	Open	GND	2 × V_{CCO}

Note15: dV/dt ≥ 1.0V/ns

Application Circuits



Data transmission from System 1 to System 2 and then from System 2 to System 1:

State	DIR Ctrl	IO-1	IO-2	Description
1	H	Output	Input	System 1 data to System 2
2	H	Hi-Z	Hi-Z	System 2 is getting ready to send data to System 1. I/O-1 and I/O-2 are disabled. The bus line state depends on pull up or pull down. [16]
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pull up or pull down. [16]
4	L	Input	Output	System 2 data to System 1

Note16: System 1 and System 2 must use the same conditions, that is, both pull up or both pull down.

Calculate the enable times using the following formulas:

t_{PZH} (DIR to A) = t_{PLZ}(DIR to B) + t_{PLH} (B to A)

t_{PZL} (DIR to A) = t_{PHZ}(DIR to B) + t_{PHL} (B to A)

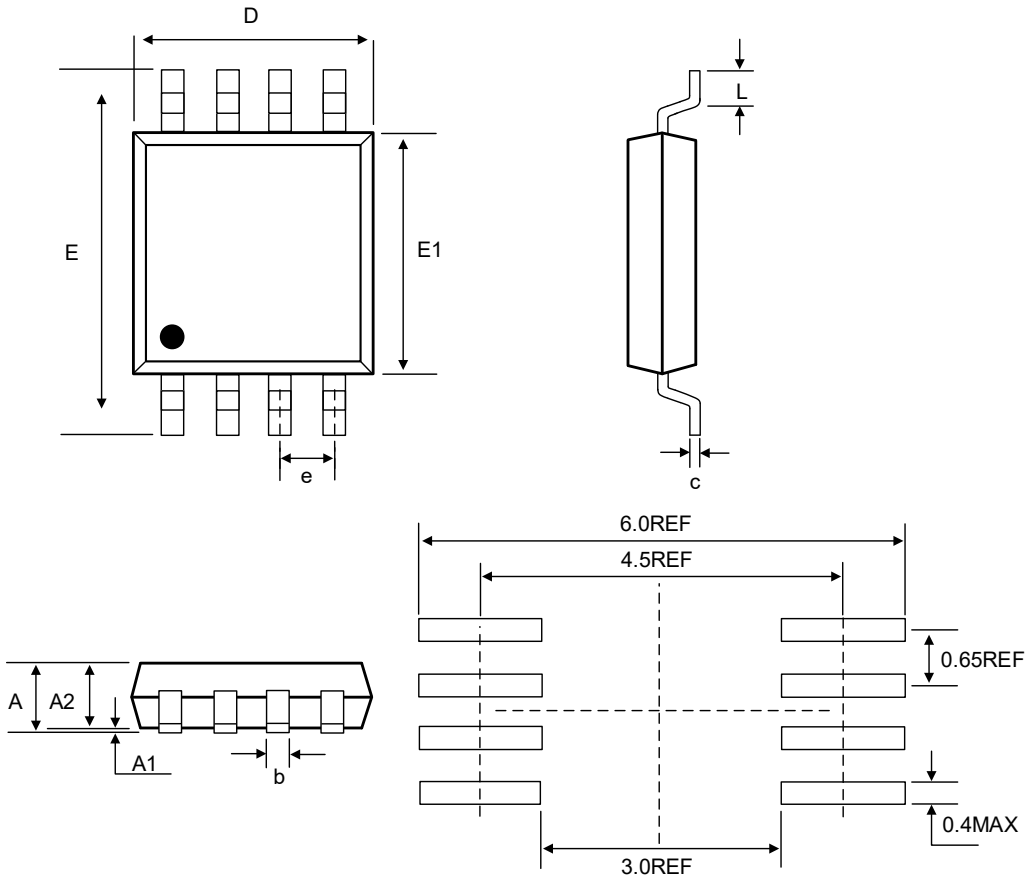
t_{PZH} (DIR to B) = t_{PLZ}(DIR to A) + t_{PLH} (A to B)

t_{PZL} (DIR to B) = t_{PHZ}(DIR to A) + t_{PHL} (A to B)

Figure6. Application Circuits

Package Dimension

MSOP8 (3.0mm × 3.0mm)

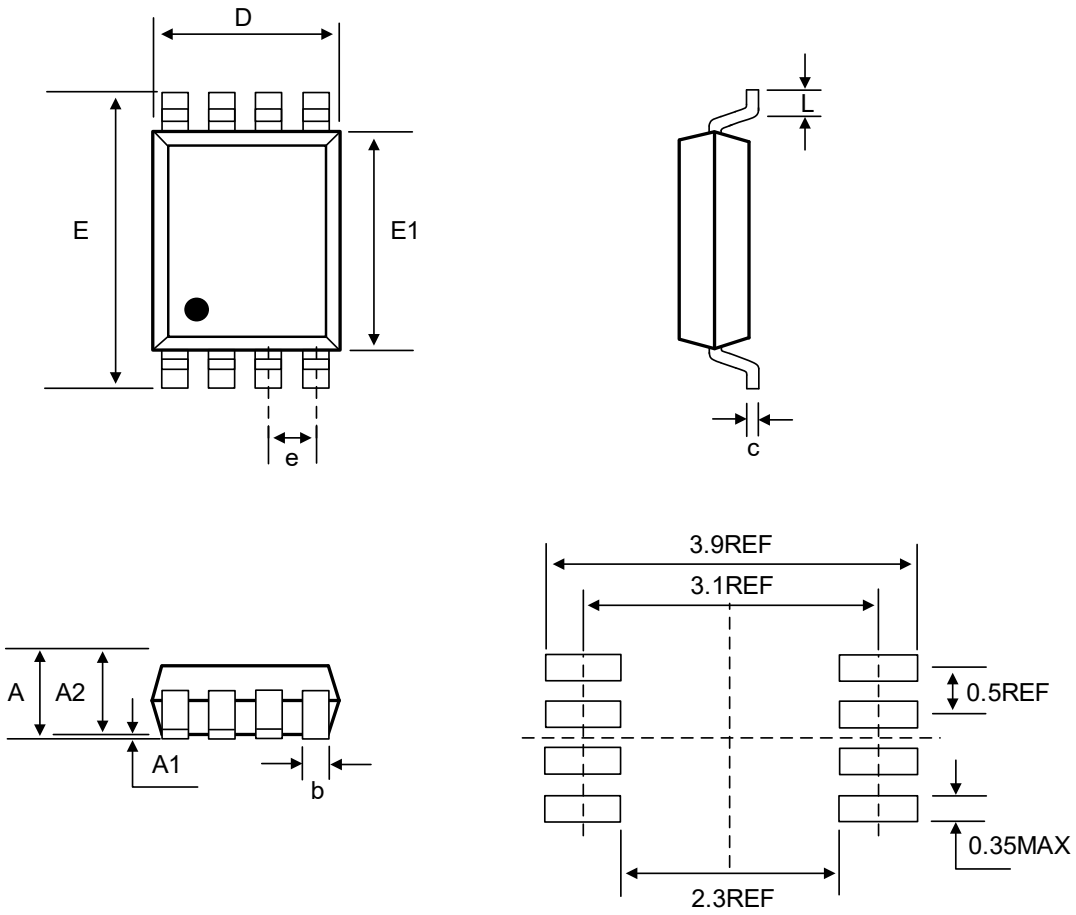


COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	-	0.15
A2	0.75	0.85	0.95
b	0.22	0.30	0.38
c	0.08	0.1	0.20
D	2.90	3.00	3.10
E	3.90	-	5.10
E1	2.90	3.00	3.10
e	0.65BSC		
L	0.33	-	0.7

VSSOP8 (2.0mm × 2.3mm)



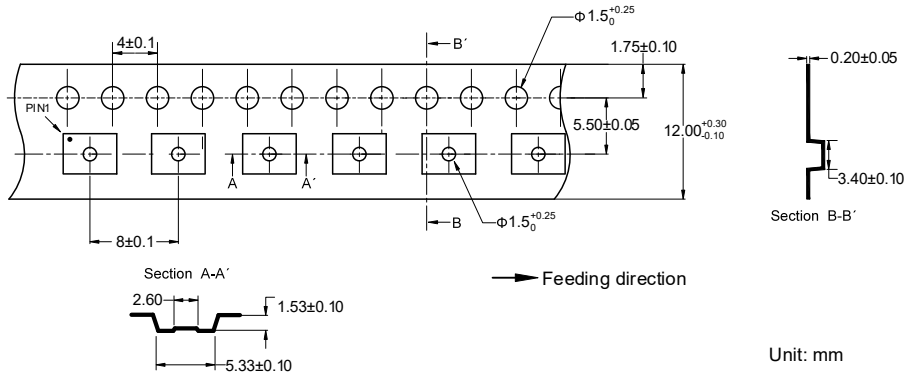
COMMON DIMENSIONS

(Unit: mm)

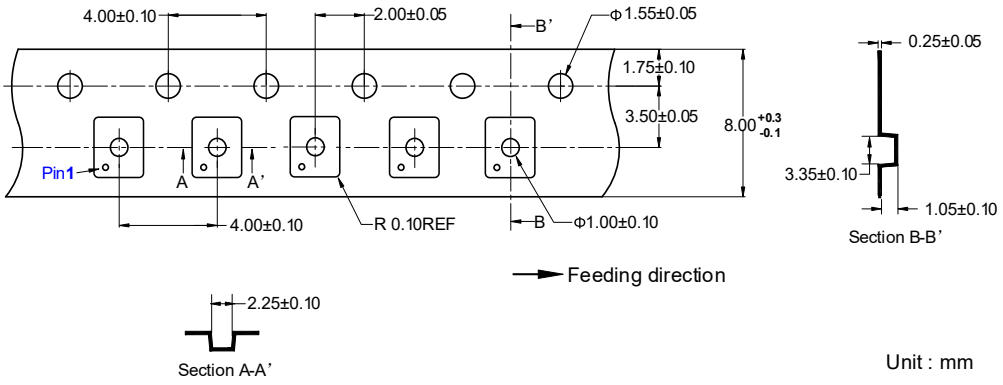
SYMBOL	MIN	NOM	MAX
A	-	-	0.90
A1	0.00	-	0.10
A2	0.65	0.75	0.80
b	0.17	-	0.27
c	0.08	-	0.20
D	1.90	2.00	2.10
E	3.00	3.10	3.20
E1	2.20	2.30	2.40
e	0.50BSC		
L	0.20	-	0.35

Tape Information

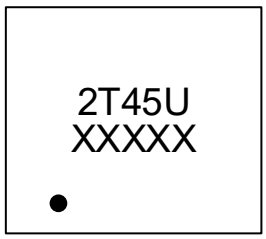
MSOP8 (3.0mm × 3.0mm)



VSSOP8 (2.0mm × 2.3mm)



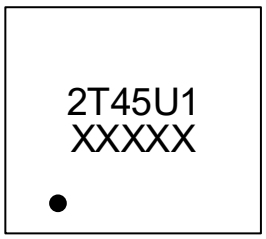
Marking Information



ET74AVCH2T45U

2T45U = Part Number

XXXXX = Tracking Number



ET74AVCH2T45U1

2T45U1 = Part Number

XXXXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2024-11-03	Preliminary Version	Li cheng	Tu guozhu	Liu jiaying
1.0	2025-03-20	Official Version	Wang anran	Yang xiaoxu	Liu jiaying
1.1	2025-05-14	Update EC Table	Wang anran	Yang xiaoxu	Liu jiaying
1.1.a	2025-09-24	Update Package	Yang xiaoxu	Yang xiaoxu	Liu jiaying
1.2	2025-10-20	Update Format	Wang anran	Yang xiaoxu	Liu jiaying
1.3	2025-10-24	Add MSOP8 TSSOP8 Package	Yang xiaoxu	Yang xiaoxu	Liu jiaying
1.3.a	2025-11-29	Delete TSSOP8 Package	Yang xiaoxu	Yang xiaoxu	Liu jiaying