1A Low Dropout LDO with Adjustable Output

General Description

The ET5A0ADJY1B is CMOS-based low-dropout, low-power linear regulators, offering 1A with low dropout voltage, high ripple rejection, high output accuracy and low supply current. The ET5A0ADJY1B consist of an accurate voltage-reference block, an error amplifier, a voltage-setting resistor net, a PMOSFET pass device, a thermal-shutdown circuit, and a current limit circuit with short protection.

The ET5A0ADJY1B use a type of outstanding CMOS process to minimize the supply current. A low on-resistance PMOS pass device is equipped for lower dropout voltage. ET5A0ADJY1B also possess the EN function to save more energy and extend the battery life.

The ET5A0ADJY1B can choose the output current 1.0A. The output voltage can be adjusted from 0.75V to 4.3V using two external resistors.

The ET5A0ADJY1B is available in the DFN6 package (1.5mm × 1.0mm).

Features

- Wide Input Voltage Range: 1.8V to 5.5V
- Output Current: 1.0A optional
- Adjustable Output Voltage Range: 0.75V to 4.3V
- Very Low I_Q: 125μA
- Excellent Load/Line Transient Response
- Line Regulation: 0.02% Typical
- Built-in Over-current Protection and Thermal Shutdown Circuit
- Built-in Auto-discharging Circuit
- Reverse Current Protection

Part No.	Package	MSL
ET5A0ADJY1B	DFN6 (1.5mm × 1.0mm)	Level 1

Applications

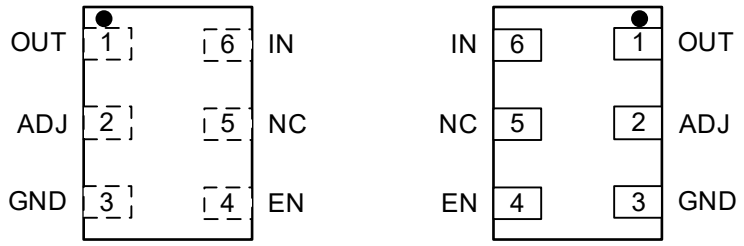
- Constant-voltage Power Supply for Battery-powered Device
- Constant-voltage Power Supply for TV, Notebook PC and Home Electric Appliance
- Constant-voltage Power Supply for Portable Equipment
- Label Information

Device Information

ET 5A0 ADJ Y1 B

Output Voltage		Package		Auto-discharging Function	
ADJ	Adjustable Output	**Y1**	DFN6 (1.5 × 1.0)	**B**	Available

Pin Configuration

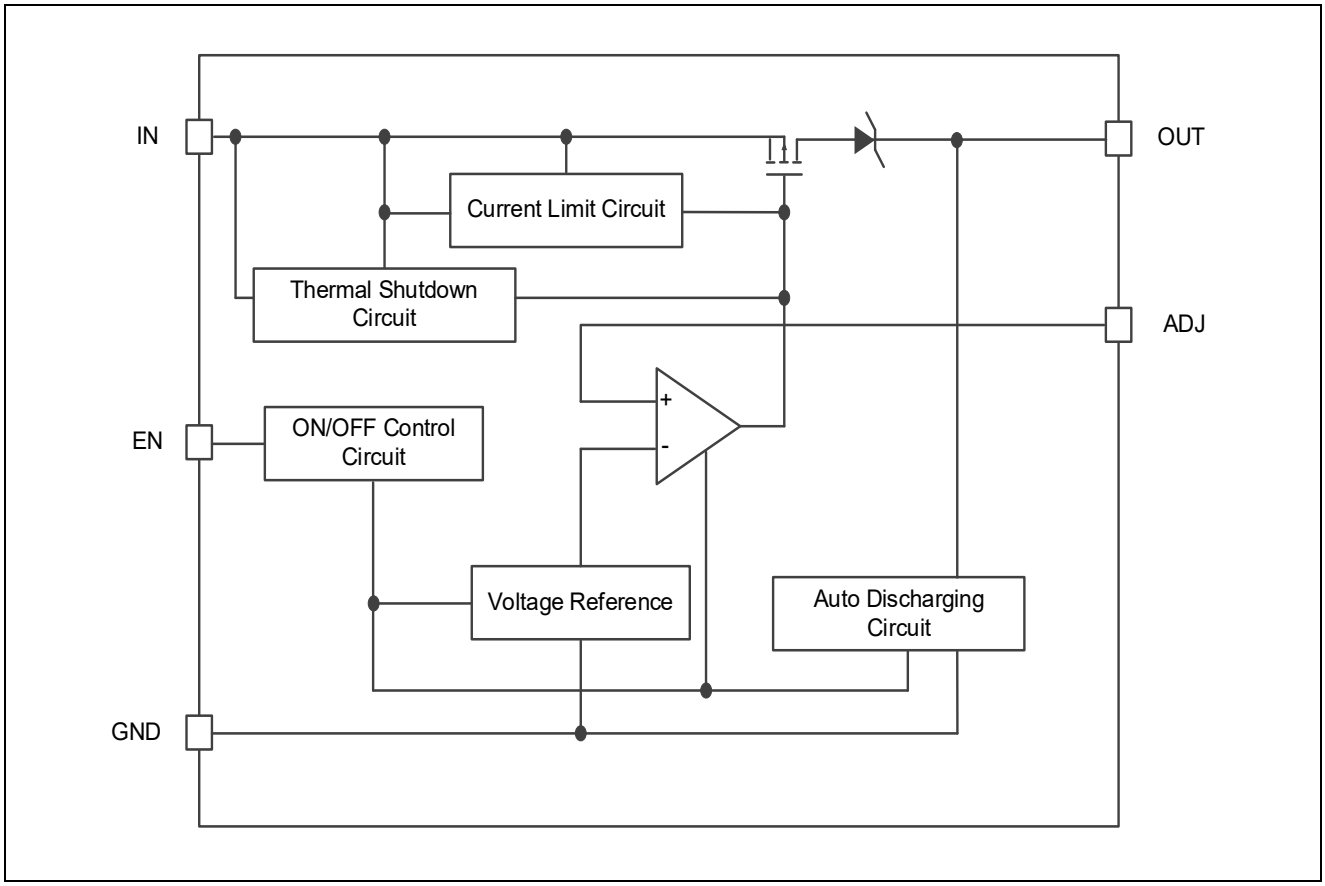


Top View Bottom View

Pin Function

Pin	Symbol	Pin Description
1	OUT	Output Pin
2	ADJ	Adjustable Regulator Feedback Input. Connect to output voltage resistor divider central node.
3	GND	Ground Pin
4	EN	Chip Enable Pin
5	NC	No Connect
6	IN	Input Pin

Block Diagram



Functional Description

Input Capacitor

A 1μF ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND.

Please pay attention, in the case of high impedance of the power supply, the input capacitance of the IC is small or the capacitor is not connected, the oscillation may occur. When the capacitance value of the output capacitor is greater than the capacitance value of the input capacitor, it is possible to generate oscillation.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is 1μF, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

EN Pin Operation

The ET5A0ADJY1B is turned on by setting the EN pin to “H”. When the EN pin is used, connect the EN pin with IN to keep the LDO in operating mode.

Current Limit Protection

When output current of OUT pin is higher than current limit threshold or the OUT pin is direct short to GND, the current limit protection will be triggered and clamp the output current at a predesigned level to prevent over-current and thermal damage. ET5A0ADJY1B output current limit will be 1.4A.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +155°C, allowing the device to cool down. When the junction temperature reduces to approximately +120°C the output circuit is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Reverse Current Protection Circuit

Under normal conditions, when V_{OUT} is higher than V_{IN}, the parasitic diode of Pch output transistor becomes forward direction. As a result, the current flows from OUT pin to IN pin.

The ET5A0ADJY1B switches the mode to the reverse current protection mode before V_{IN} becomes lower than V_{OUT} by connecting the parasitic diode of Pch output transistor to the backward direction, and connecting the gate to OUT pin. As a result, the Pch output transistor is turned off. However, from OUT pin to GND pin, via the internal divider resistors, very small current IREV flows.

Auto Discharging

When the EN pin set to “L”, the output circuit will be disable immediately, and the Auto-Discharging circuit will be turned on to discharge the electric charge on output capacitor, and decrease the voltage of V_{OUT} in very short time. The Auto-Discharging function is optional.

Output Voltage

The output voltage is adjustable using external 2-resistors. For better performance of the circuit, the R2 value need to be between 30kΩ and 100kΩ. The output voltage is calculated by:

$$\mathbf{V_{OUT} = (1 + R1 / R2) \times 0.75\ (V)}$$

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Rating	Unit
V_{IN}	Input Voltage	-0.3 to 6	V
V_{EN}	Input Voltage (EN Pin)	-0.3 to 6	V
V_{OUT}	Output Voltage	-0.3 to VIN + 0.3	V
I_{MAX}	Maximum Load Current	1000	mA
P_D	Maximum Power Consumption	1000	mW
T_J	Operating Junction Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-65 to 150	°C
T_{SOLD}	Lead Temperature (Soldering, 5sec)	260	°C
ESD	HBM(JEDEC JS-001)	±4000	V
	CDM(JEDEC JS-002)	±1500	V

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	1.8 to 5.5	V
I_{OUT}	Output Current	0 to 1000	mA
T_A	Operating Ambient Temperature	-40 to 85	°C
C_{IN}	Effective Input Ceramic Capacitor Value	1 to 10	μF
C_{OUT}	Effective Output Ceramic Capacitor Value	1 to 10	μF
ESR	Input and Output Capacitor Equivalent Series Resistance	5 to 100	mΩ

Electrical Characteristics

(Unless otherwise noted, V_{IN} = V_{SET} + 1.0V, T_A = -40°C ~ 85°C, C_{IN} = C_{OUT} = 1uF (effective capacitance [4]); Typical values are at V_{IN} = V_{SET} + 1.0V, T_A = 25°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN} [1]	Input Voltage Operation Range	$V_{IN} \geq V_{SET}$ + 0.5V	1.8		5.5	V
V_{OUT}	Output Voltage	I_{OUT} = 1mA, T_A = 25°C	×0.98		×1.02	V
		I_{OUT} = 1mA~1A, T_A = 25°C	-40		+40	mV
V_{DROP} [2]	Dropout Voltage	V_{OUT} = 3.3V, I_{OUT} = 1A, V_{OUT} Dropping to 0.98 × V_{OUT}	80	150	200	mV
I_{Q_ON}	Supply Quiescent Current	Active Mode: V_{EN} = High, I_{OUT} = 0mA	70	125	150	μA
$I_{Q\ OFF}$	Supply Shutdown Current	V_{EN} = 0V		1	3	μA
Reg_{LINE}	Output Voltage Line Regulation	V_{SET} + 0.5V ≤ V_{IN} ≤ 5.5V (V_{IN} ≥ 1.8V), I_{OUT} = 10mA (ΔV_{OUT} / ΔV_{IN} / V_{OUT})		0.02	0.1	%/V
Reg_{LOAD}	Output Voltage Load Regulation	I_{OUT} from 1mA to 1A V_{IN} = V_{SET} + 0.5V (ΔV_{OUT})		20	40	mV
V_{TRLN} [3]	Line Transient (The absolute value of the output change)	V_{OUT} = 3.3V, I_{OUT} = 1mA, V_{IN} = 4.3V to 5.5V in 10us, T_A = 25°C		15	30	mv
		V_{OUT} = 3.3V, I_{OUT} = 1mA, V_{IN} = 5.5V to 4.3V in 10us, T_A = 25°C		15	30	
V_{TRLD} [3]	Load Transient (The absolute value of the output change)	V_{OUT} = 3.3V, V_{IN} = 4.3V, I_{OUT} from 1mA to 1000mA in 10us, T_A = 25°C		75	120	mv
		V_{OUT} = 3.3V, V_{IN} = 4.3V, I_{OUT} from 1000mA to 1mA in 10us, T_A = 25°C		75	120	
I_{OUT}	Output Current		1000			mA
I_{LMT}	Over Current Limit	V_{OUT} = 3.3V, V_{IN} = 4.3V, T_A = 25°C	1050	1400	1900	mA
I_{SHORT}	Short Current Limit	V_{OUT} = 0V, T_A = 25°C	60	130	200	mA
I_{RUSH}	Inrush Current Limit	V_{OUT} = 3.3V, V_{IN} = 4.3V, T_A = 25°C	400	600	800	mA
PSRR [3]	Power Supply Rejection Ratio	f = 1kHz, C_{OUT} = 1μF, I_{OUT} = 20mA, V_{IN} = 4.3V, T_A = 25°C		70		dB
e_N [3]	Output Noise	10Hz to 100kHz, I_{OUT} = 30mA, C_{OUT} = 1μF, T_A = 25°C		50* V_{OUT}	80* V_{OUT}	μV_{RMS}
V_{IL}	EN Low Threshold	V_{IN} = 1.8 to 5.5V			0.3	V
V_{IH}	EN High Threshold	V_{IN} = 1.8 to 5.5V	1			V
I_{EN}	EN Pull-down Current	V_{IN} = 4.3V, V_{EN} = 4.3V, T_A = 25°C		0.3	1	μA

Electrical Characteristics (Continued)

(Unless otherwise noted, V_{IN} = V_{SET} + 1.0V, Ta = -40°C ~ 85°C, C_{IN} = C_{OUT} = 1uF (effective capacitance [4]); Typical values are at V_{IN} = V_{SET} + 1.0V, Ta = 25°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
R_{LOW}	Output Resistance of Auto Discharge at Off State	V_{EN} = 0V, V_{IN} = 4V, V_{OUT} = 3V	30	60	100	Ω
T_{TSD} [3]	Thermal Shutdown Temperature	Junction Temperature Rising	135	155	175	°C
T_{HYS} [3]	Thermal Shutdown Released Hysteresis	Junction Temperature falling from shutdown	20	40	60	°C

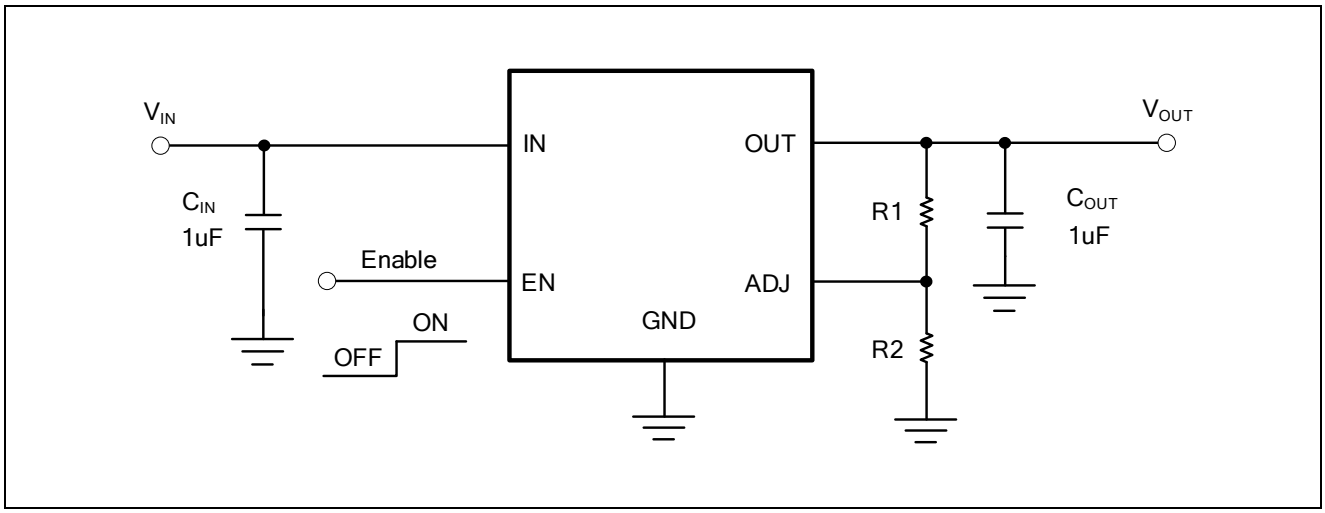
Note (1): V_{IN} means internal circuit can work normal. If V_{IN} < V_{OUT}, Reverse current protection circuit will work.

Note (2): V_{DROP} FT test method: test the V_{OUT} voltage at V_{SET} + $V_{DROPMAX}$ with output current.

Note (3): Guaranteed by design and characterization. not a FT item.

Note (4): Effective capacitance, including the effect of DC bias, tolerance and temperature.

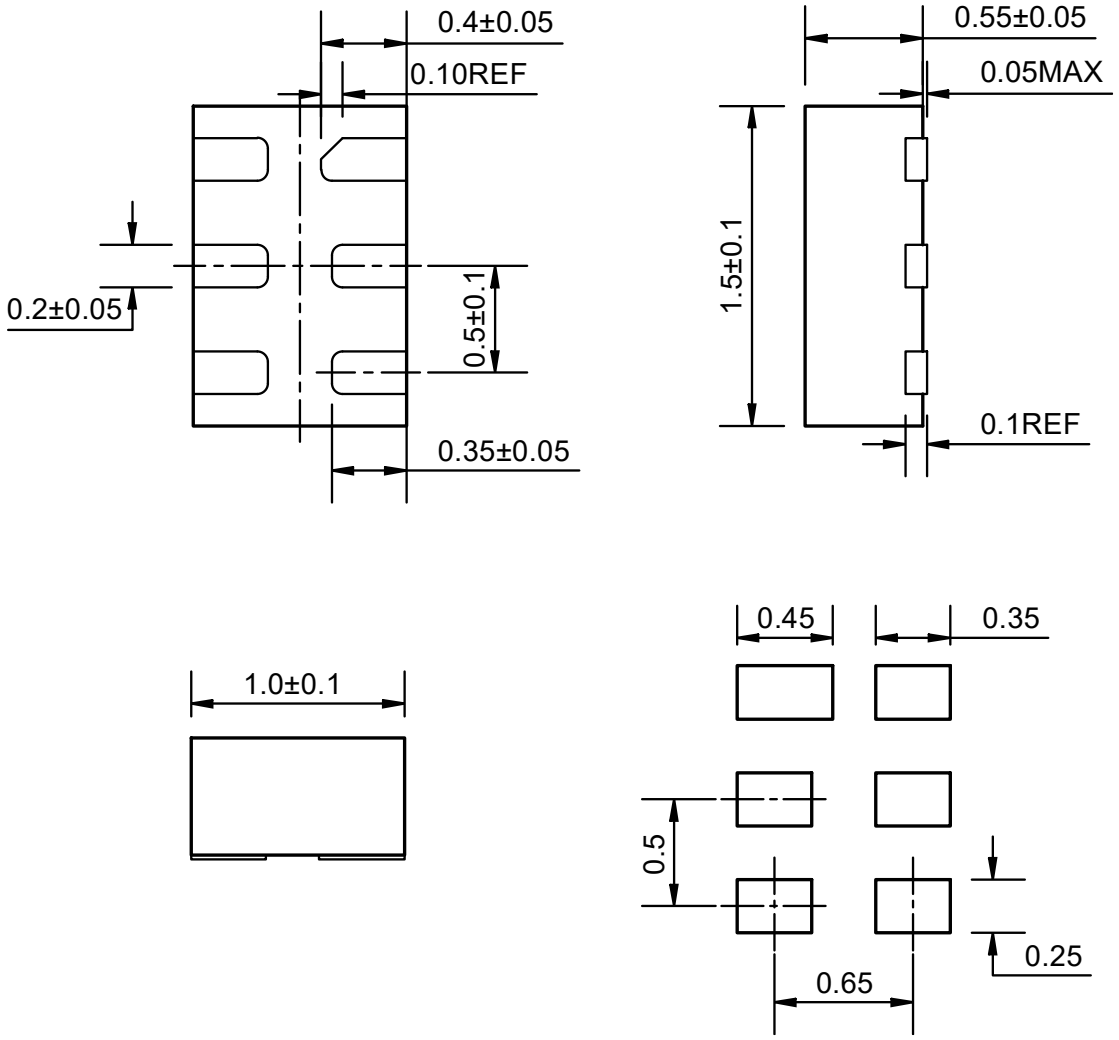
Application Circuits



*: V_{OUT}= (1 + R1 / R2) × 0.75V, R2 recommend 30KΩ ~ 100KΩ.

Package Dimension

DFN6



Recommended Land Pattern

Unit: mm

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2022-08-18	Initial version	Shibo	Liuyg	Liujy
1.0.a	2026-03-07	Update Format	Yuyifan	Liuyg	Liujy