Constant Current Matrix LED Driving Circuit

General Description

ET62181 is an array type constant current LED driver circuit, which has 32 steps constant current global adjustment function, and supports up to 8×8 matrix output. Each point has 256 steps PWM current adjustment function.

ET62181 internal integration of MCU digital interface, data latch, RAM, PWM constant current drive module. It is mainly used in the display driver of household appliances, with the advantages of rich display effect and simple operation.

Features

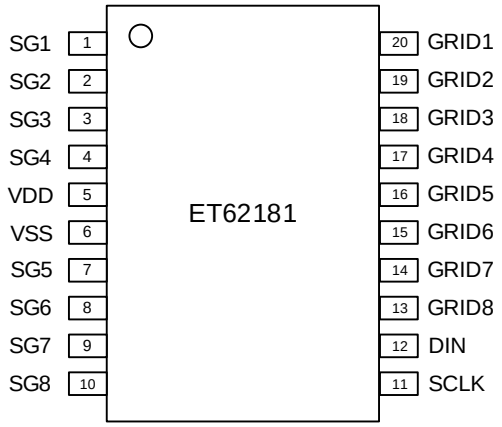
- 8 constant current driver channels, max output current 32mA.
- Support 1～8 scan application, the maximum application matrix is 8×8
- Each point supports 256 steps brightness adjustment
- Two wire serial interface(SCLK，DIN)
- Built in RC oscillation
- Built in power on reset circuit
- Built in automatic blanking circuit
- Part Number and Package

Part No.	Package	Pack
ET62181	SOP20	Default material tube packaging Tape packaging suffix -TR
ET62181V	TSSOP20	

Application

- LED Matrix driver
- Digital tube driver

Pin Assignments



Top View (SOP20/TSSOP20)

Pin Function

Pin No.	Name	Function
1~4,7~10	SG1~SG8	Segment output, connected to LED anode.
5	VDD	Power supply.
6	VSS	GND
11	SCLK	Clock input, enter data on the rising edge.
12	DIN	Serial data input, the input data changes at the low level of SCLK and is transmitted at the high level of SCLK.
13~20	GRID8~GRID1	Grid output, connected to LED cathode.

Absolute Maximum Ratings (Unless otherwise noted ,T_A=25°C)

Symbol	Characteristic	Rating	Unit
V_{DD}	Supply voltage	-0.5~7.0	V
V_I	Input Voltage	-0.5~V_{DD}+0.5	V
I_{O1}	LED SEG drive output current	-35	mA
I_{O2}	LED GRID drive output current	400	mA
P_D	Power Dissipation (SOP20)	450	mW
	Power Dissipation (TSSOP20)	450	mW
T_J	Junction Temperature	-40～150	°C
T_A	Operating Temperature	-40～85	°C
T_{STG}	Storing Temperature	-65～150	°C
V_{ESD}	HBM (All Pins)	±4.0	KV
	CDM (All Pins)	±1.0	KV

Electrical Characteristics (Unless otherwise noted， V_{DD}=5V ,T_A=25°C)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
DC Characteristics						
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{IH}	Logic high level	SCLK，DIN	0.7*V_{DD}		V_{DD}	V
V_{IL}	Logic low level	SCLK，DIN	0		0.3*V_{DD}	V
I_I	Input current	SCLK，DIN：V_I=V_{DD}	-	-	±1	μA
I_{OH}	LED SEG drive output current	SG1~SG8,V_O=V_{DD}-1V	-29	-32	-35	mA
I_{OL}	LED GRID drive output current	GRID1~GRID8,V_O=0.3V	250		-	mA
I_{DD_DYN}	Dynamic current Dissipation	No load, Display off	-	-	5	mA
Switch Characteristics						
Fosc	Oscillation frequency			1		MHz
T_{TZH1}	GRID1~GRID8 rising time	C_L=300pF,R_L=1K			2	μs
T_{TZH2}	SEG1~SEG8 rising time				0.5	μs
T_{THZ}	Dropping time	C_L=300pF, SGn, GRIDn			120	μs
C_I	Input capacitance				15	pF
Timing Characteristics						
PW_{CLK}	Clock pulse width		400	-	-	ns
t_{SETUP}	Data setup time		100	-	-	ns
t_{HOLD}	Data hold time		100	-	-	ns

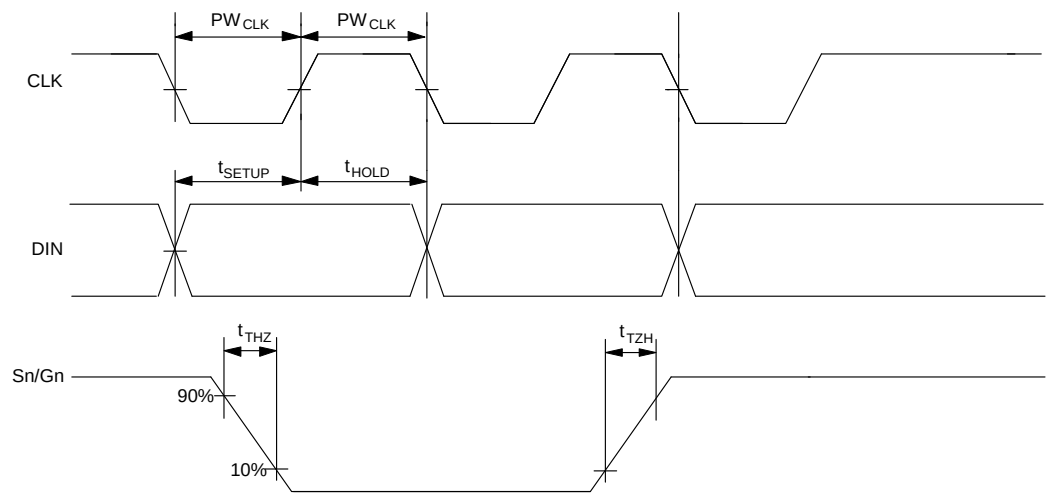


Figure1. Timing Diagram

Functions Description

1. Serial Port Interface

The data of MCU communicates with ET62181 through two-wire bus interface. While input data, when SCLK is high level, the signal on DIN must remain unchanged; only when the clock signal on SCLK is low level, the signal on DIN can be changed. The input of data is always high in the front and low in the back. The start condition of data input is that din changes from high to low when SCLK is high, and the end condition is that din changes from low to high when SCLK is high.

The instruction data transmission process is shown in the figure below：

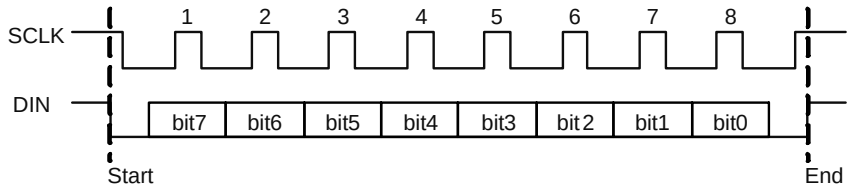


Figure 2. Instruction data transmission format

Write SRAM data address continuous write mode (First address must be 0X00)：

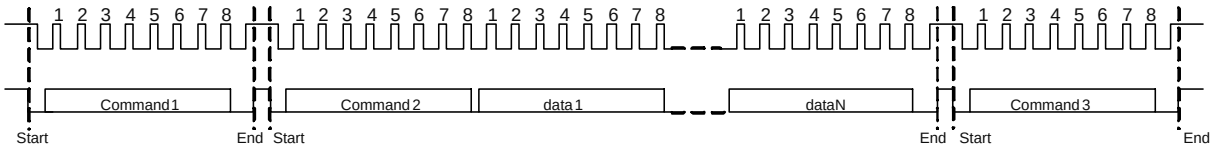


Figure 3. Automatic address continuous write data format

Command1： Set data

Command2：Set address

Data1~N：Transmit display data

Command3：Control display

Write SRAM data to fixed address mode：

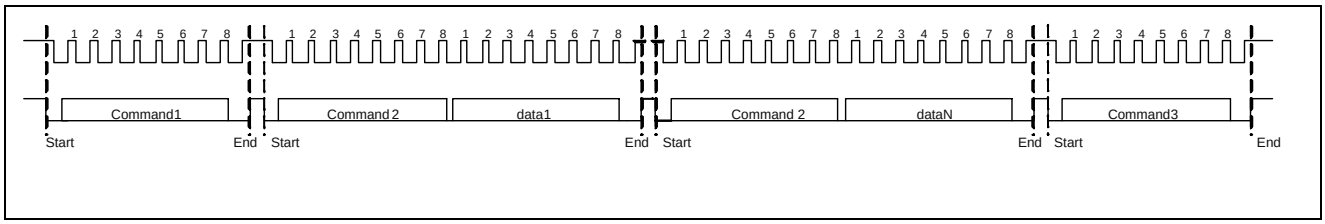


Figure 4. Write SRAM data to fixed address format

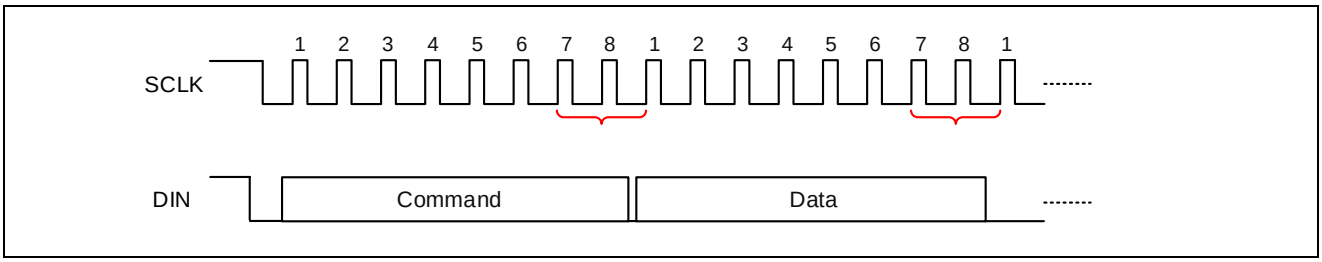
Command1：Set data

Command2：Set address

Data1~N：Transmit display data

Command3：Control display

Note1：Before using fixed address write mode, SRAM needs to be initialized with continuous write mode.



Note2：Since the ET62181 occupies its internal display module during the seventh and eighth clock cycles of a set of commands/data, if the host suspends communication during this period, it will cause the display to temporarily shut down.

2. Data Instruction

The command is used to set the display mode and the status of the LED driver. After the instruction start is valid, the first byte entered by DIN is regarded as an instruction. After decoding, the highest B7 and B6 bits are selected to distinguish different instructions.

B7	B6	Instruction
0	0	Initialization Setting
0	1	Data Instruction
1	0	Display Control Instruction setting
1	1	Address Instruction setting

Table 1. Instruction setting classification

If end is valid during instruction or data transmission, serial communication is initialized and the instruction or data being transmitted is invalid (the instruction or data previously transmitted remains valid).

2.1 Data Command Set

Before writing display data, send data instruction. The data instruction sets the number of scan lines, which determines the range of SRAM address, the number of write data, and the final display cycle.

Address mode：Automatic address mode means that the address is automatically accumulated from 00h when writing data. The maximum address value depends on the number of scanning lines. The fixed address

mode is to use the address in the address setting command to write data.

B7	B6	B5	B4	B3	B2	B1	B0	Description
0	1	0	0	0		0		1scan line
		0	0	1				2 scan line
		0	1	0				3 scan line
		0	1	1				4 scan line
		1	0	0				5 scan line
		1	0	1				6 scan line
		1	1	0				7 scan line
		1	1	1				8 scan line
					0			Automatic address mode
					1			Fixed address mode
							0	Force update mode
							1	Automatic update mode

Table 2. Data Instruction setting

2.2 Address Instruction Setting

B7	B6	B5	B4	B3	B2	B1	B0	Display Address
1	1	0	0	0	0	0	0	00H
1	1	0	0	0	0	0	1	01H
1	1	~	~	~	~	~	~	~
1	1	1	1	1	1	1	0	3EH
1	1	1	1	1	1	1	1	3FH

Table 3. Display Address Instruction Setting

Note: When power on, the address is set to 00H by default.

The corresponding relationship among display data, chip pins and display addresses is shown in the table below：

SEG8 Bit7~Bit0	SEG7 Bit7~Bit0	SEG6 Bit7~Bit0	SEG5 Bit7~Bit0	SEG4 Bit7~Bit0	SEG3 Bit7~Bit0	SEG2 Bit7~Bit0	SEG1 Bit7~Bit0	
07H	06H	05H	04H	03H	02H	01H	00H	**GRID1**
0FH	0EH	0DH	0CH	0BH	0AH	09H	08H	**GRID2**
17H	16H	15H	14H	13H	12H	11H	10H	**GRID3**
1FH	1EH	1DH	1CH	1BH	1AH	19H	18H	**GRID4**
27H	26H	25H	24H	23H	22H	21H	20H	**GRID5**
2FH	2EH	2DH	2CH	2BH	2AH	29H	28H	**GRID6**
37H	36H	35H	34H	33H	32H	31H	30H	**GRID7**
3FH	3EH	3DH	3CH	3BH	3AH	39H	38H	**GRID8**

Table 4. Display the corresponding relationship among data, address and chip pin

2.3 Display Control Instruction

B7	B6	B5	B4	B3	B2	B1	B0	Description
1	0	0	0	0	0			Display Off
				1				Display on
						0	0	Line feed time: 4 PWM clock cycles
						0	1	Line feed time: 8 PWM clock cycles
						1	0	Line feed time: 12 PWM clock cycles
						1	1	Line feed time: 16 PWM clock cycles

Table 5. Display Control Instruction

Note: Display cycle: Number of scanning lines × (line feed time + 256 steps PWM cycle)

2.4 Initialization Setting

After the system is powered on, the initialization setting command is sent first. The initialization setting command can be used to adjust the SEG current (high level output current).

B7	B6	B5	B4	B3	B2	B1	B0	SEG current gain factor(G)
0	0	0	1	0	0	1	0	20
0	0	0	1	1	1	1	1	32

Table 6. Initialization setting instruction

Note: After the system is powered on, the initialization setting command is sent first.

3. Display Cycle

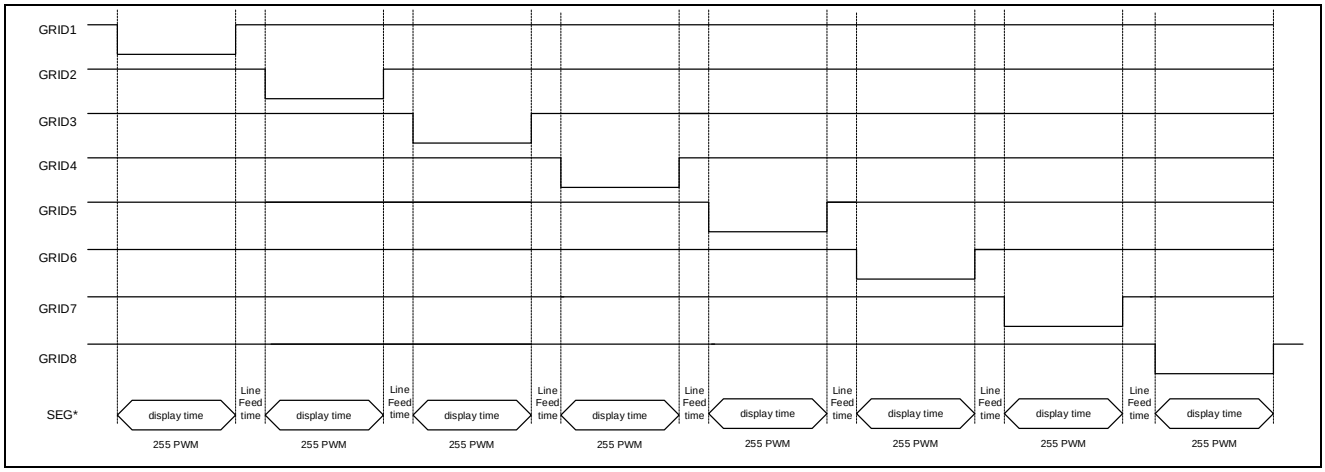
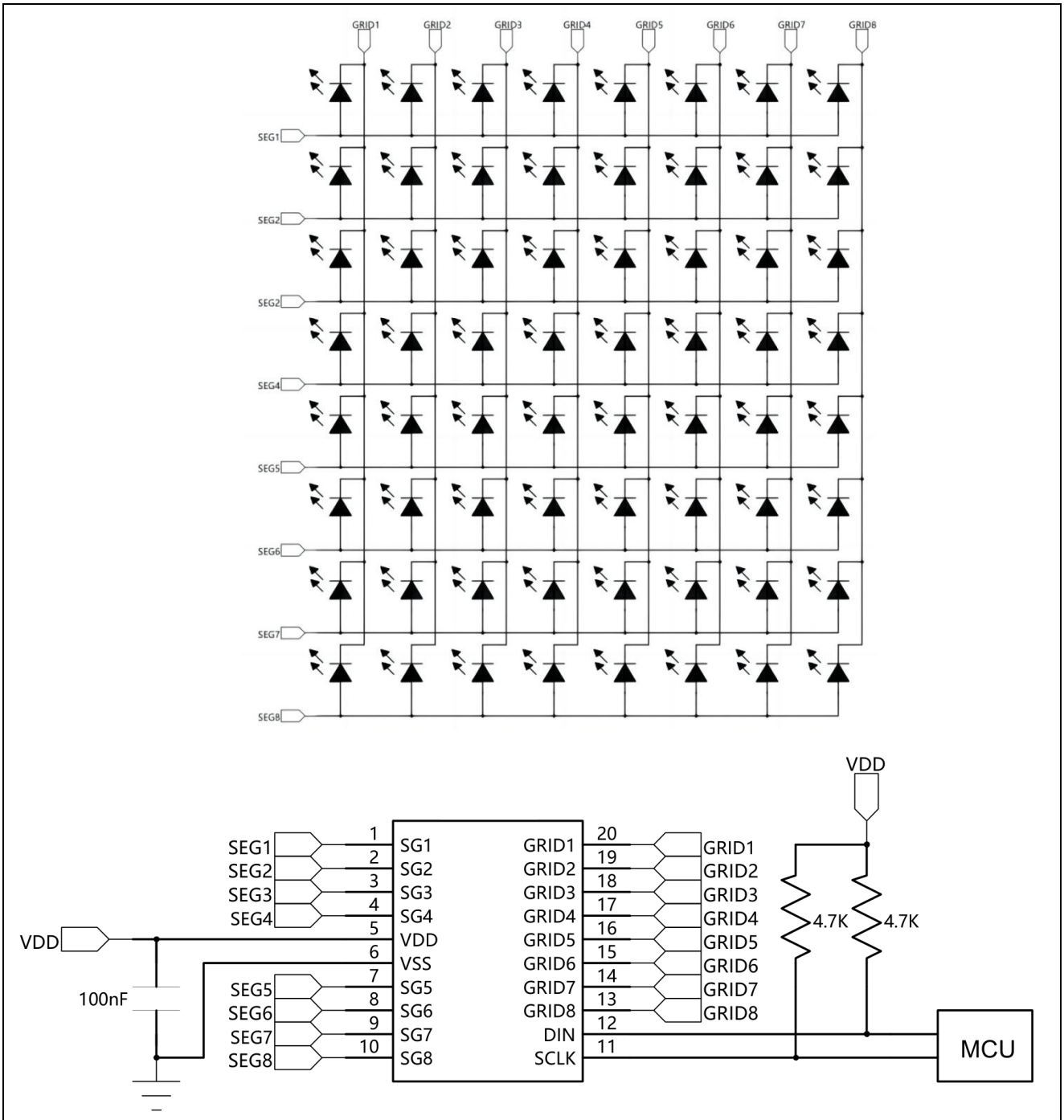


Figure 5. Display Cycle: Scan Line×(Line feed time+256 steps PWM time)

Application circuit



8×8 LED array display application circuit

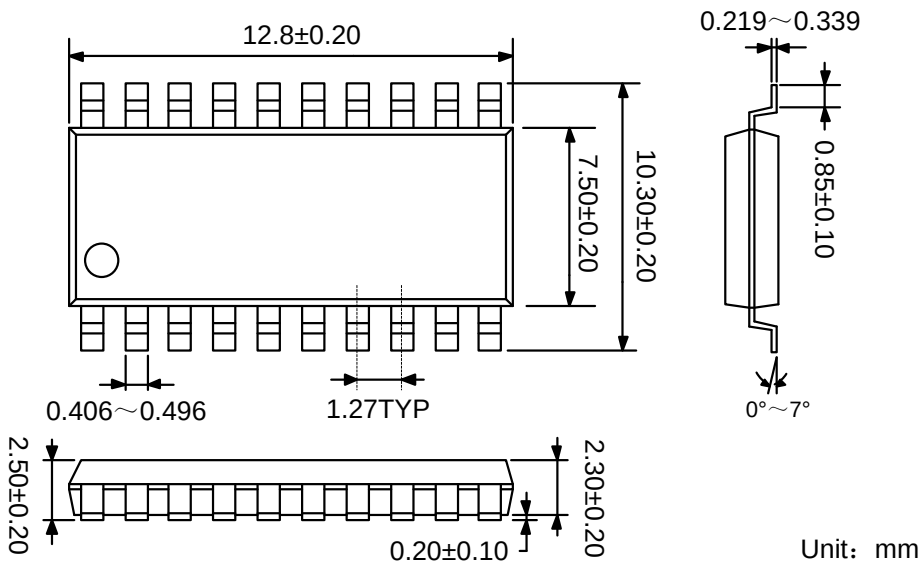
Notes：

1. This application circuit is only for reference.

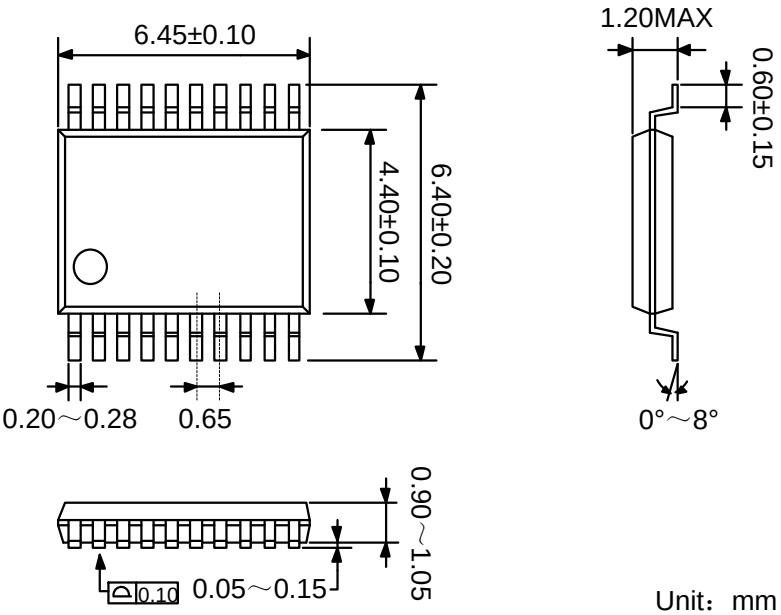
2. DIN and SCLK signals must adopt push-pull output structure.

Package

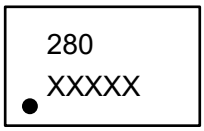
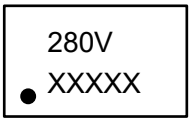
SOP20



TSSOP20



Marking Information

ET62181	ET62181V
	
280 : Part Number XXXXX : Lot Number	280V : Part Number XXXXX : Lot Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2026-03-11	Initial Version	Wu Yu Chen	Li Chen Xuan	Liu Jia Ying