7-Channel LDO PMIC for Camera Applications

General Description

The ET5907SX is CMOS-based low-dropout, low-power linear regulator. It's a 7-channel integrated LDOs for camera applications. Two channels offering max 1200mA with NMOS pass transistor, five channels offering max 400mA with PMOS pass transistor. ET5907SX include 1000kHz high speed I2C interface, the function setting is flexible such as Under voltage lockout (UVLO), power sequence, output voltage, output discharge, current limit per channel. The chip enable control support EN pin control and I2C control.

The ET5907SX is available in 20-bump, 0.35 mm pitch, Wafer-Level Chip-Scale Package (WLCSP).

Features

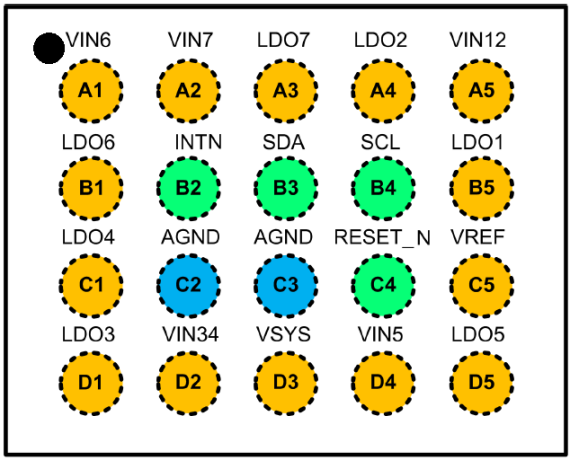
- LDO1 and LDO2
  - VIN12 input voltage range: 1.0V to 2.0V
  - Programmable Output Voltage 0.8V to 1.8V in 6mV steps
  - Max 1200mA Output Current Capability
  - Ultra Low dropout: Typ.100mV at 1000mA, 1.05V Output
- LDO3~LDO7
  - VIN34/VIN5/VIN6/VIN7 input voltage range: 1.9 V to 5.5V
  - Programmable Output Voltage 1.5V to 3.75V in 10mV steps
  - Max 400mA Output Current Capability
  - Less than 20uV(typ) Noise
  - Ultra Low dropout: Typ. 110mV at 400mA, 2.8V Output
- Very Low input quiescent current of Typ. 150μA
- Operation guaranteed with battery voltage down to 2.7V
- Programmable Power Start-Up/Down Sequencing
- Built-in thermal Global Shutdown Protection (OTP)
- Built-in under Voltage Global Shutdown Protection(UVP)
- Built-in over current protection(OCP) and auto-discharging circuit
- Built-in under voltage lockout (UVLO)
- I²C serial control to program output voltage and features
- Package Information:

Part No.	Package	MSL
ET5907SX	WLCSP-20 1.85mm×1.48mm	Level 1

Applications

- Constant-voltage power supply for battery-powered device
- Constant-voltage power supply for smartphones, tablets
- Constant-voltage power supply for cameras, DVRs, STB and camcorders

Pin Configuration

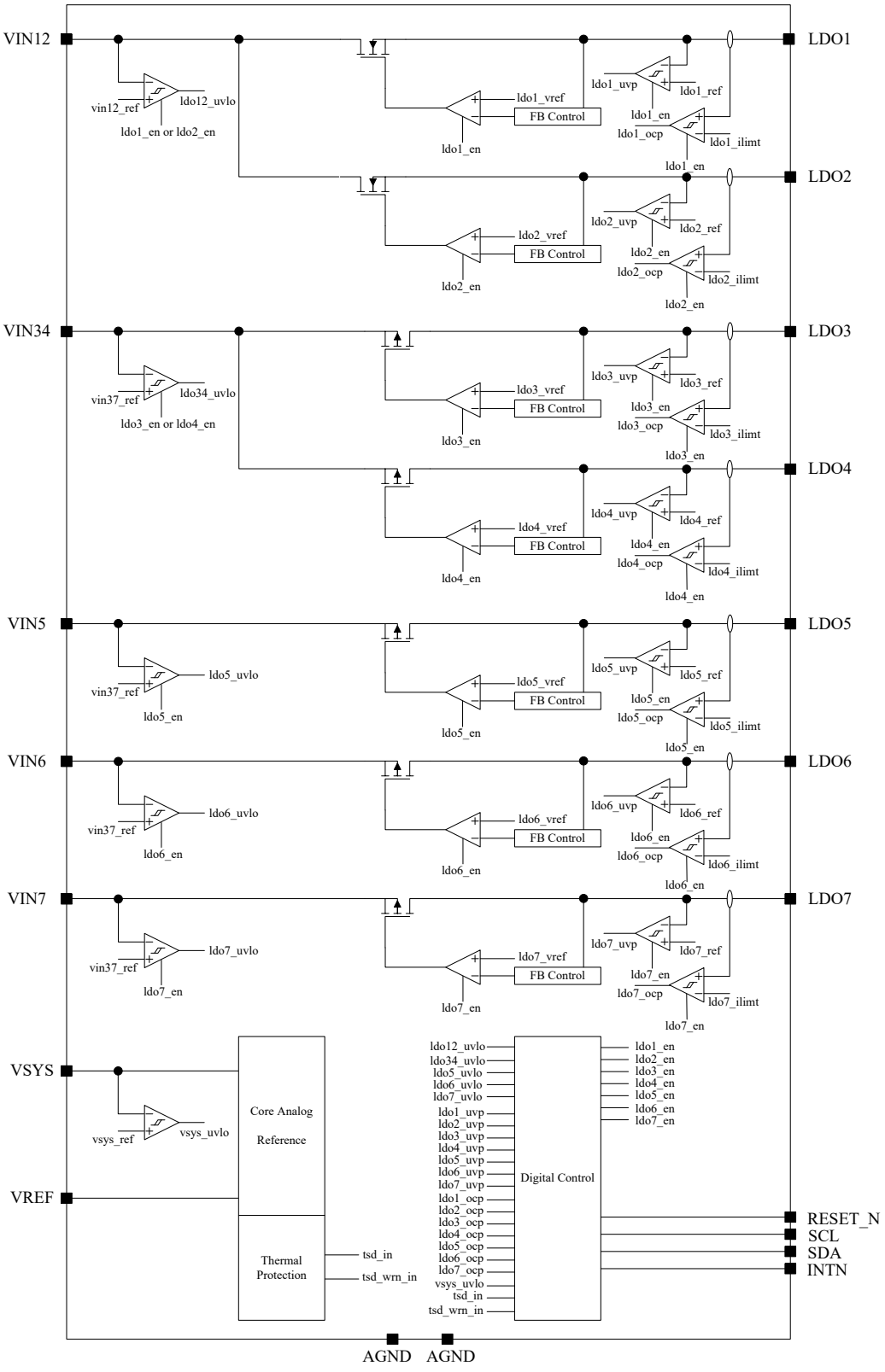


TOP View (Bumps Down) WLCSP-20

Pin Function

Pin No.	Pin Name	Pin Function
A1	VIN6	Input power pin for LDO6.
A2	VIN7	Input power pin for LDO7.
A3	LDO7	LDO7 regulator output
A4	LDO2	LDO2 regulator output
A5	VIN12	Input power pin for LDO1 and LDO2.
B1	LDO6	LDO6 regulator output
B2	INTN	Interface pin for interrupts. Open drain output.
B3	SDA	I2C Data pin. Node should be tied high through a pull up resistor.
B4	SCL	I2C Clock pin. Node should be tied high through a pull up resistor.
B5	LDO1	LDO1 regulator output
C1	LDO4	LDO4 regulator output
C2	AGND	Ground pin.
C3	AGND	Ground pin.
C4	RESET_N	RESET_N pin is used to enable basic circuits necessary for controlling the PMIC. The RESET_N pin has an internal pull-down and should always be connected to a logic high or low.
C5	VREF	Reference bypass pin. If used, connect a 100nF capacitor between this pin and analog ground.
D1	LDO3	LDO3 regulator output
D2	VIN34	Input power pin for LDO3 and LDO4.
D3	VSYS	System power pin. Route trace from system to this pin.
D4	VIN5	Input power pin for LDO5.
D5	LDO5	LDO5 regulator output

Block Diagram



Functional Description

ET5907SX has 7 LDO regulators. LDO1/2 are using NMOS pass transistor for output voltage regulation. The others LDOs are using PMOS pass transistor for output voltage regulation. The ET5907SX LDO1 and LDO2 output voltages can be programmed via I2C from 0.8V to 1.8V in 6mV steps and LDO3-LDO7 can programmed from 1.5V to 3.75V in 10mV steps using the associated I2C registers. The voltage transition going from a lower to a higher voltage is a single step with transition time dependent on output current and output capacitance. The output current drives the voltage slew rate from higher to lower voltage transitions.

The device is in reset when the RESET_N is low and will power up the device's main control circuits when RESET_N is pulled high.

If LDOx_EN bits are set to 1 prior to RESET_N being asserted high, the LDOs will power up a short time after RESET_N is pulled high. When the RESET_N pin is pulled low, any interrupt bits in registers 0x15 to 0x17 will be cleared along with the status bits in 0x18 to 0x21. Additionally, all fault counters will reset to 0.

Enable of each LDO can be accomplished using I2C register LDOx_EN bit in register 0x03 or the LDOs can be powered up/down sequentially using the Sequence State Machine, settable using the register bits in registers 0x0B to 0x0F. The device is also designed to support multiple start-up or shut-down sequences for multiple module loads.

The current limit and deglitch timer of each LDO can be programmed to optimize the LDO performance for the application. The device monitors each power input pin and each LDO output. If any of these below a threshold a status and interrupt bit are set.

RESET_N PIN and ENABLE BITS

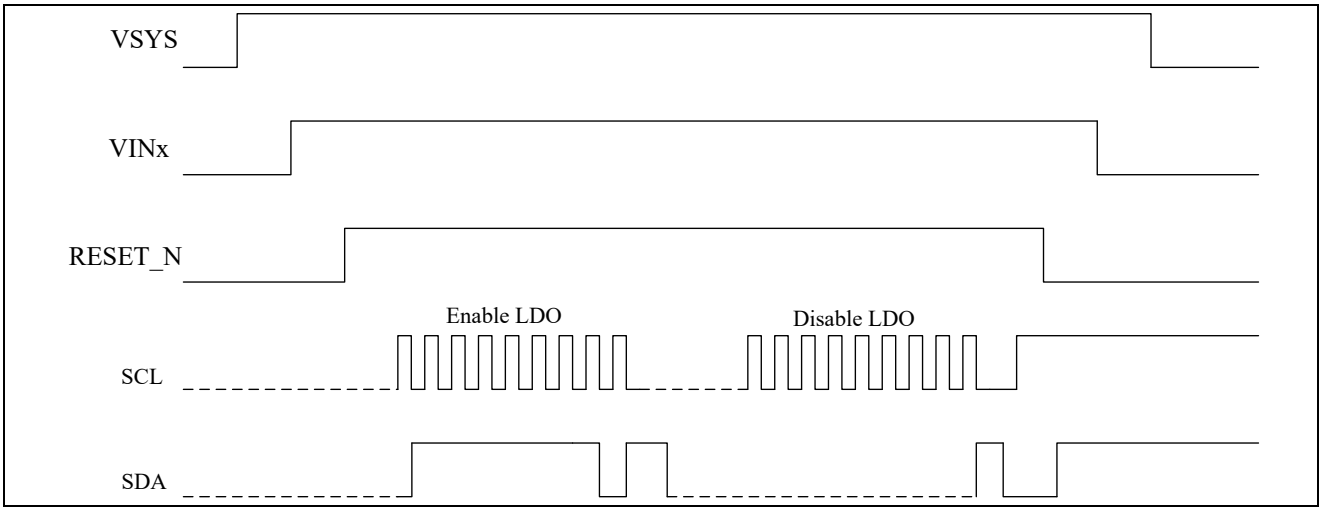
The tables below provide the states of the LDOs based on the combination of the enable pins and register bits.

RESET_N	LDOX_SEQ	LDOX_EN	SEQ_CONTROL Dependent	On/Off
Low	000	0	No	Off
High	000	0	No	Off
Low	>000	0	No	Off
High	>000	0	Yes	CNTL
Low	000	1	No	Off
High	000	1	No	ON
Low	>000	1	No	Off
High	>000	1	Yes	CNTL

Note: CNTL indicates that the state of the output will be dependent on the setting of the seq_ctrl[1:0] bits. When RESET_N is high, seq_ctrl[1:0]=2'b01 will enable any outputs based on their LDOX_SEQ>000.

Power up/down sequence control

The recommended power on sequence of ET5907SX is to power on VSYS first, then power on input power VINx, then set RESET_N to high level, and then enable LDOx. The corresponding power off sequence is to turn off LDOx first, then set RESET_N to low level, then power off input power VINx, and finally power off VSYS.



The ET5907SX LDO's can be enabled two ways using the I2C register bits if RESET_N is high.

1. Setting LDOX_SEQ=000 in 0x0B(LDO12_SEQ) or 0x0C(LDO34_SEQ) or 0x0D(LDO56_SEQ) or 0x0E(LDO7_SEQ) and the LDOX_EN assigned to the LDO in register 0x03, ENABLE to 1.

2. Setting LDOX_SEQ>000 in registers 0x0B/C/D/E and then set seq_ctrl[1:0]=2'b01 in the 0x0F, SEQ_CTR register.

ET5907SX LDOs have internal soft-start which limits the battery current to the setting LDOX_ILIM in register 0x02. If an LDO output fails to reach 90% of the programmed voltage at start-up, a UVP fault is declared. See the output UVP section for description of LDO.

Power-up and shut down of each regulator can be controlled by an I2C register. It can be set at the registers ldox_seq[2:0] (x=1 to 7) respectively. ldox_en is an internal signal to enable one of regulators, if ldox_seq[2:0] set to '000', that LDOX channel can be controlled directly by a bit specified in register LDO_EN. LDOX_VSET[7:0] can set output voltage of each channel.

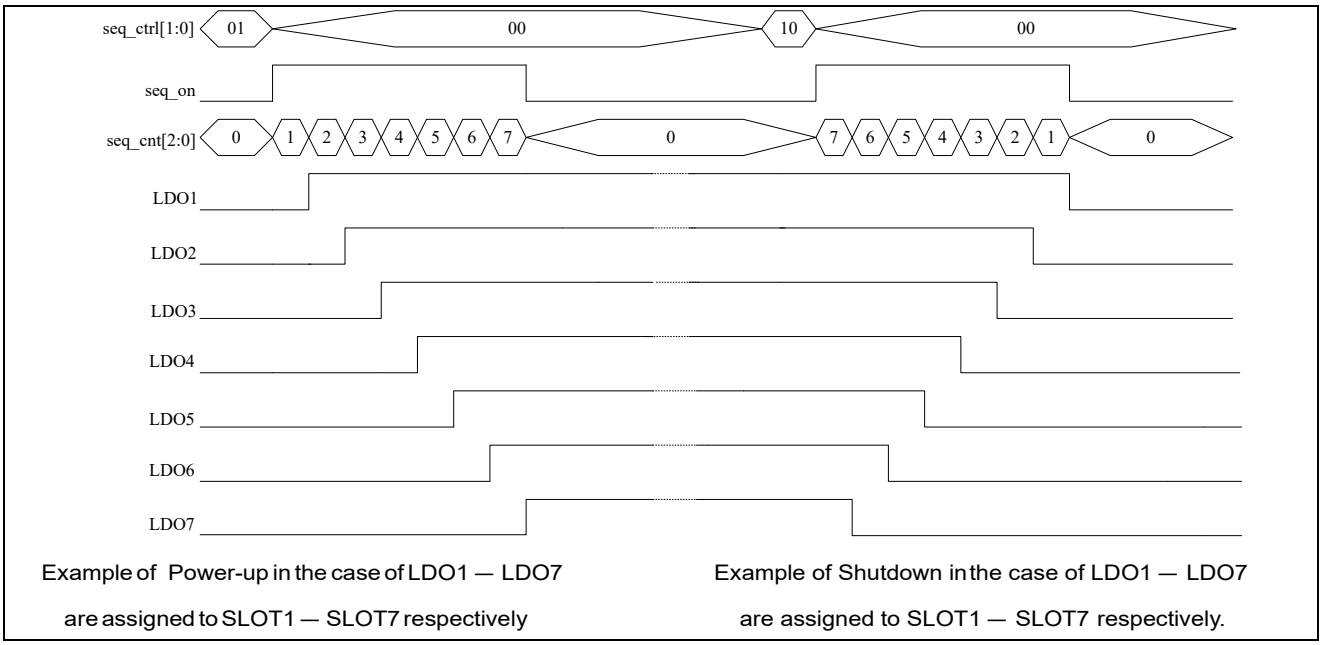
3. Automatic power up/down sequence control.

ET5907SX has seven SLOTs to which each regulator can be assigned.

They are started by seq_ctrl[1:0] signal. when seq_ctrl[1:0] is set '01'. Internal counter seq_cnt[2:0] starts increments from 0 ("000") to 7 ("111"). When seq_ctrl[1:0] is set '10', seq_cnt[2:0] decrements from 7 ("111") to 0 ("000"). Regulators assigned to one of SLOTs starts power-up or power-down.

The seq_cnt[2:0] matches the SLOT number, when seq_cnt[2:0]=000, it indicates that sequencing has completed or not started.

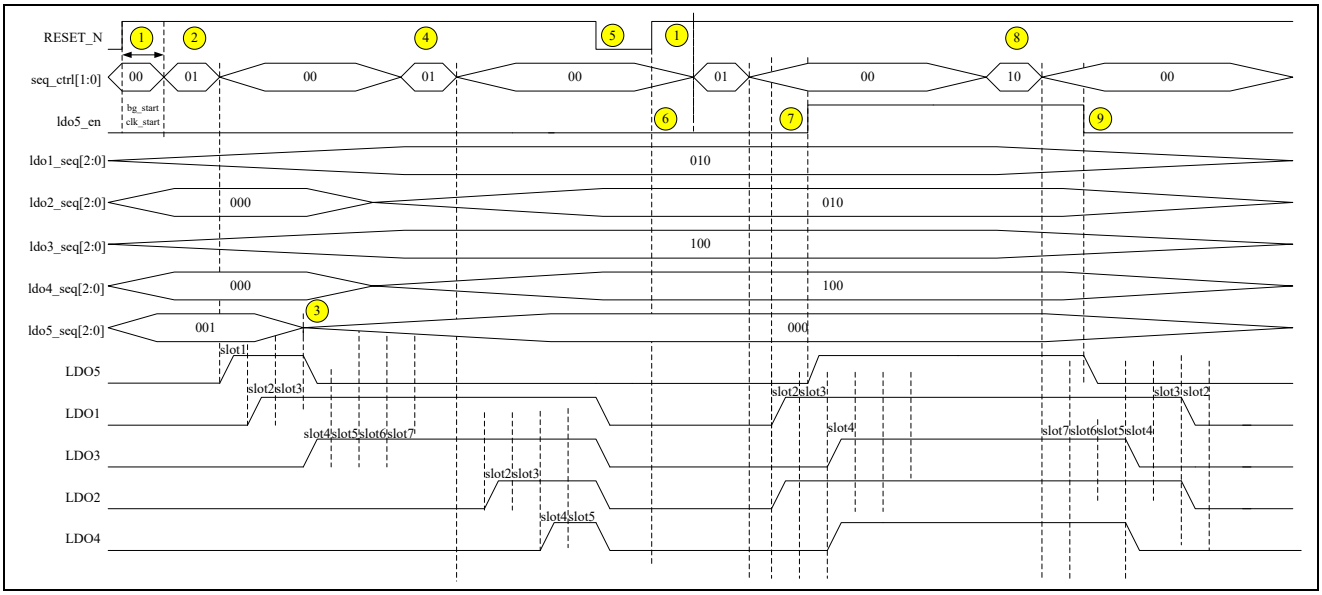
Internal logic signal seq_on=1 indicates that sequencing is executing and somewhere between the start of slot 1 and the end of slot 7, seq_on=0, it indicates that has completed or not started.



Example of Power-up in the case of LDO1 — LDO7 are assigned to SLOT1 — SLOT7 respectively

Example of Shutdown in the case of LDO1 — LDO7 are assigned to SLOT1 — SLOT7 respectively.

Sequence Timing and Control



State Description:

1. RESET_N is asserted high and the band gap and internal clock are started. A minimum time of 100us needs to be allowed between RESET_N being asserted high and seq_ctrl[1:0] changed to 01 in order for the device to transition from shutdown to Sleep mode where the Bandgap and digital circuitry are enabled.

2. Upon seq_ctrl[1:0] being set to 01, LDO5 is started in slot 1 (ldo5_seq[2:0]=001). seq_ctrl[1:0] bits are cleared immediately after the sequence is initiated. LDO1 and LDO3 are started in the associated slot given to their ldox_seq value.

3. The ldo5_seq[2:0] is set to 000, disabling the LDO.

4. ldo2_seq[2:0] and ldo4_seq[2:0] are set and a new sequence is started when seq_ctrl[1:0] is set to 01 again. The state of any other LDO is not changed.

5. RESET_N is pulled low and all LDOs are disabled.

6. RESET_N is pulled high enabling the IC.

7. ldo5_en is set to 1 and LDO5 is enable.

8. seq_ctrl[1:0] is set to 10, starting a shutdown sequence

9. Asynchronous to the shutdown sequence LDO5 is disabled when ldo5_en=0.

If an LDO faults during a start-up sequence, the other LDOs will still be started in their assigned time slot. The ldox_seq[2:0] bits for the faulted LDO will remain set to the assigned slot. The system can then attempt to start the faulted LDO in another sequence by setting the seq_ctrl[1:0] bits to 01 or by clearing the ldox_seq[2:0] bits to 000 and then writing a "1" to the ldox_en Enable bit.

Shutdown

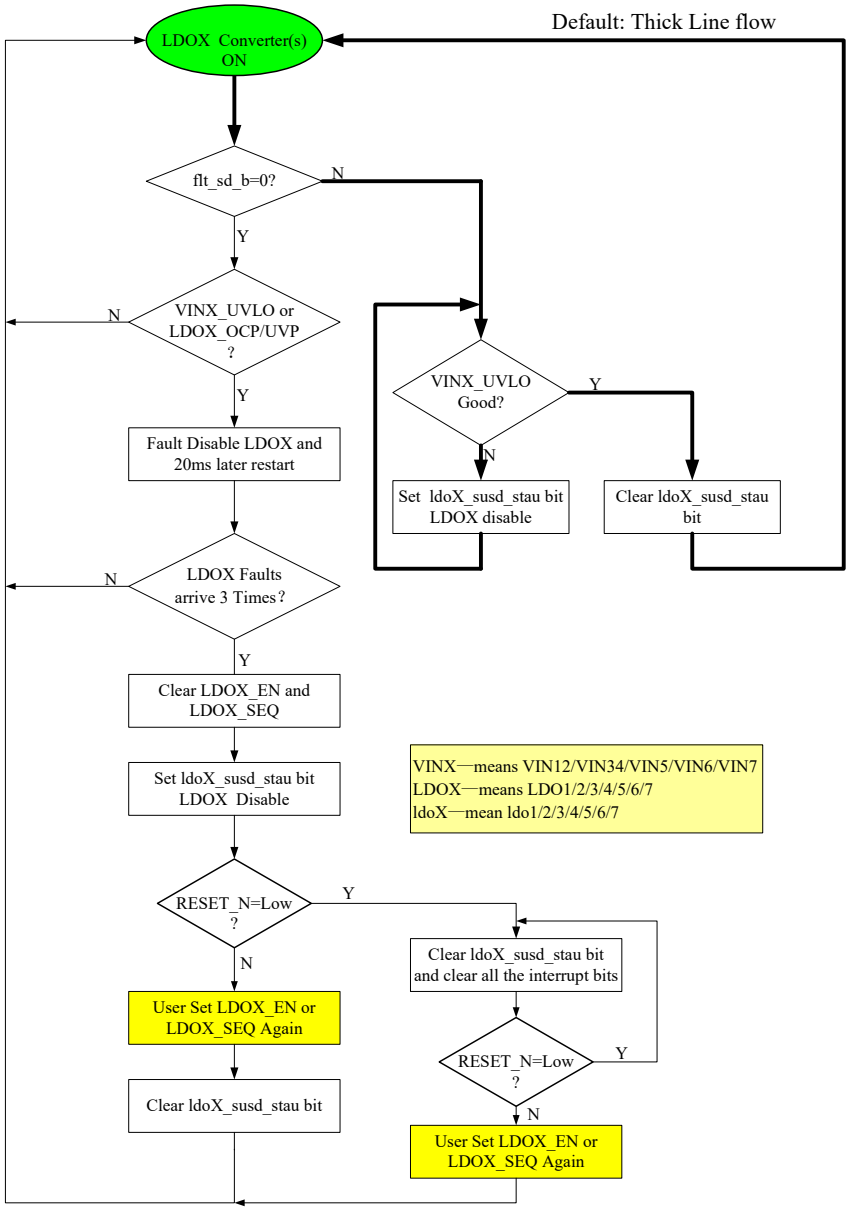
To disable the ET5907SX LDO(s), set the I2C register bit, ldox_en assigned to the LDO in register 0x03 to 0 or if register, 0x0F, SEQ_CTR bits [5:4], seq_ctrl[1:0] is set to "10" and ldox_seq[2:0]>000, the LDO(s) will be disabled in the Reserved order of time slot they are assigned. To do a global shutdown of all LDOs set the RESET_N pin low.

Multiple Fault Shutdown

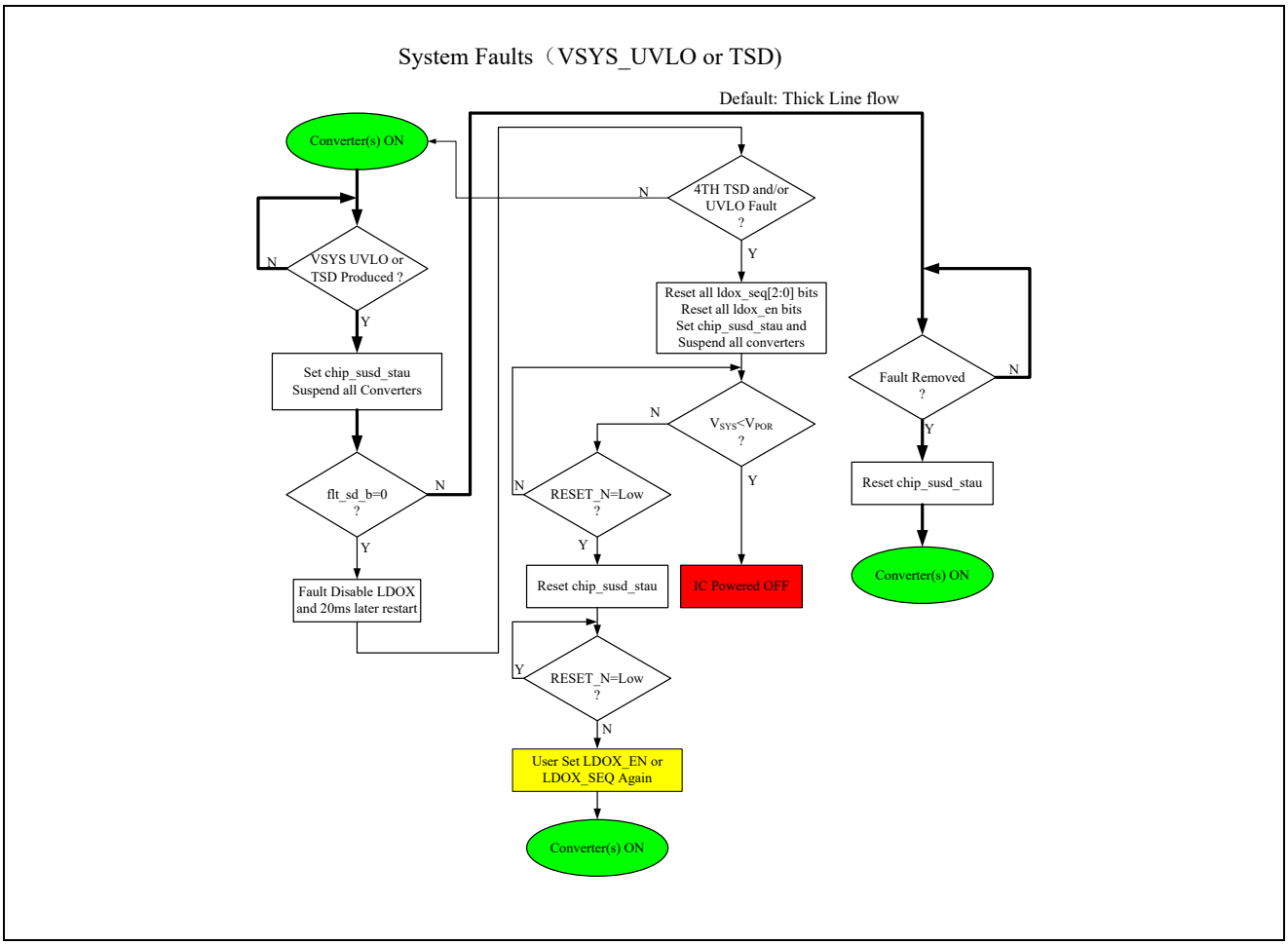
To prevent repetitive starting and faulting of an LDO, detection of 3 failures will result in a complete shutdown of the LDO. If for instance LDO1 where to have a qualifying UVP condition and the LDO was disabled, LDO1 will be restarted 20ms later. If LDO1 where disable three times due to any faults (UVP, OCP or Short Circuit), LDO1 would be permanently shutdown until it is re-enabled by I2C commands. When LDO1 is shutdown under such a condition, the LDO1_EN bit is set to 0 and the ldo1_seq[2:0] is set to 000. This shutdown behavior applies to all of the ET5907SX LDOs.

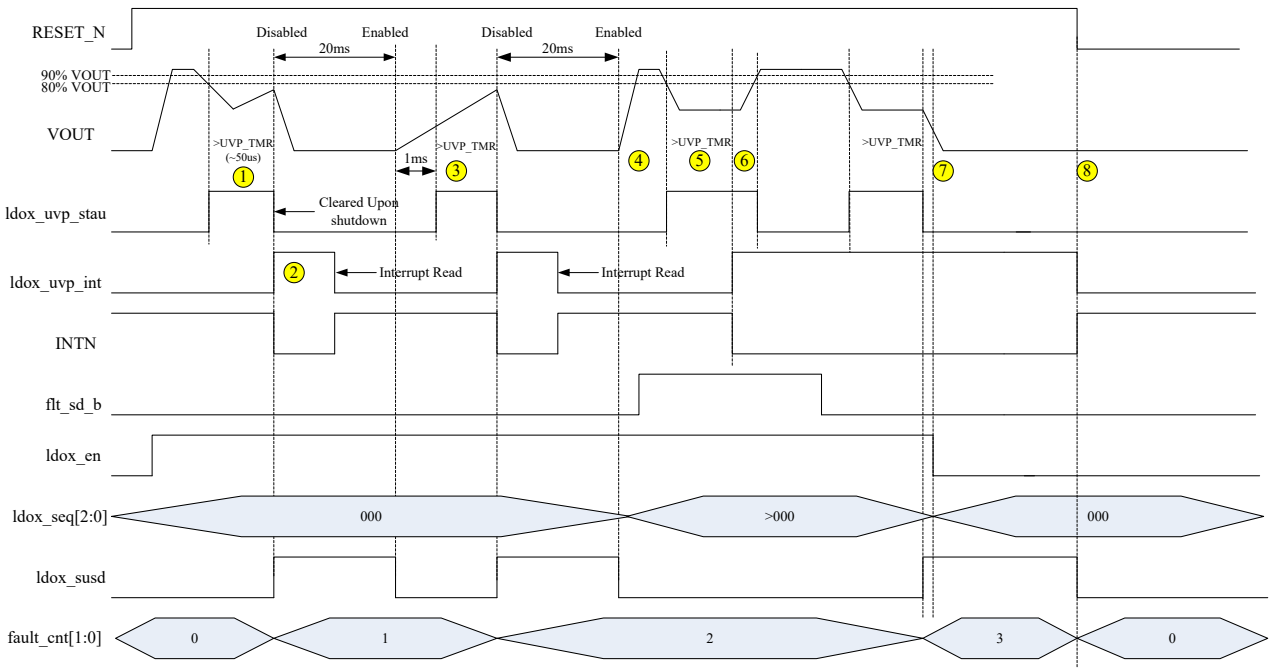
If UVP, OCP occurs when flt_sd_b is set to 1, the LDO(s) is not disabled and the fault counter is not incremented, but the interrupt and status bits indicate the fault occurred. flt_sd_b=1 doesn't prevent shutdown of LDOs when VIN12, VIN34, VIN5, VIN6 or VIN7 are in a UVLO condition, but the fault counter is not incremented.

LDO FAULTS(VINX_UVLO or LDOX_OCP or LDOX_UVP)



When flt_sd_b=0, if there are any combination of four VSYS_UVLO and/or Thermal Shutdown faults(shutdown and after 20ms restart again for 4 times), the device will permanently shutdown and the chip_susd_stau bit will be set until RESET_N has been set low and is asserted high again; When flt_sd_b=1, if there is VSYS_UVLO or Thermal Shutdown faults, the device will shutdown and restart until the faults are released.


System Faults（VSYS_UVLO or TSD)
Default: Thick Line flow
Converter(s) ON
VSYS UVLO or TSD Produced ?
Set chip_susd_stau Suspend all Converters
flt_sd_b=0 ?
Fault Disable LDOX and 20ms later restart
4TH TSD and/or UVLO Fault ?
Reset all ldox_seq[2:0] bits Reset all ldox_en bits Set chip_susd_stau and Suspend all converters
VSYS<VPOR ?
RESET_N=Low ?
Reset chip_susd_stau
IC Powered OFF
RESET_N=Low ?
User Set LDOX_EN or LDOX_SEQ Again
Converter(s) ON
Fault Removed ?
Reset chip_susd_stau
Converter(s) ON
N
Y


RESET_N
Disabled
Enabled
20ms
90% VOUT
80% VOUT
VOUT
>UVP_TMR (~50us)
1ms
ldox_uvp_stau
Cleared Upon shutdown
ldox_uvp_int
Interrupt Read
INTN
flt_sd_b
ldox_en
ldox_seq[2:0]
000
>000
ldox_susd
fault_cnt[1:0]
0
1
2
3

State Description:

1. A timer starts at the beginning of a UVP event and the UVP condition remains for the timer length(>50us), the converter is disabled for the first time.

2. The converter ldox_uvp_stau is set and 50us later the ldo_uvp_int bit is set and the INTN pin is pulled down. The converter is disabled and the ldo_uvp_stau bit is blanked, the ldox_susd bit is set while the conveter is suspended until the next start. The fault_cnt[1:0] is incremented upon shutdown.

3. The converter fails to reach UVP_Rising(90% Vtarget) within 1ms of restart-up. Since the flt_sd_b=0, a second UVP failure is counted.

4. At the restart, the interrupt bit remains a 1until read. The ldox_susd bit is reset by the restart action. The converter successfully reaches a voltage above UVP_Rising within 1ms and runs. Meanwhile the flt_sd_b and ldox_seq[2:0] are set to 1 and >000 respectively.

5. With flt_sd_b set to 1 when the fault occurs, the converter remains on, but the interrupt bit is set to one and INTN pin is pulled down. The ldox_susd bit remains a “0” since the converter remains enabled.

6. The ldo_uvp_stau is set when the fault occurs, but clears when the converter is >90% of the target voltage.

7. When the converter is shutdown for the third time, the ldox_en is set to 0; ldox_seq is set to 000; The ldox_uvp_stau bit is set to 0. The fault_cnt[1:0] keep three and ldox_susd keep high level.

8. When RESET_N is set low, the fault_cnt[1:0] is cleared to 0 and ldox_susd is cleared to 0. At the same time, ldox_uvp_int is cleared to 0. Another way to clear fault_cnt[1:0] and ldox_susd bits is reset the ldox_en or ldox_seq bit, and LDOx will restart again.

UVLO Rising

All LDOs use VSYS to power their analog and control circuitry. For proper operation the VSYS input is monitored for under voltage conditions. LDO1 and LDO2 use VIN12, LDO3 and LDO4 use VIN34, LDO5 uses VIN5, LDO6 uses VIN6 and LDO7 uses VIN7 to power their outputs.

If VSYS is greater than the POR threshold (~2.0V), but did not reach VSYS_UVLO_RISE when RESET_EN is high, a UVLO interrupt vsys_uvlo_int bit and the status bit sys_uvlo_stau are set and the INTN pin is asserted low. When the LDO(s) are commanded to start or are running when VSYS falls below the UVLO threshold, but above VPOR, a re-start of the LDO(s) will be attempted again for the longer of 20ms (flt_sd_b=0) or when the VSYS rises above the VSYS_UVLO_RISE threshold. While in this state, the chip_susd_stau bit is set. The status bit remains set to "1" only while VSYS>VSYS_UVLO_RISE. The Interrupt bit will be cleared when read.

LDO1 and LDO2 may temporarily start if one or both VIN12 and VSYS have not reached VIN12_UVLO THRESHOLD RISING or VSYS_UVLO_RISE level respectively prior to the LDO being enabled. If VSYS is good, but VIN12 is not when LDO1 and/or LDO2 are enabled, the interrupt bit ldo12_uvlo_int and status bit, ldo12_uvlo_stau are set and the INTN pin will be pulled low. Additionally, ldo1_susd and/or ldo2_susd will be set to "1" the longer of 20ms(flt_sd_b=0) or until VIN12 is greater than VVIN12_UVLO_RISE. At which time the SUSD bits will be cleared and the LDO(s) started. The ldo12_uvlo_stau, status bit remains set as long as VIN12 < VIN_UVLO_RISE. Similarly UVLO for VSYS, the LDO will not be restarted for a minimum of 20ms

and until VIN12 is greater than VIN12_UVLO_RISE. When the set output is low and the input voltage is less than 1.0V, the state of VIN12_UVLO should be ignored.

UVLO for LDO3 and LDO4 are identical to that described above for LDO1 and LDO2. The UVLO threshold for LDO3 and LDO4 are VVIN34_UVLO_RISE. Behavior for LDO5, LDO6 and LDO7 are similar relative to VIN5, VIN6 and VIN7 as that discussed for LDO1.

Notes:

- Status bits may not be reliable until VSYS has reached a level of ~2.0V (VPORmax).

- The power on speed of VSYS should be faster than 2.5v/ms, otherwise it will be interrupted due to UVLO.

UVLO Falling

If VSYS falls below its VSYS_UVLO_FALL, falling threshold while one or more of the LDOs are enabled, a UVLO interrupt in 0x17, vsys_uvlo_int is set and the INTN pin is pulled low. A status bit in register 0x1A, vsys_uvlo_stau is also set while the rail remains below the rising UVLO threshold. Likewise, if VIN12, VIN34, VIN5, VIN6 or VIN7 fall below their falling threshold while the respective LDO is enabled, the associated input TSD_UVLO_STAU register bits will be momentarily set, the bits in TSD_UVLO_INT will be set and the INTN pin is pulled low. Then the LDOs will be disabled, the status bit reset and the associated ldox_susd bit in 0x1B, SUSD_STAU set to indicate the supply has been suspended.

PMIC Operation in VSYS UVLO

VSYS State	RESET_N	Results
VSYS < VPOR	Low	Device in shutdown, I2C registers not reliable
VPOR<VSYS<UVLO	Low	Band Gap off, I2C registers readable
VSYS > UVLO	Low	Upon POR initialization, all registers set to their default values. If programmed prior to system fault, registers retain value and begin a start up after RESET_N is high
VSYS < VPOR	High	Device in shutdown, I2C registers not reliable
VPOR < VSYS <UVLO	High	Band Gap on, I2C registers readable
VSYS > UVLO	High	Registers retain value prior to system fault and do an automatic restart upon RESET_N going high.

When an over-temperature or a VSYS UVLO event occurs, all ET5907SX LDOs are disabled for a minimum of 20ms(flt_sd_b=0). For UVLO on the LDO inputs, the individual LDO's will be disabled for a minimum of 20ms(flt_sd_b=0) and until the voltage rises above UVLO_VSYS_RISE.

Current Limit Protection

For each channel, when output current of LDO output pin is higher than current limit threshold or the output pin is direct short to GND, the current limit protection will be triggered and clamp the output current at a predesigned level to prevent over-current and thermal damage. Set related bits to select Current limit threshold register.

The LDO output current is short-circuit protected and the short-circuit current level can be programmed using the settings in register 0x02, LDO_ILIMT. When a short occurs(VLDO1/2<30%VSET, VLDO3~7<0.5V) on the

LDOx output, the current is automatically limited to the programmed current limit and Vout may drop, depending on the difference between the input and target output voltage. The resultant VOUT is the product of current limit setting in register 0x02 LDO_ILIMT and the load impedance. When current limit is detected, the associated OCP status bit in 0x19, OCP_STAU is set to "1", If the LDOx remains in current limit for 1ms(default value), an interrupt bit in register 0x16, OCP_INT is generated and the INTN pin is pulled low. Then the LDOx is disabled, the status bit in 0x16 OCP_STAU register is reset to 0 and the associated suspend bit in the 0x1B SUSD_STAU register is set to "1".

The LDOx will attempt a restart 20ms later(flt_sd_b=0) and the associated suspend will be reset to "0". If the associated interrupt bit was not read while the output was suspended, the interrupt will remain a 1 after restart and INTN (if not masked) will remain low.

Note: The OCP deglitch timer can be programmed to one of four periods by setting Reg. 0x11, bits [2:1].

Inrush Current Limit

After enable the LDOs, the inrush current limit circuit is in operation, LDO1~2 inrush time is approximately 2ms, and LDO3~7 inrush time is approximately 700us. Therefore, the load current should be drawn after the output voltage reached the preset value.

If the load current is drawn during the start-up, it should be within the following values:

Register 0x02 is set to 0x7F:

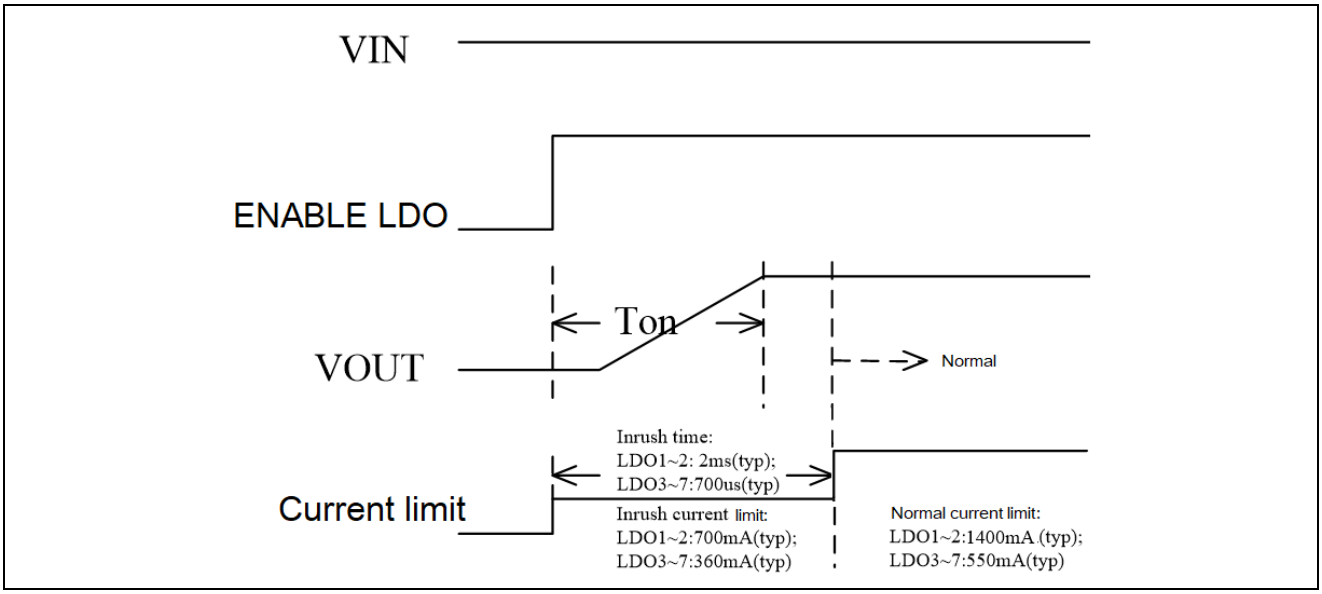
Iout1~2≤700mA on ldo1~2 (Typ);

Iout3~7≤360mA on ldo3~7(Typ).

Register 0x02 is set to 0x00:

Iout1~2≤600mA on ldo1~2 (Typ);

Iout3~7≤275mA on ldo3~7(Typ).



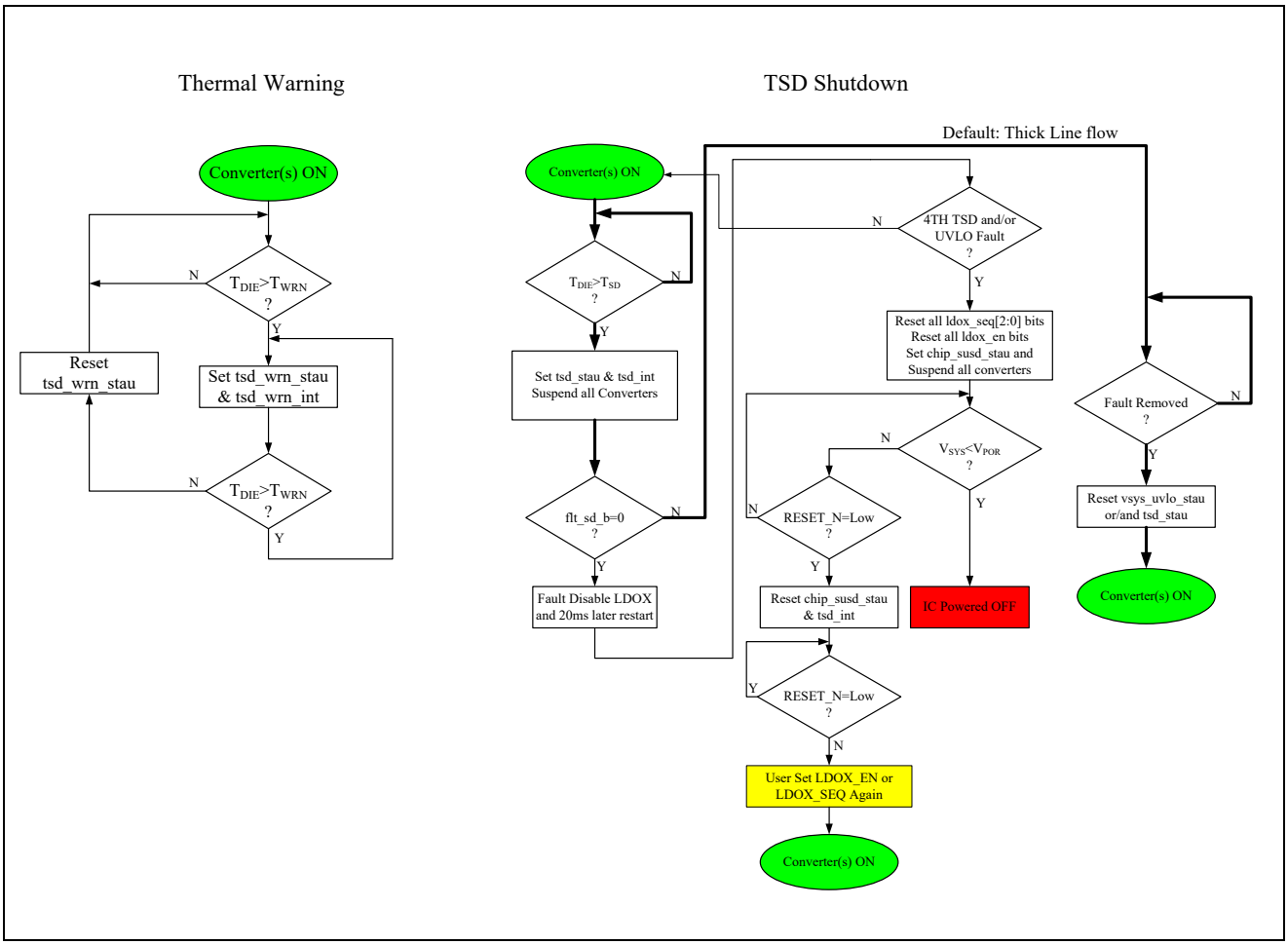
Thermal Shutdown Protection

When the die temperature rises to a nominal 125°C, a Thermal Warning interrupt occurs setting the tsd_wrn_int bit to "1" and INTN pin is pulled low. The tsd_wrn_stau register bit will be set to "1" and remain set until the die temperature drops to a nominal value of 100°C.

If the die temperature continues to rise above the thermal warning level, a Thermal Shutdown event is activated at a nominally 145°C. When the Thermal Shutdown level is reached, all power outputs are disabled without shutdown sequencing, but I2C communications remain. The device remains in thermal shutdown until the die temperature falls to approximately +120°C.

At the time a Thermal Shutdown detection occurs, the tsd_int, interrupt bit is set and the INTN pin is pulled low to notify the system of the event. The tsd_stau, register bit is also set and will remain set as long as the device is above TWRN°C. The C_SUSD bit is set while the device is shutdown due to the overtemp condition.

After the die temperature has fallen below the TWRN threshold following a Thermal Shutdown event, the state of the I2C control registers will remain as they were prior to shutdown, the tsd_wrn_stau and tsd_stau bits will clear and the device will return to the operating conditions prior to the thermal shutdown event.



Output UVP (Under Voltage Protection)

If the LDO is enable and the output voltage falls approximately 20%(10% for LDO1/2) below the programmed voltage, the associated UVP Status bit in register 0x18, UVP_STAU will be set to "1". If the fault persists for more than 50us the UVP Interrupt bit in register 0x15, UVP_INT will be set to "1" and the INTN pin will be pulled low. The LDO will then be disabled, the associated Status bit set back to "0" and Suspend bit in 0x1B, SUSD_STAU set to a "1". The interrupt bit will be cleared upon a read of the bit.

The LDO will be restarted 20ms (providing it is not the third fault) after it was shutdown by a UVP event and the suspend bit in SUSD_STAU reset to "0". If the associated UVP interrupt bit is not read while the output was suspended, the interrupt (if not masked) will remain a "1" after restart and INTN will remain low.

In order to make the UVP of LDO 3 ~ 7 work normally, the input voltage of LDO should be greater than the output voltage, and the voltage of VSYS should be greater than the output voltage of LDO.

Note: For LDOx, if VSYS<VOUTx+1.1V(x=1~7), the output UVP interrupt output function for LDOx can not be used. And the corresponding mask UVP interrupt bit in LDOx_MASK(0x1C) register should be set to 1(mask LDOx UVP interrupt output function) through I2C before enable LDOx.

Recommended: Set LDOx_MASK(0x1C) to 0x7F before enable LDOx through I2C to disable all LDO UVP interrupt output function.

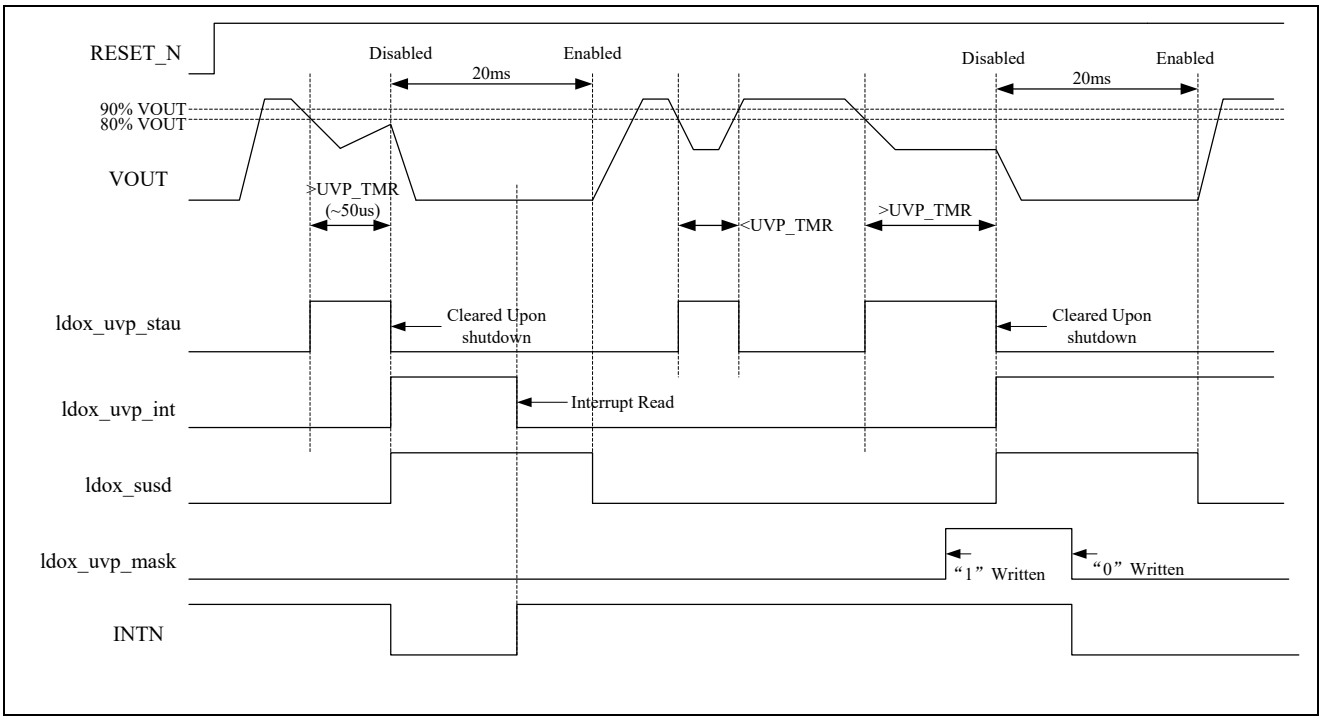
UVP Timing

The timing diagram below represents the general way each LDO's under-voltage circuitry behave. The names shown in the diagram are general descriptions.

In the first UVP detection case, the ldox_uvp_stau bit is set when the fault is detected and after a 50us wait period, the ldox_uvp_int bit is set and the INTN pin is pulled low. The LDO output is disabled, the Status bit is reset and then the associated ldox_susd bit in SUSD_STAU register is set. After 20ms(flt_sd_b=0) the LDO is restarted and the SUSD_STAU bit is cleared. Shown in the graph is a read of the interrupt bit register before the 20ms expires. This clears the interrupt bit and the INTN pin is released and rises high.

In the second case, the output is not in the UVP condition for the qualifying time (UVP_TMR) and ldox_uvp_stau bit returns to 0.

For the third case, the output falls for longer than UVP_TMR and the interrupt bit is set, the LDO is disabled, the Status bit reset and the ldox_susd, suspend bit is set. Since the interrupt is masked by ldox_uvp_mask, the INTN pin is not pulled low until the Mask bit is set back to "0". When the LDO is re-enabled after 20ms(flt_sd_b=0), the ldox_uvp_int remains a "1" as the register bit was not read.



Auto Discharging

For each channel, when shut down the output, the Auto-Discharging circuit will be turned on to discharge the electric charge on output capacitor, and decrease the voltage of output pin in very short time. The Auto-Discharging function is optional. Set related bits to select output discharge function for Discharge Resistor (LDO_DIS Register), "1": Enable. "0": Disable.

Input and output Capacitor

The LDO1/2 are designed to be stable for ceramic output capacitors with Effective capacitance in the range from 4.7μF to 47 μF. The LDO3~LDO7 are designed to be stable for ceramic output capacitors with Effective capacitance in the range from 0.68 μF to 10 μF.

The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range. In applications where no low input supplies impedance available, the recommended C_{VSYS}, C_{VIN34}, C_{VIN5}, C_{VIN6}, C_{VIN7}, Capacitance ≥1uF and C_{VIN12}=≥4.7uF.

Serial Port Interface (I2C)

- **Bus Interface**

Baseband Processor can transmit data with ET5907SX each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected.

- **Data Validity**

When the SCL signal is HIGH, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

- **Start (Re-start) and Stop Working Conditions**

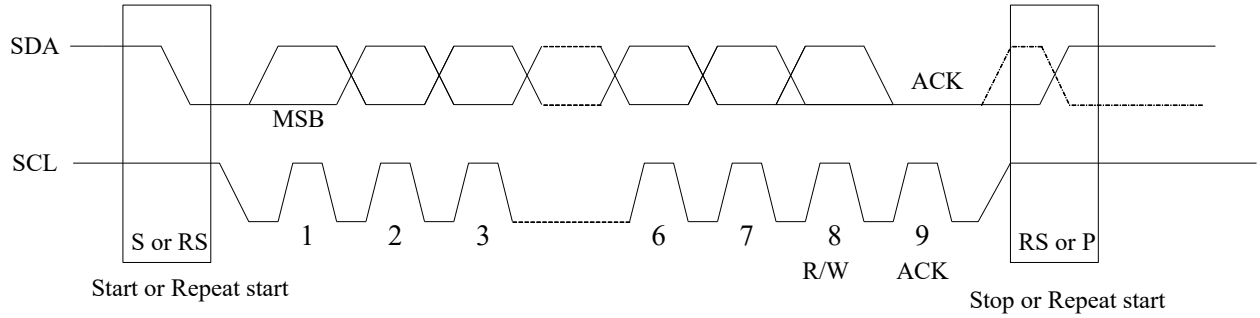
When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

- **Byte format**

Each byte of data line contains 8 bits, which contains an acknowledge bit. The first data is transmitted MSB.

- **Acknowledge**

During the writing mode, ET5907SX will send a low level response signal with one period width to the SDA port. During the reading mode, ET5907SX will not send response signal and the host will send a high response signal one period width to the SDA.



I2C write mode

Note:

ACK=Acknowledge

MSB=Most Significant Bit

S=Start Conditions RS=Restart Conditions P=Stop Conditions

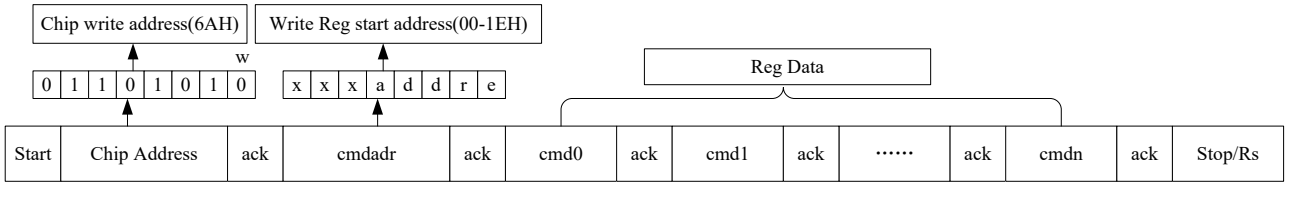
Fastest Transmission Speed =1000KBITS/S

Restart: SDA-level turnover as expressed by the dashed line waveform

- **I2C Slave Address**

The default 7bit I2C slave address is 0110101b(0x35), and 8bit address for the writing register mode is 01101010b(0x6A), the reading register mode is 01101011b(0x6B). The I2C address can also be changed by setting the 2 bits in register 0x12, i2c_adr_sel[1:0] register bits reflects the default options available for request. The Address register will be cleared back to default setting anytime a power-on-reset POR or when a software reset is implemented in the SOFT_RESET register.

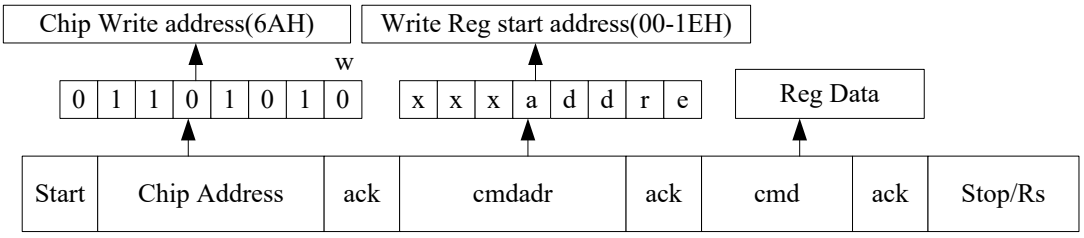
- **I2C Writing Command Register Interface Protocol (continuous)：**



I2C Writing Command Register(continuous)

- Start=Start Conditions
- Chip address=Write register address =0110101+0(w)b
- ack=Acknowledge from ET5907SX
- Write Reg start address byte = cmdadr(xxx + REG's 5bit addre)
- ack=Acknowledge from ET5907SX
- Reg data 0 = cmd0(Command data0)
- ack=Acknowledge from ET5907SX
- ……
- Reg data n =cmdn(Command datan)
- ack=Acknowledge from ET5907SX
- Stop/Rs=Stop Condition/Restart Condition

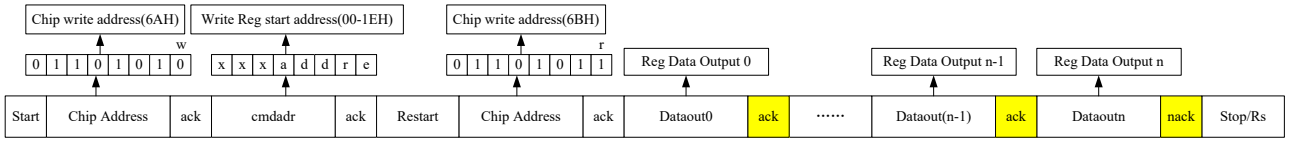
- **I2C Writing Command Register Interface Protocol (single)：**



I2C Writing Command Register(single)

- Start=Start Conditions
- Chip address =Write register address=0110101+0(w)b
- ack=Acknowledge from ET5907SX
- Write Reg start address byte = cmdadr(xxx + REG's 5bit addre)
- ack=Acknowledge from ET5907SX
- Reg data= cmd(Command data)
- ack=Acknowledge from ET5907SX
- Stop/Rs=Stop Condition/Restart Condition

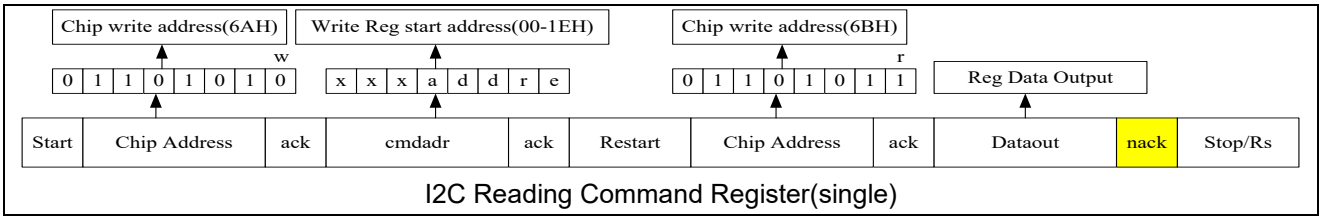
- **I2C Reading Command Register Interface Protocol(continuous)**



I2C Reading Command Register(continuous)

- Start=Start Conditions
- Chip address =Write register address=0110101+0(w)b
- ack=Acknowledge from ET5907SX
- Write Reg start address byte = cmdadr(xxx + REG's 5bit addre)
- ack=Acknowledge from ET5907SX
- Restart=Restart condition
- Chip address Read register address=0110101+1(r)b
- ack=Acknowledge from ET5907SX
- Dataout0=Register data output 0
- ack=Acknowledge from Host
- ……
- Dataoutn=Register data output n
- nack=No Acknowledge from Host
- Stop/Rs=Stop Condition/Restart Condition

- **I2C Reading Command Register Interface Protocol(single)**



I2C Reading Command Register(single)

- Start=Start Conditions
- Chip address =Write register address=0110101+0(w)b
- ack=Acknowledge from ET5907SX
- Write Reg start address byte = cmdadr(xxx + REG's 5bit addre)
- ack=Acknowledge from ET5907SX
- Restart=Restart condition
- Chip address Read register address=0110101+1(r)b
- ack=Acknowledge from ET5907SX
- Dataout=Register data output
- nack=No Acknowledge from Host
- Stop/Rs=Stop Condition/Restart Condition

- **Register Map**

Addr	Name	RST	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0X00	CHIPID	0X01	000000						chip_id[1:0]	
0x01	VERID	0x00	000000						ver_id[1:0]	
0x02	LDO_ILIMIT	0x7F	0	ldo7_ilimt	ldo6_ilimt	ldo5_ilimt	ldo4_ilimt	ldo3_ilimt	ldo2_ilimt	ldo1_ilimt
0x03	LDO_EN	0x00	0	ldo7_en	ldo6_en	ldo5_en	ldo4_en	ldo3_en	ldo2_en	ldo1_en
0x04	LDO1_VSET	0x64	ldo1_vset[7:0]							
0x05	LDO2_VSET	0x64	ldo2_vset[7:0]							
0x06	LDO3_VSET	0xA0	ldo3_vset[7:0]							
0x07	LDO4_VSET	0xA0	ldo4_vset[7:0]							
0x08	LDO5_VSET	0xA0	ldo5_vset[7:0]							
0x09	LDO6_VSET	0xA0	ldo6_vset[7:0]							
0x0A	LDO7_VSET	0xA0	ldo7_vset[7:0]							
0x0B	LDO12_SEQ	0x00	00		ldo2_seq[2:0]			ldo1_seq[2:0]		
0x0C	LDO34_SEQ	0x00	00		ldo4_seq[2:0]			ldo3_seq[2:0]		
0x0D	LDO56_SEQ	0x00	00		ldo6_seq[2:0]			ldo5_seq[2:0]		
0x0E	LDO7_SEQ	0x00	00000					ldo7_seq[2:0]		
0x0F	SEQ_CTR	0x00	seq_speed[1:0]		seq_ctrl[1:0]		seq_on	seq_cnt[2:0]		
0x10	LDO_DIS	0x7F	0	ldo7_dis	ldo6_dis	ldo5_dis	ldo4_dis	ldo3_dis	ldo2_dis	ldo1_dis
0x11	RESET	0x07	soft_reset[3:0]				0	ocp_time[1:0]		flt_sd_b
0x12	I2C_ADDR	0x01	000000						I2C_addr_sel[1:0]	
0x13	Reserved	0x00								
0x14	Reserved	0x00								
0x15	UVP_INT	0x00	0	ldo6_uvp_int	ldo6_uvp_int	ldo5_uvp_int	ldo4_uvp_int	ldo3_uvp_int	ldo2_uvp_int	ldo1_uvp_int
0x16	OCP_INT	0x00	0	ldo7_ocp_int	ldo6_ocp_int	ldo5_ocp_int	ldo4_ocp_int	ldo3_ocp_int	ldo2_ocp_int	ldo1_ocp_int
0x17	TSD_UVLO_INT	0x00	tsd_int	tsd_wrn_int	vsys_uvlo_int	ldo7_uvlo_int	ldo6_uvlo_int	ldo5_uvlo_int	ldo34_uvlo_int	ldo12_uvlo_int
0x18	UVP_STAU	0x00	0	ldo7_uvp_stau	ldo6_uvp_stau	ldo5_uvp_stau	ldo4_uvp_stau	ldo3_uvp_stau	ldo2_uvp_stau	ldo1_uvp_stau
0x19	OCP_STAU	0x00	0	ldo7_ocp_stau	ldo6_ocp_stau	ldo5_ocp_stau	ldo4_ocp_stau	ldo3_ocp_stau	ldo2_ocp_stau	ldo1_ocp_stau
0x1A	TSD_UVLO_STAU	0x00	tsd_ stau	tsd_wrn_stau	vsys_uvlo_stau	ldo7_uvlo_stau	ldo6_uvlo_stau	ldo5_uvlo_stau	ldo34_uvlo_stau	ldo12_uvlo_stau
0x1B	SUSD_STAU	0x00	chip_susd_stau	ldo7_susd_stau	ldo6_susd_stau	ldo5_susd_stau	ldo4_susd_stau	ldo3_susd_stau	ldo2_susd_stau	ldo1_susd_stau
0x1C	UVP_INTMA	0x00	0	ldo7_uvp_mask	ldo6_uvp_mask	ldo5_uvp_mask	ldo4_uvp_mask	ldo3_uvp_mask	ldo2_uvp_mask	ldo1_uvp_mask
0x1D	OCP_INTMA	0x00	0	ldo7_ocp_mask	ldo6_ocp_mask	ldo5_ocp_ mask	ldo4_ocp_mask	ldo3_ocp_mask	ldo2_ocp_mask	ldo1_ocp_mask
0x1E	TSD_UVLO_INTMA	0x00	tsd_mask	tsd_wrn_mask	vsys_uvlo_mask	ldo7_uvlo_mask	ldo6_uvlo_mask	ldo5_uvlo_mask	ldo34_uvlo_mask	ldo12_uvlo_mask

- **0x00 CHIPID Register---- Indicates the product ID with revision. Default=0x01 type: Read only**

  chip_id[1:0] Indicates the product ID with revision. Read only.

- **0x01 VERID Register---- Indicates the device ID with revision. Default = 0x00 type: Read only**

  ver_id[1:0] Indicates the device ID with revision. Read only.

- **0x02 LDO_ILIMIT Register ----LDO Current Limit Selection. Default = 0x7F**

  The detail current limit threshold value is shown in the table as below:

Bit	Name	Default	Type	Description
7	Rev.	0	R	Reserved
6	ldo7_ilimt	1	R/W	LDO7 current limit threshold value: 0b: current limit~420mA short current limit~ 35mA 1b: current limit~550mA short current limit~ 45mA
5	ldo6_ilimt	1	R/W	LDO6 current limit threshold value: 0b: current limit~420mA short current limit~ 35mA 1b: current limit~550mA short current limit~ 45mA
4	ldo5_ilimt	1	R/W	LDO5 current limit threshold value: 0b: current limit~420mA short current limit~ 35mA 1b: current limit~550mA short current limit~ 45mA
3	ldo4_ilimt	1	R/W	LDO4 current limit threshold value: 0b: current limit~420mA short current limit~ 35mA 1b: current limit~550mA short current limit~ 45mA
2	ldo3_ilimt	1	R/W	LDO3 current limit threshold value: 0b: current limit~420mA short current limit~ 35mA 1b: current limit~550mA short current limit~ 45mA
1	ldo2_ilimt	1	R/W	LDO2 current limit threshold value: 0b: current limit~1200mA short current limit~ 300mA 1b: current limit~1400mA short current limit~ 350mA
0	ldo1_ilimt	1	R/W	LDO1 current limit threshold value: 0b: current limit~1200mA short current limit~ 300mA 1b: current limit~1400mA short current limit~ 350mA

- **0x03 LDO_EN Register ----LDOs Chip enable control register. Default = 0x00**

LDO enable control register by I2C while the register value of ldox_seq[2:0] are set to be default “000”. This register can be written to enable or disable the corresponding LDO regulator.

Bit	Name	Default	Type	Description
7	Rev.	0	R	Reserved
6	ldo7_en	0	R/W	LDO7 enable control: 0b: Disable 1b: Enable

5	ldo6_en	0	R/W	LDO6 enable control: 0b: Disable 1b: Enable
4	ldo5_en	0	R/W	LDO5 enable control: 0b: Disable 1b: Enable
3	ldo4_en	0	R/W	LDO4 enable control: 0b: Disable 1b: Enable
2	ldo3_en	0	R/W	LDO3 enable control: 0b: Disable 1b: Enable
1	ldo2_en	0	R/W	LDO2 enable control: 0b: Disable 1b: Enable
0	ldo1_en	0	R/W	LDO1 enable control: 0b: Disable 1b: Enable

- **0x04 LDO1 Register ---- LDO1 output voltage setting register. Default = 0x64 Type: R/W**
- **0x05 LDO2 Register ---- LDO2 output voltage setting register. Default = 0x64 Type: R/W**

The register LDO1/2_VSET[7:0] set the voltage of LDO1/ LDO2, it have 200 steps, shown as below table, the formula is VOUT =0.600V + [d*6mV];

LDO1/LDO2 Output Voltage set by LDO1/2_VSET[7:0]		
Dec	**Binary**	**Output Voltage(V)**
0	00000000	0.600
1	00000001	0.606
2	00000010	0.612
3	00000011	0.618
……	…..	……
33	00100001	0.798
34	00100011	0.804
35	00100100	0.810
……	……	……
100	**01100100(default)**	**1.200**
101	01100101	1.206
102	01100110	1.212
……	……	……
200	11001000	1.8
201~255	11001001~11111111	Reserved

VOUT is less than 0.8V, which is not recommended. If you need to use it, please contact us.

- **0x06~0x0A LDO3~7 Register ---- LDO3~7 output voltage setting register. Default = 0xA0 Type: R/W**

The registers LDO3~7_VSET[7:0] set the voltage of LDO3~LDO7, each voltage have 226 steps, shown as below table, the formula is VOUT=1.200V + [d*10mV].

LDO1/LDO2 Output Voltage set by LDO1/2_VSET[7:0]		
Dec	**Binary**	**Output Voltage(V)**
0~29	00000000~00011101	Reservedd
30	00011110	1.500
31	00011111	1.510
32	00100000	1.520
33	00100001	1.530
34	00100010	1.540
……	……	……
160	**10100000(default)**	**2.8V**
161	10100001	2.810
162	10100010	2.820
……	……	……
255	11111111	3.750

- **0x0B~0x0E LDO12/34/56/7_SEQ Register ---- Power sequence setting register. Default = 0x00**

Power sequence setting register. there are 7 time slots defined as following table. The power-up sequence is start from slot1 to slot7, and shut down start from slot7 to slot1. Power-up and shut down of each LDO regulator can be set at any one of the slots.

ldox_seq[2:0]	VOUTX
000	Controlled by I2C register ldox_en
001	Slot1
010	Slot2
011	Slot3
100	Slot4
101	Slot5
110	Slot6
111	Slot7

- **0x0F SEQ_CTR Register ---- Power sequence setting and status register. Default = 0x00**

<table>
<tr><th>Bit</th><th>Name</th><th>Default</th><th>Type</th><th>Description</th></tr>
<tr><td>7:6</td><td>seq_speed[1:0]</td><td>00</td><td>R/W</td><td>Define the slot period as following:
<table>
<tr><th>Register Value</th><th>Slot period(ms)</th></tr>
<tr><td>00</td><td>0.5</td></tr>
<tr><td>01</td><td>1.0</td></tr>
<tr><td>10</td><td>1.5</td></tr>
<tr><td>11</td><td>2.0</td></tr>
</table></td></tr>
<tr><td>5:4</td><td>seq_ctrl[1:0]</td><td>00</td><td>W/C</td><td>Enables power-up or shut down of SEQ:
<table>
<tr><th>Register Value</th><th>Description</th></tr>
<tr><td>00</td><td>Default</td></tr>
<tr><td>01</td><td>Starts an LDO power up sequence</td></tr>
<tr><td>10</td><td>Starts an LDO shutdown sequence</td></tr>
<tr><td>11</td><td>Bit configuration is ignored</td></tr>
</table>
Note: The bits will always clear immediately when written to and always read back 00.</td></tr>
<tr><td>3</td><td>seq_on</td><td>0</td><td>R</td><td>Indicates the activation signal of SEQ.
0b: Indicates that the sequencing is not in process
1b: Indicates that the sequencing is executing and somewhere between the start of slot 1 and the end of slot 7. The bit remains a 1 until slot 7 has completed at start-up or slot 1 has finished at shutdown, regardless of what slots are used.</td></tr>
<tr><td>2:0</td><td>seq_cnt[2:0]</td><td>0</td><td>R</td><td>Indicates the slot number of SEQ at the moment:
<table>
<tr><th>Register Value</th><th>SEQ Counter</th></tr>
<tr><td>000</td><td>Sequencing has completed or not started</td></tr>
<tr><td>001</td><td>Indicates was in slot 1 during register read</td></tr>
<tr><td>010</td><td>Indicates was in slot 2 during register read</td></tr>
<tr><td>011</td><td>Indicates was in slot 3 during register read</td></tr>
<tr><td>100</td><td>Indicates was in slot 4 during register read</td></tr>
<tr><td>101</td><td>Indicates was in slot 5 during register read</td></tr>
<tr><td>110</td><td>Indicates was in slot 6 during register read</td></tr>
<tr><td>111</td><td>Indicates was in slot 7 during register read</td></tr>
</table></td></tr>
</table>

- **0x10 LDO_DIS Register ----Discharge Resistor Selection. Default = 0x7F**

  Each LDO regulators output discharge resistor enable control.

Bit	Name	Default	Type	Description
7	Rev.	0	R	Reserved
6	ldo7_dis	1	R/W	LDO7 Discharge Enabled/Disabled control: 0b: Disable Pull down will not be activated when LDO7 is disabled by any event 1b: Enable Pull down will be activated when LDO7 is disabled by RESET_N going low or ldo7_en=0 or a Sequenced shutdown or ldo7_susd_stau=1(VIN7_UVLO/LDO7_OCP/LDO7_UVP event) or chip_susd_stau=1(TSD or VSYS_UVLO event)
5	ldo6_dis	1	R/W	LDO6 Discharge Enabled/Disabled control: 0b: Disable Pull down will not be activated when LDO6 is disabled by any event 1b: Enable Pull down will be activated when LDO6 is disabled by RESET_N going low or ldo6_en=0 or a Sequenced shutdown or ldo6_susd_stau=1(VIN6_UVLO/LDO6_OCP/LDO6_UVP event) or chip_susd_stau=1(TSD or VSYS_UVLO event)
4	ldo5_dis	1	R/W	LDO5 Discharge Enabled/Disabled control: 0b: Disable Pull down will not be activated when LDO5 is disabled by any event 1b: Enable Pull down will be activated when LDO5 is disabled by RESET_N going low or ldo5_en=0 or a Sequenced shutdown or ldo5_susd_stau=1(VIN5_UVLO/LDO5_OCP/LDO5_UVP event) or chip_susd_stau=1(TSD or VSYS_UVLO event)
3	ldo4_dis	1	R/W	LDO4 Discharge Enabled/Disabled control: 0b: Disable Pull down will not be activated when LDO4 is disabled by any event 1b: Enable Pull down will be activated when LDO4 is disabled by RESET_N going low or ldo4_en=0 or a Sequenced shutdown or ldo4_susd_stau=1(VIN4_UVLO/LDO4_OCP/LDO4_UVP event) or chip_susd_stau=1(TSD or VSYS_UVLO event)

2	ldo3_dis	1	R/W	LDO3 Discharge Enabled/Disabled control: 0b: Disable Pull down will not be activated when LDO3 is disabled by any event 1b: Enable Pull down will be activated when LDO3 is disabled by RESET_N going low or ldo3_en=0 or a Sequenced shutdown or ldo3_susd_stau=1(VIN3_UVLO/LDO3_OCP/LDO3_UVP event) or chip_susd_stau=1(TSD or VSYS_UVLO event)
1	ldo2_dis	1	R/W	LDO2 Discharge Enabled/Disabled control: 0b: Disable Pull down will not be activated when LDO2 is disabled by any event 1b: Enable Pull down will be activated when LDO2 is disabled by RESET_N going low or ldo2_en=0 or a Sequenced shutdown or ldo2_susd_stau=1(VIN12_UVLO/LDO2_OCP/LDO2_UVP event) or chip_susd_stau=1(TSD or VSYS_UVLO event)
0	ldo1_dis	1	R/W	LDO1 Discharge Enabled/Disabled control: 0b: Disable Pull down will not be activated when LDO1 is disabled by any event 1b: Enable Pull down will be activated when LDO1 is disabled by RESET_N going low or ldo1_en=0 or a Sequenced shutdown or ldo1_susd_stau=1(VIN12_UVLO/LDO1_OCP/LDO1_UVP event) or chip_susd_stau=1(TSD or VSYS_UVLO event)

- **0x11 RESET Register ----LDOs reset control register. Default = 0x07**

Bit	Name	Default	Type	Description
7:4	soft_reset[3:0]	0000	W/C	Writing a "1011" begins a soft reset of the device I2C registers to their default values. This bit is cleared upon execution of the Reset function. Any other value than "1011" will be ignored.
3	Rev.	0	R	Reserved.
2:1	ocp_time[1:0]	11	R/W	Option bits to control the length of the deglitch timer for current limit on all LDOs before a fault is triggered: **Register Value** / **Slot period(us)** 00 / 125 01 / 250 10 / 500 11 / 1000

0	flt_sd_b	1	R/W	Prevents Shutdown When a Fault Occurs: 0b: LDO is shutdown if a UVP or OCP event occurs or if the LDO's input VIN12, VIN34, VIN5, VIN6 or VIN7 have a UVLO event. Each shutdown time is about 20ms, then restart again, when the times of shutdown are arrived to three, the according register bit ldox_en will be cleared. All LDO(s) are shutdown if a VSYS UVLO or TSD event occurs. Each shutdown time is about 20ms, then restart again, when the times of shutdown are arrived to four, the according register bit ldox_en will be cleared. ***Notes:*** If this bit function is desired, flt_sd_b should be set to "0" prior to enabling any LDOs after a Power-On-Reset. 1b: LDO is not shutdown if a UVP or OCP event occurs. If the LDO's input VIN12, VIN34, VIN5, VIN6 or VIN7 have a UVLO event, the associated LDO will be shutdown until the supply returns, but the fault will not be counted. If a VSYS UVLO or TSD event occurs, All LDO(s) will be shutdown until the VSYS supply returns and TSD is released, but the fault will not be counted.

- **0x12 ADDR Register ---- I2C address select register. Default = 0x01**

Bit	Name	Default	Type	Description
7:2	Rev.	000000	R	Reserved.
1:0	i2c_addr_sel[1:0]	01	R/W	Tunnel bits to change value for customer to select a different I2C address: **Register Value** / **I2C Address Settings** 00 / 0x20 01 / 0x35 10 / 0x61 11 / 0x72

- **0x15 UVP_INT Register ---- LDO UVP Interrupt register. Default = 0x00**

Bit	Name	Default	Type	Description
7	Rev.	0	R	Reserved
6	ldo7_uvp_int	0	R/C	LDO7 UVP Interrupt: 0b: Clear It can be cleared by reading this register or setting RESET_N pin to 0 1b: Under-Voltage event detected on the LDO7 output.
5	ldo6_uvp_int	0	R/C	LDO6 UVP Interrupt: 0b: Clear It can be cleared by reading this register or setting RESET_N pin to 0 1b: Under-Voltage event detected on the LDO6 output.
4	ldo5_uvp_int	0	R/C	LDO5 UVP Interrupt: 0b: Clear It can be cleared by reading this register or setting RESET_N pin to 0 1b: Under-Voltage event detected on the LDO5 output.
3	ldo4_uvp_int	0	R/C	LDO4 UVP Interrupt: 0b: Clear It can be cleared by reading this register or setting RESET_N pin to 0 1b: Under-Voltage event detected on the LDO4 output.
2	ldo3_uvp_int	0	R/C	LDO3 UVP Interrupt: 0b: Clear It can be cleared by reading this register or setting RESET_N pin to 0 1b: Under-Voltage event detected on the LDO3 output.
1	ldo2_uvp_int	0	R/C	LDO2 UVP Interrupt: 0b: Clear It can be cleared by reading this register or setting RESET_N pin to 0 1b: Under-Voltage event detected on the LDO2 output.
0	ldo1_uvp_int	0	R/C	LDO1 UVP Interrupt: 0b: Clear It can be cleared by reading this register or setting RESET_N pin to 0 1b: Under-Voltage event detected on the LDO1 output.

- **0x16 OCP_INT Register ---- LDO OCP Interrupt Register. Default = 0x00**

Bit	Name	Default	Type	Description
7	Rev.	0	R	Reserved
6	ldo7_ocp_int	0	R/C	LDO7 OCP Interrupt : 0b:Clear It can be cleared by reading this register or setting RESET_N pin to 0 1b: Over current event detected on the LDO7 output.

5	ldo6_ocp_int	0	R/C	LDO6 OCP Interrupt : 0b:Clear It can be cleared by reading this register or setting RESET_N pin to 0 1b: Over current event detected on the LDO6 output.
4	ldo5_ocp_int	0	R/C	LDO5 OCP Interrupt : 0b:Clear It can be cleared by reading this register or setting RESET_N pin to 0 1b: Over current event detected on the LDO5 output.
3	ldo4_ocp_int	0	R/C	LDO4 OCP Interrupt : 0b:Clear It can be cleared by reading this register or setting RESET_N pin to 0 1b: Over current event detected on the LDO4 output.
2	ldo3_ocp_int	0	R/C	LDO3 OCP Interrupt : 0b:Clear It can be cleared by reading this register or setting RESET_N pin to 0 1b: Over current event detected on the LDO3 output.
1	ldo2_ocp_int	0	R/C	LDO2 OCP Interrupt : 0b:Clear It can be cleared by reading this register or setting RESET_N pin to 0 1b: Over current event detected on the LDO2 output.
0	ldo1_ocp_int	0	R/C	LDO1 OCP Interrupt : 0b:Clear It can be cleared by reading this register or setting RESET_N pin to 0 1b: Over current event detected on the LDO1 output.

- **0x17 TSD_UVLO_INT Register ---- TSD and UVLO Interrupt Register. Default = 0x00**

Bit	Name	Default	Type	Description
7	tsd_int	0	R/C	Thermal Shutdown Interrupt: 0b: Clear It can be cleared by reading this register or setting RESET_N pin to 0 1b: A Thermal Shutdown event detected or that the temperature has fallen below the hysteresis level.
6	tsd_wrn_int	0	R/C	Thermal Warning Interrupt: 0b: Clear It can be cleared by reading this register or setting RESET_N pin to 0 1b: Thermal Shutdown Warning threshold was surpassed or that the temperature has fallen below the hysteresis level.
5	vsys_uvlo_int	0	R/C	VSYS Under-Voltage-Lock-Out Interrupt: 0b: Normal operation It can be cleared by reading this register or setting RESET_N pin to 0 1b: Indicates that the VSYS power fell below the UVLO input

				threshold or that the supplies have risen above the rising thresholds after a UVLO fault
4	ldo7_uvlo_int	0	R/C	VIN7 Under-Voltage-Lock-Out Interrupt: 0b: Normal operation It can be cleared by reading this register or setting RESET_N pin to 0 1b: Indicates that the VIN7 power fell below the UVLO input threshold or that the supplies have risen above the rising thresholds after a UVLO fault
3	ldo6_uvlo_int	0	R/C	VIN6 Under-Voltage-Lock-Out Interrupt: 0b: Normal operation It can be cleared by reading this register or setting RESET_N pin to 0 1b: Indicates that the VIN6 power fell below the UVLO input threshold or that the supplies have risen above the rising thresholds after a UVLO fault
2	ldo5_uvlo_int	0	R/C	VIN5 Under-Voltage-Lock-Out Interrupt: 0b: Normal operation It can be cleared by reading this register or setting RESET_N pin to 0 1b: Indicates that the VIN5 power fell below the UVLO input threshold or that the supplies have risen above the rising thresholds after a UVLO fault
1	ldo34_uvlo_int	0	R/C	VIN34 Under-Voltage-Lock-Out Interrupt: 0b: Normal operation It can be cleared by reading this register or setting RESET_N pin to 0 1b: Indicates that the VIN34 power fell below the UVLO input threshold or that the supplies have risen above the rising thresholds after a UVLO fault
0	ldo12_uvlo_int	0	R/C	VIN12 Under-Voltage-Lock-Out Interrupt: 0b: Normal operation It can be cleared by reading this register or setting RESET_N pin to 0 1b: Indicates that the VIN12 power fell below the UVLO input threshold or that the supplies have risen above the rising thresholds after a UVLO fault

- **0x18 UVP_STAU Register ---- LDO UVP Status Register. Default = 0x00**

Bit	Name	Default	Type	Description
7	Rev.	0	R	Reserved
6	ldo7_uvp_stau	0	R	LDO7 UVP Status: 0b: Clear 1b: Under-Voltage event occurred on LDO7 output while LDO7 is been commanded to be enabled.

5	ldo6_uvp_stau	0	R	LDO6 UVP Status: 0b: Clear 1b: Under-Voltage event occurred on LDO6 output while LDO6 is been commanded to be enabled.
4	ldo5_uvp_stau	0	R	LDO5 UVP Status: 0b: Clear 1b: Under-Voltage event occurred on LDO5 output while LDO5 is been commanded to be enabled.
3	ldo4_uvp_stau	0	R	LDO4 UVP Status: 0b: Clear 1b: Under-Voltage event occurred on LDO4 output while LDO4 is been commanded to be enabled.
2	ldo3_uvp_stau	0	R	LDO3 UVP Status: 0b: Clear 1b: Under-Voltage event occurred on LDO3 output while LDO3 is been commanded to be enabled.
1	ldo2_uvp_stau	0	R	LDO2 UVP Status: 0b: Clear 1b: Under-Voltage event occurred on LDO2 output while LDO2 is been commanded to be enabled.
0	ldo1_uvp_stau	0	R	LDO1 UVP Status: 0b: Clear 1b: Under-Voltage event occurred on LDO1 output while LDO1 is been commanded to be enabled.

- **0x19 OCP_STAU Register ---- LDO OCP Status Register. Default = 0x00**

Bit	Name	Default	Type	Description
7	Rev.	0	R	Reserved
6	ldo7_ocp_stau	0	R	LDO7 OCP Status: 0b: Clear 1b: Over current event detected on the LDO7 output while LDO7 is been commanded to be enabled.
5	ldo6_ocp_stau	0	R	LDO6 OCP Status: 0b: Clear 1b: Over current event detected on the LDO6 output while LDO7 is been commanded to be enabled.
4	ldo5_ocp_stau	0	R	LDO5 OCP Status: 0b: Clear 1b: Over current event detected on the LDO5 output while LDO5 is been commanded to be enabled.

3	ldo4_ocp_stau	0	R	LDO4 OCP Status: 0b: Clear 1b: Over current event detected on the LDO4 output while LDO4 is been commanded to be enabled.
2	ldo3_ocp_stau	0	R	LDO3 OCP Status: 0b: Clear 1b: Over current event detected on the LDO3 output while LDO3 is been commanded to be enabled.
1	ldo2_ocp_stau	0	R	LDO2 OCP Status: 0b: Clear 1b: Over current event detected on the LDO2 output while LDO2 is been commanded to be enabled.
0	ldo1_ocp_stau	0	R	LDO1 OCP Status: 0b: Clear 1b: Over current event detected on the LDO1 output while LDO1 is been commanded to be enabled.

- **0x1A TSD_UVLO_STAU Register ---- TSD and UVLO Status Register. Default = 0x00**

Bit	Name	Default	Type	Description
7	tsd_stau	0	R	Thermal Shutdown Status: 0b: Normal operation 1b: A Thermal Shutdown event detected
6	tsd_wrn_stau	0	R	Thermal Warning Status: 0b: Normal operation 1b: The temperature is above the thermal Warning threshold and shutdown is impending.
5	vsys_uvlo_stau	0	R	VSYS Under-Voltage-Lock-Out Status: 0b: Normal operation 1b: Indicates that the VSYS power fell below the UVLO input threshold.
4	ldo7_uvlo_stau	0	R	VIN7 Under-Voltage-Lock-Out Status: 0b: Normal operation 1b: Indicates that the VIN7 power fell below the UVLO input threshold while LDO7 is been commanded to be enabled.
3	ldo6_uvlo_stau	0	R	VIN6 Under-Voltage-Lock-Out Status: 0b: Normal operation 1b: Indicates that the VIN6 power fell below the UVLO input threshold while LDO6 is been commanded to be enabled.
2	ldo5_uvlo_stau	0	R	VIN5 Under-Voltage-Lock-Out Status: 0b: Normal operation 1b: Indicates that the VIN5 power fell below the UVLO input

				threshold while LDO5 is been commanded to be enabled.
1	ldo34_uvlo_stau	0	R	VIN34 Under-Voltage-Lock-Out Status: 0b: Normal operation 1b: Indicates that the VIN34 power fell below the UVLO input threshold while LDO3 or LDO4 is been commanded to be enabled.
0	ldo12_uvlo_stau	0	R	VIN12 Under-Voltage-Lock-Out Status: 0b: Normal operation 1b: Indicates that the VIN12 power fell below the UVLO input threshold while LDO1 or LDO2 is been commanded to be enabled.

- **0x1B SUSD_STAU Register ---- LDO Suspend Status Register. Default = 0x00**

Bit	Name	Default	Type	Description
7	chip_susd_stau	0	R	Chip Suspension: 0b: Chip normal state 1b: The entire chip has been suspended due to a global fault condition
6	ldo7_susd_stau	0	R	LDO7 Output Suspended: 0b: LDO7 in normal state. 1b: LDO7 has been suspended due to a fault condition.
5	ldo6_susd_stau	0	R	LDO6 Output Suspended: 0b: LDO6 in normal state. 1b: LDO6 has been suspended due to a fault condition.
4	ldo5_susd_stau	0	R	LDO5 Output Suspended: 0b: LDO5 in normal state. 1b: LDO5 has been suspended due to a fault condition.
3	ldo4_susd_stau	0	R	LDO4 Output Suspended: 0b: LDO4 in normal state. 1b: LDO4 has been suspended due to a fault condition.
2	ldo3_susd_stau	0	R	LDO3 Output Suspended: 0b: LDO3 in normal state. 1b: LDO3 has been suspended due to a fault condition.
1	ldo2_susd_stau	0	R	LDO2 Output Suspended: 0b: LDO2 in normal state. 1b: LDO2 has been suspended due to a fault condition.
0	ldo1_susd_stau	0	R	LDO1 Output Suspended: 0b: LDO1 in normal state. 1b: LDO1 has been suspended due to a fault condition.

- **0x1C UVP_INTMA Register ---- LDO UVP Interrupt MASK Register. Default = 0x00**

Bit	Name	Default	Type	Description
7	Rev.	0	R	Reserved
6	ldo7_uvp_mask	0	R/W	LDO7 UVP Mask: 0b: No masking of interrupt. 1b: INTN pin will not change states when LDO7 Under Voltage interrupt occurs
5	ldo6_uvp_mask	0	R/W	LDO6 UVP Mask: 0b: No masking of interrupt. 1b: INTN pin will not change states when LDO6 Under Voltage interrupt occurs
4	ldo5_uvp_mask	0	R/W	LDO5 UVP Mask: 0b: No masking of interrupt. 1b: INTN pin will not change states when LDO5 Under Voltage interrupt occurs
3	ldo4_uvp_mask	0	R/W	LDO4 UVP Mask: 0b: No masking of interrupt. 1b: INTN pin will not change states when LDO4 Under Voltage interrupt occurs
2	ldo3_uvp_mask	0	R/W	LDO3 UVP Mask: 0b: No masking of interrupt. 1b: INTN pin will not change states when LDO3 Under Voltage interrupt occurs.
1	ldo2_uvp_mask	0	R/W	LDO2 UVP Mask: 0b: No masking of interrupt. 1b: INTN pin will not change states when LDO2 Under Voltage interrupt occurs
0	ldo1_uvp_mask	0	R/W	LDO1 UVP Mask: 0b: No masking of interrupt. 1b: INTN pin will not change states when LDO1 Under Voltage interrupt occurs

- **0x1D OCP_INTMA Register ---- LDO OCP Interrupt MASK Register. Default = 0x00**

Bit	Name	Default	Type	Description
7	Rev.	0	R	Reserved
6	ldo7_ocp_mask	0	R/W	LDO7 OCP Mask: 0b: No masking of interrupt. 1b: INTN pin will not change states when LDO7 Over-Current interrupt occurs.

5	ldo6_ocp_mask	0	R/W	LDO6 OCP Mask: 0b: No masking of interrupt. 1b: INTN pin will not change states when LDO6 Over-Current interrupt occurs.
4	ldo5_ocp_mask	0	R/W	LDO5 OCP Mask: 0b: No masking of interrupt. 1b: INTN pin will not change states when LDO5 Over-Current interrupt occurs.
3	ldo4_ocp_mask	0	R/W	LDO4 OCP Mask: 0b: No masking of interrupt. 1b: INTN pin will not change states when LDO4 Over-Current interrupt occurs.
2	ldo3_ocp_mask	0	R/W	LDO3 OCP Mask: 0b: No masking of interrupt. 1b: INTN pin will not change states when LDO3 Over-Current interrupt occurs.
1	ldo2_ocp_mask	0	R/W	LDO2 OCP Mask: 0b: No masking of interrupt. 1b: INTN pin will not change states when LDO2 Over-Current interrupt occurs.
0	ldo1_ocp_mask	0	R/W	LDO1 OCP Mask: 0b: No masking of interrupt. 1b: INTN pin will not change states when LDO1 Over-Current interrupt occurs.

- **0x1E TSD_UVLO_INTMA Register ---- TSD and UVLO Interrupt MASK Register. Default = 0x00**

Bit	Name	Default	Type	Description
7	tsd_mask	0	R/W	Thermal Shutdown Mask: 0b: No masking of interrupt. 1b: INTN pin will not change states when a Thermal Shutdown interrupt occurs.
6	tsd_wrn_mask	0	R/W	Thermal Warning Mask: 0b: No masking of interrupt. 1b: INTN pin will not change states when a Thermal Shutdown Warning interrupt occurs.
5	vsys_uvlo_mask	0	R/W	VSYS Under-Voltage-Lock-Out Mask: 0b: No masking of interrupt 1b: INTN pin will not change states when VSYS Input Power Under Voltage interrupt occurs.
4	ldo7_uvlo_mask	0	R/W	VIN7 Under-Voltage-Lock-Out Mask: 0b: No masking of interrupt

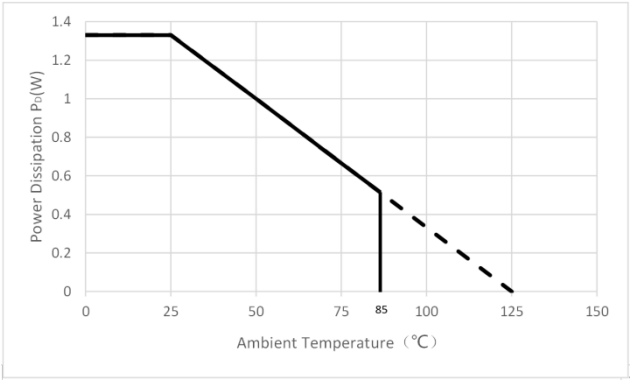
				1b: INTN pin will not change states when VIN7 Input Power Under Voltage interrupt occurs.
3	ldo6_uvlo_mask	0	R/W	VIN6 Under-Voltage-Lock-Out Mask: 0b: No masking of interrupt 1b: INTN pin will not change states when VIN6 Input Power Under Voltage interrupt occurs.
2	ldo5_uvlo_mask	0	R/W	VIN5 Under-Voltage-Lock-Out Mask: 0b: No masking of interrupt 1b: INTN pin will not change states when VIN5 Input Power Under Voltage interrupt occurs.
1	ldo34_uvlo _mask	0	R/W	VIN34 Under-Voltage-Lock-Out Mask: 0b: No masking of interrupt 1b: INTN pin will not change states when VIN34 Input Power Under Voltage interrupt occurs.
0	ldo12_uvlo _mask	0	R/W	VIN12 Under-Voltage-Lock-Out Mask: 0b: No masking of interrupt 1b: INTN pin will not change states when VIN12 Input Power Under Voltage interrupt occurs.

Absolute Maximum Ratings

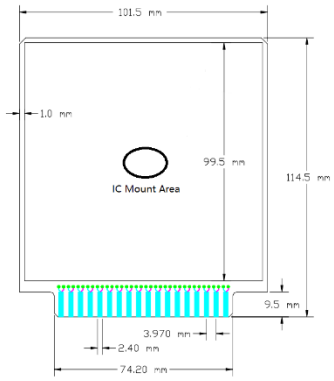
Symbol	Parameters (Items)	Value	Unit
V_{SYS}, V_{IN12}, V_{IN34}, V_{IN5}, V_{IN6}, V_{IN7}	POWER IN Pins Voltage	-0.3 to 6	V
LDO1~7	POWER OUT Pins Voltage	-0.3 to (V_{IN} + 0.3) ≤ 6	
SDA, SCL, RESET_N	SDA, SCL and RESET_N Pins Voltage	-0.3 to 6	V
INTN	INTN Pin Voltage	-0.3 to 6	V
$I_{MAX1/2}$	LDO1/2 Maximum Load Current	1200	mA
$I_{MAX3\sim7}$	LDO3~7 Maximum Load Current	400	mA
P_D[(1)(2)]	Maximum Power Consumption, Ta=25°C	1330	mW
$R_{\theta JA}$[(1)]	Thermal Resistance, Junction−to−Ambient,Ta=25°C	75	°C/W
T_J	Operating Junction Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-65 to 150	°C
T_{SLOD}	Lead Temperature (Soldering, 10 sec)	300	°C
ESD[(3)]	HMB	4000	V
	CDM	1500	V

Note (1): PD and $R_{\theta JA}$ are measured under natural convection (still air) at TA = 25°C with the component mounted on 101.5*114.5mm FR-4, 4layer, Top and Bottom layer 1.5oz, both two inner layer 1oz. Meet JEDEC（JESD51-9）standard.

Note (2): Recommended operating conditions are only used to limit the reasonable use range of the single condition of the product, and the circuit use must comply with other instructions in the manual. For parameter performance indicators, please refer to the EC table and the test condition specification in the table.



Power Dissipation



Measurement Board pattern

Note (3): This device series incorporates ESD protection and is tested by the following methods:

HBM tested per EIA/JESD22-A114

CDM tested per EIA/JESD22-C101

Recommended Operating Conditions

Symbol	Parameters	Rating	Unit
V_{VSYS}	Supply Input Voltage	2.7 to 5.5	V
V_{VIN12}	Supply Input Voltage	1.0 to 2.0	V
V_{VIN34}	Supply Input Voltage	1.9 to 5.5	V
V_{VIN5}	Supply Input Voltage	1.9 to 5.5	V
V_{VIN6}	Supply Input Voltage	1.9 to 5.5	V
V_{VIN7}	Supply Input Voltage	1.9 to 5.5	V
$I_{LDO3\sim7}$	Output Current(400mA LDO)	0 to 400	mA
$I_{LDO1/2}$	Output Current(1200mA LDO)	0 to 1200	mA
T_A	Operating Ambient Temperature	-40 to 85	ºC
C_{VIN12}	Effective Input Ceramic Capacitor Value	4.7 to 47	uF
C_{VSYS}/C_{VIN34}/ C_{VIN5}/C_{VIN6}/ C_{VIN7}	Effective Input Ceramic Capacitor Value	0.47 to 10	uF
C_{VREF}	Effective Bypass Ceramic Capacitor Value	0 to 1	uF
$C_{LDO1/2}$	Effective Output Ceramic Capacitor Value(1200mA LDO)	4.7 to 22	uF
$C_{LDO3\sim7}$	Effective Output Ceramic Capacitor Value(400mA LDO)	0.68 to 10	uF
ESR	Input and Output Capacitor Equivalent Series Resistance (ESR)	5 to 100	mΩ

Electrical Characteristics

(Unless otherwise noted, V_{VIN12}=$V_{LDO1/2}$+0.25V, V_{VSYS}=($V_{LDO1/2}$+1.6V) or 2.7V whichever greater, I_{OUT}=1mA, C_{VIN12}=10μF, C_{VSYS}=C_{VIN34}=C_{VIN5}=C_{VIN6}=C_{VIN7}=1uF, C_{LDO1}=C_{LDO2}=10μF, C_{LDO3}=C_{LDO4}=C_{LDO5}=C_{LDO6}=C_{LDO7}=1μF, C_{VREF}=0.1μF, Ta=-40°C~85°C. Typical values are at. Ta=25 ºC, V_{VSYS}=3.8V; V_{VIN12}=1.3V; V_{VIN34}, V_{VIN5}, V_{VIN6}, V_{VIN7}=3.8V; $V_{LDO1/2}$=1.05V, $V_{LDO3/4/5/6/7}$=2.8V.)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{VIN12}	VIN12 Input Voltage Range	V_{VIN12}>($V_{LDO1/2}$+$V_{DROP_LDO1/2}$)	1.0		2.0	V
V_{VIN34}[4], V_{VIN5}[4], V_{VIN6}[4], V_{VIN7}[4]	VIN34,VIN5,VIN6, VIN7 Input Voltage Range		1.9		5.5	V
V_{VSYS}[5]	VSYS Voltage Range	$V_{LDO1/2}$+1.6V, V_{VSYS}≥2.7V & V_{VSYS}>V_{LDOx}+0.5V	2.7		5.5	V
V_{UVLO_VSYS}	VSYS Under-voltage lock-out	Rising, Ta=25 ºC	2.3	2.55	2.8	V
		Falling, Ta=25 ºC	1.95	2.2	2.45	V
V_{UVLO_VIN12}	VIN12 Under-voltage lock-out	Rising	0.8	0.9	1.1	V
		Falling	0.7	0.85	1.0	V
V_{UVLO_VIN34}, V_{UVLO_VIN5}, V_{UVLO_VIN6}, V_{UVLO_VIN7}	VIN34,VIN5,VIN6, VIN7 Under-voltage lock-out	Rising	1.7	1.8	1.9	V
		Falling	1.65	1.75	1.8	V
I_{Q_ON}[9]	V_{VSYS} Current	Active mode: V_{RESET_N}=High and enable all LDO by I²C, no load	90	150	250	μA
I_{Q_OFF}[9]		V_{RESET_N}=0V	0.01	1.5	3	μA
I_{Q_STB}[9]		V_{RESET_N}=V_{VSYS} and disable chip by I²C	10	30	45	μA
I_{RESET_N}	RESET_N Pull-down Current	V_{RESET_N}=5.5V, V_{VSYS}=5.5V	0.01	0.3	1	μA
V_{RESET_NH}	RESET_N Input Voltage High		0.9			V
V_{RESET_NL}	RESET_N Input Voltage Low				0.4	V
V_{I2CH}	SCL/SDA Input Voltage High		0.9			V
V_{I2CL}	SCL/SDA Input Voltage Low				0.3	V
V_{OL}	SDA Logic Low Output	3mA Sink			0.4	V

Electrical Characteristics (Continued)

(Unless otherwise noted, V_{VIN12}=$V_{LDO1/2}$+0.25V, V_{VSYS}=($V_{LDO1/2}$+1.6V) or 2.7V whichever greater, I_{OUT}=1mA, C_{VIN12}=10μF, C_{VSYS}=C_{VIN34}=C_{VIN5}=C_{VIN6}=C_{VIN7}=1uF, C_{LDO1}=C_{LDO2}=10μF, C_{LDO3}=C_{LDO4}=C_{LDO5}=C_{LDO6}=C_{LDO7}=1μF, C_{VREF}=0.1μF, Ta=-40°C~85°C. Typical values are at. Ta=25 ºC, V_{VSYS}=3.8V; V_{VIN12}=1.3V; V_{VIN34}, V_{VIN5}, V_{VIN6}, V_{VIN7}=3.8V; $V_{LDO1/2}$=1.05V, $V_{LDO3/4/5/6/7}$=2.8V.)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{OL_INTN}	INTN Output Low Voltage	3mA Sink			0.4	V
T_{TSD}(6)	Thermal shutdown threshold	T_J rising	130	145	165	°C
T_{HYS_TSD}(6)	Thermal shutdown hysteresis	T_J falling from shutdown		25		°C
T_{TSB}(6)	Thermal warning threshold	T_J rising		125		°C
T_{HYS_TSB}(6)	Thermal warning hysteresis	T_J falling from warning		25		°C

1200mA LDO1/2

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{LDO1/2}$	Output Voltage	I_{OUT}=1mA~1200mA, Ta=25ºC	-1.0		1.0	%
		I_{OUT}=10mA, Ta=-40°C~85°C	-1.5		1.5	%
$V_{DROP_LDO1/2}$(7)	Dropout Voltage	I_{OUT}=500mA, V_{OUT}=1.05V		50	75	mV
		I_{OUT}=1000mA, V_{OUT}=1.05V		100	150	
$IQ_{LDO1/2_VSYS}$	Quiescent Current	Only LDO1 or LDO2 on, no load. Total current on VSYS		65	100	uA
$IQ_{LDO1/2_VIN}$		Only LDO1 or LDO2 on, no load. Total current on VIN12		10	20	uA
$I_{Q_OFF_LDO1/2}$	VIN12 Standby Current	V_{VSYS}=V_{VIN12}=3.8V, V_{RESET_N}=0V or Shutdown by I^2C		0.1	1	uA
$I_{OUT_LDO1/2}$	Output Current		1200			mA
$I_{LIM_LDO1/2}$	Current Limit	Default Ilimit register value, Ta=25ºC	1200	1400	2500	mA
$I_{SHORT_LDO1/2}$	Short Current Limit	Default Ilimit register value $V_{LDO1/2}$=0V, Ta=25ºC	200	350	500	mA
$UVP_{LDO1/2}$(10)	OUTPUT Under Voltage Protection	Falling, V_{OUT}=1.05V @V_{VSYS}-V_{OUT}>1.1V	87.5	90		% $V_{_target}$
		Rising, V_{OUT}=1.05V @V_{VSYS}-V_{OUT}>1.1V		95	97.5	% $V_{_target}$
$TMR_{LDO1/2}$	LDO1/2 Protection Timer	V_{OUT}=1.05V, Time between V_{OUT} forced to 0.9V and INIT going low	50	80	110	us
$Reg_{LOAD_LDO1/2}$	Load Regulation	1mA≤I_{OUT}≤1200mA		0.002	0.005	%/mA

Electrical Characteristics (Continued)

(Unless otherwise noted, V_{VIN12}=$V_{LDO1/2}$+0.25V, V_{VSYS}=($V_{LDO1/2}$+1.6V) or 2.7V whichever greater, I_{OUT}=1mA, C_{VIN12}=10μF, C_{VSYS}=C_{VIN34}=C_{VIN5}=C_{VIN6}=C_{VIN7}=1uF, C_{LDO1}=C_{LDO2}=10μF, C_{LDO3}=C_{LDO4}=C_{LDO5}=C_{LDO6}=C_{LDO7}=1μF, C_{VREF}=0.1μF, Ta=-40°C~85°C. Typical values are at. Ta=25 ºC, V_{VSYS}=3.8V; V_{VIN12}=1.3V; V_{VIN34}, V_{VIN5}, V_{VIN6}, V_{VIN7}=3.8V; $V_{LDO1/2}$=1.05V, $V_{LDO3/4/5/6/7}$=2.8V.)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$Reg_{LINE_LDO1/2}$	V_{VIN12} Line Regulation	$V_{LDO1/2}$+0.25V≤V_{VIN12}≤2V (I_{OUT}=1mA)		0.01	0.5	%/V
	V_{VSYS} Line Regulation	2.7V or ($V_{LDO1/2}$+1.6V) whichever greater <V_{VSYS}<5.5V, V_{VIN12}=$V_{LDO1/2}$+0.25V, I_{OUT}=1mA		0.01	0.2	%/V
$PSRR_{_LDO1/2}$[6]	Ripple Rejection	V_{IN} to V_{OUT}, f=100Hz, Ripple 0.2Vp-p, I_{OUT}=30mA		80		dB
		V_{IN} to V_{OUT}, f=1kHz, Ripple 0.2Vp-p, I_{OUT}=30mA	65	80	100	
		V_{IN} to V_{OUT}, f=10kHz, Ripple 0.2Vp-p, I_{OUT}=30mA		60		
		V_{IN} to V_{OUT}, f=100kHz, Ripple 0.2Vp-p, I_{OUT}=30mA		40		
		V_{IN} to V_{OUT}, f=1MHz, Ripple 0.2Vp-p, I_{OUT}=30mA		35		
		V_{VSYS} to V_{OUT}, f=1kHz, Ripple 0.2Vp-p, I_{OUT}=30mA	65	80	100	
$e_{N_LDO1/2}$[6]	Output Noise	V_{VIN12}=1.55V, V_{OUT}=1.05V, Iout=30mA, f=10Hz to 100kHz		30	100	μV_{RMS}
$R_{LOW_LDO1/2}$	Output resistance of auto discharge at off state	V_{RESET_N}=0V, or Shutdown by I^2C, V_{OUT}=0.5V, Ta=25ºC V_{SYS}=3.8V, V_{IN12}=1.3V	250	350	450	Ω
$V_{TRLN_LDO1/2}$[6]	Line transient	V_{VIN12}=$V_{LDO1/2}$+0.3V to $V_{LDO1/2}$+1.3V≤2V in 10us, I_{OUT}=1mA, Ta=25ºC		18	30	mV
		V_{VIN12}=$V_{LDO1/2}$+1.3V to $V_{LDO1/2}$+0.3V≤2V in 10us, I_{OUT}=1mA, Ta=25ºC		18	30	mV
$V_{TRLD_+LDO1/2}$[6]	Load transient	I_{OUT}=1mA to 1200mA in 10us V_{VIN12}=$V_{LDO1/2}$+0.5V≤2V, Ta=25ºC		120	180	mV
		I_{OUT}=1200mA to 1mA in 10us V_{VIN12}=$V_{LDO1/2}$+0.5V≤2V, Ta=25ºC		80	120	mV
$T_{ON_LDO1/2}$[6][8]	Turn-On Time	V_{OUT}≥0.8V From assertion of enable to V_{OUT}=95%$V_{LDO1/2(NOM)}$		450	900	μs

Electrical Characteristics (Continued)

(Unless otherwise noted, V_{VIN12}=$V_{LDO1/2}$+0.25V, V_{VSYS}=($V_{LDO1/2}$+1.6V) or 2.7V whichever greater, I_{OUT}=1mA, C_{VIN12}=10μF, C_{VSYS}=C_{VIN34}=C_{VIN5}=C_{VIN6}=C_{VIN7}=1uF, C_{LDO1}=C_{LDO2}=10μF, C_{LDO3}=C_{LDO4}=C_{LDO5}=C_{LDO6}=C_{LDO7}=1μF, C_{VREF}=0.1μF, Ta=-40°C~85°C. Typical values are at. Ta=25 ºC, V_{VSYS}=3.8V; V_{VIN12}=1.3V; V_{VIN34}, V_{VIN5}, V_{VIN6}, V_{VIN7}=3.8V; $V_{LDO1/2}$=1.05V, $V_{LDO3/4/5/6/7}$=2.8V.)

400mA LDO3/LDO4

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{DROP_LDO3/4}$[7]	Dropout Voltage	I_{OUT}=400mA, $V_{LDO3/4}$=1.8V		150	300	mV
		I_{OUT} =400mA, $V_{LDO3/4}$=2.8V		110	175	mV
$V_{LDO3/4}$	Regulated Output Voltage	I_{OUT}=1mA~400mA, Ta=25°C	-2		2	%
		I_{OUT}=1mA, Ta =-40°C~85°C	-2		2	
$Reg_{LINE_LDO3/4}$	Output Voltage Line Regulation	$V_{LDO3/4}$=2.8V 3.3V≤V_{VIN34}≤5.5V, I_{OUT}=10mA ($\Delta V_{LDO3/4}/\Delta V_{VIN34}/V_{LDO3/4}$)		0.01	0.5	%/V
$Reg_{LOAD_LDO3/4}$	Output Voltage Load Regulation	I_{OUT} from 1mA to 400mA $\Delta V_{LDO3/4}$		0.002	0.005	%/mA
$V_{TRLN_LDO3/4}$[6]	Line Transient (The absolute value of the output change)	$V_{LDO3/4}$=2.8V, I_{OUT}=1mA, V_{VIN34} =3.8V to 5.5V in 10us, Ta=25°C		5	20	mv
		$V_{LDO3/4}$=2.8V, I_{OUT}=1mA, V_{VIN34}=5.5V to 3.8V in 10us, Ta=25°C		5	20	
		I_{OUT}=1mA, V_{VIN34} =V_{OUT}+1 to 5.5V at 10us/V, Ta=25°C		5	35	
		I_{OUT}=1mA, V_{VIN34}=5.5V to V_{OUT}+1 at 10us/V, Ta=25°C		5	35	
$V_{TRLD_LDO3/4}$[6]	Load Transient (The absolute value of the output change)	$V_{LDO3/4}$=2.8V, V_{VIN34}=3.8V, I_{OUT} from 1mA to 400mA in 10us, Ta=25°C		40	80	mv
		$V_{LDO3/4}$=2.8V, V_{VIN34}=3.8V, I_{OUT} from 400mA to 1mA in 10us, Ta=25°C		40	80	
$IQ_{LDO3/4_VSYS}$	Quiescent Current	Only LDO3 or LDO4 on, no load. Total current on VSYS		30	55	uA
$IQ_{LDO3/4_VIN}$		Only LDO3 or LDO4 on, no load. Total current on VIN34		14	30	uA
$I_{Q_OFF_LDO3/4}$	VIN3~4 Standby Current	V_{VSYS}=$V_{VIN3/4}$=3.8V, V_{RESET_N}=0V or Shutdown by I^2C		0.1	1	uA

Electrical Characteristics (Continued)

(Unless otherwise noted, V_{VIN12}=$V_{LDO1/2}$+0.25V, V_{VSYS}=($V_{LDO1/2}$+1.6V) or 2.7V whichever greater, I_{OUT}=1mA, C_{VIN12}=10μF, C_{VSYS}=C_{VIN34}=C_{VIN5}=C_{VIN6}=C_{VIN7}=1uF, C_{LDO1}=C_{LDO2}=10μF, C_{LDO3}=C_{LDO4}=C_{LDO5}=C_{LDO6}=C_{LDO7}=1μF, C_{VREF}=0.1μF, Ta=-40°C~85°C. Typical values are at. Ta=25 ºC, V_{VSYS}=3.8V; V_{VIN12}=1.3V; V_{VIN34}, V_{VIN5}, V_{VIN6}, V_{VIN7}=3.8V; $V_{LDO1/2}$=1.05V, $V_{LDO3/4/5/6/7}$=2.8V.)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$I_{OUT_LDO3/4}$	Output Current		400			mA
$I_{LMT_LDO3/4}$	Over Current Limit	Default Ilimit register value, V_{VIN34}=V_{LDOx_VSET}+1V, Ta=25ºC	400	550	900	mA
$I_{SHORT_LDO3/4}$	Short Current Limit	Default Ilimit register value, $V_{LDO3/4}$=0V, Ta=25ºC	20	45	80	mA
$UVP_{LDO3/4}$(10)	OUTPUT Under Voltage Protection	Falling, V_{OUT}=2.8V @V_{VSYS}-V_{OUT}>1.1V	77	80		% V_{target}
		Rising, V_{OUT}=2.8V @V_{VSYS}-V_{OUT}>1.1V		90	93	% V_{target}
$TMR_{LDO3/4}$	LDO3/4 Protection Timer	V_{OUT}=2.8V, Time between V_{OUT} forced to 2.2V and INIT going low	50	80	110	us
$PSRR_{LDO3/4}$(6)	Power Supply Rejection Ratio	f=100Hz, $C_{LDO3/4}$=1μF, I_{OUT}=20mA, V_{IN} to V_{OUT}, V_{VSYS}=V_{LDOx_VSET}+1V, Ripple 0.4Vp-p, Ta=25°C		90		dB
		f=1kHz, $C_{LDO3/4}$=1μF, I_{OUT}=20mA, V_{IN} to V_{OUT}, V_{VSYS}=V_{LDOx_VSET}+1V, Ripple 0.4Vp-p, Ta=25°C	72	92	112	
		f=10kHz, $C_{LDO3/4}$=1μF, I_{OUT}=20mA, V_{IN} to V_{OUT}, V_{VSYS}=V_{LDOx_VSET}+1V, Ripple 0.4Vp-p, Ta=25°C		95		
		f=100kHz, $C_{LDO3/4}$=1μF, I_{OUT}=20mA, V_{IN} to V_{OUT}, V_{VSYS}=V_{LDOx_VSET}+1V, Ripple 0.4Vp-p, Ta=25°C		60		
		f=1MHz, $C_{LDO3/4}$=1μF, I_{OUT}=20mA, V_{IN} to V_{OUT}, V_{VSYS}=V_{LDOx_VSET}+1V, Ripple 0.4Vp-p, Ta=25°C		40		
		f=1kHz, I_{OUT}=20mA, Ta=25°C V_{VSYS} to V_{OUT}, Ripple 0.4Vp-p,		105		
e_N(6)	Output Noise	10Hz to 100kHz, I_{OUT}=30mA, $V_{LDO3/4}$=2.8V, V_{VSYS}=V_{VIN34}=3.8, $C_{LDO3\sim4}$=1μF, Ta=25°C		10	100	μV_{RMS}
$R_{LOW_LDO3/4}$	Output resistance of auto discharge at off state	V_{SYS}=V_{IN34}=3.8V, V_{RESET_N}=0V, or Shutdown by I^2C, I_{OUT}=10mA, Ta=25 ºC	250	350	450	Ω
$T_{ON_LDO3/4}$(6)(8)	Output Turn-on Delay Time	From enable to V_{OUT}=95% of V_{OUT}(NOM)		180	300	us

Electrical Characteristics (Continued)

(Unless otherwise noted, V_{VIN12}=$V_{LDO1/2}$+0.25V, V_{VSYS}=($V_{LDO1/2}$+1.6V) or 2.7V whichever greater, I_{OUT}=1mA, C_{VIN12}=10μF, C_{VSYS}=C_{VIN34}=C_{VIN5}=C_{VIN6}=C_{VIN7}=1uF, C_{LDO1}=C_{LDO2}=10μF, C_{LDO3}=C_{LDO4}=C_{LDO5}=C_{LDO6}=C_{LDO7}=1μF, C_{VREF}=0.1μF, Ta=-40°C~85°C. Typical values are at. Ta=25 ºC, V_{VSYS}=3.8V; V_{VIN12}=1.3V; V_{VIN34}, V_{VIN5}, V_{VIN6}, V_{VIN7}=3.8V; $V_{LDO1/2}$=1.05V, $V_{LDO3/4/5/6/7}$=2.8V.)

400mA LDO5~LDO7

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$V_{DROP_LDO5\sim7}$(7)	Dropout Voltage	I_{OUT}=400mA, $V_{LDO5\sim7}$=1.8V		150	300	mV
		I_{OUT}=400mA, $V_{LDO5\text{-}7}$=2.8V		110	175	mV
$V_{LDO5\sim7}$	Regulated Output Voltage	I_{OUT}=1mA~400mA,Ta=25°C	-2		2	%
		I_{OUT}=1mA~400mA, Ta=-40°C~85°C	-2		2	
$Reg_{LINE_LDO5\sim7}$	Output Voltage Line Regulation	$V_{LDO5\sim7}$=2.8V 3.3V≤$V_{VIN5\sim7}$≤5.5V, I_{OUT}=10mA ($\Delta V_{LDO5\sim7}/\Delta V_{VINX}/V_{LDO5\sim7}$）		0.01	0.5	%/V
$Reg_{LOAD_LDO5\sim7}$	Output Voltage Load Regulation	I_{OUT} from 1mA to 400mA $\Delta V_{LDO5\sim7}$		0.002	0.005	%/mA
$V_{TRLN_LDO5\sim7}$(6)	Line Transient (The absolute value of the output change)	$V_{LDO5\sim7}$=2.8V, I_{OUT}=1mA, $V_{VIN5\sim7}$=3.8V to 5.5V in 10us, Ta=25°C		5	20	mv
		$V_{LDO5\sim7}$=2.8V, I_{OUT}=1mA, $V_{IN5\sim7}$=5.5V to 3.8V in 10us, Ta=25°C		5	20	
		I_{OUT}=1mA, $V_{VIN5\sim7}$=V_{OUT}+1 to 5.5V at 10us/V, Ta=25°C		5	35	
		I_{OUT}=1mA, $V_{VIN5\sim7}$=5.5V to V_{OUT}+1 at 10us/V, Ta=25°C		5	35	
$V_{TRLD_LDO5\sim7}$(6)	Load Transient (The absolute value of the output change)	$V_{LDO5\sim7}$=2.8V, V_{VSYS}=3.8V, I_{OUT} from 1mA to 400mA in 10us, Ta=25°C		40	80	mv
		$V_{LDO5\sim7}$=2.8V, V_{VSYS}=3.8V, I_{OUT} from 400mA to 1mA in 10us, Ta=25°C		40	80	
$IQ_{LDO=5\sim7_VSYS}$	Quiescent Current	Only LDO5 or LDO6 or LDO7 on, no load. Total current on VSYS		30	55	uA
$IQ_{LDO=5\sim7_VIN}$		Only LDO5 or LDO6 or LDO7 on, no load. Total current on VIN5/VIN6/VIN7		14	30	uA
$I_{Q_OFF_LDO5\sim7}$	VIN5~7 Standby Current	V_{VSYS}=$V_{VIN5\sim7}$=3.8V, V_{RESET_N}=0V or Shutdown by I^2C		0.1	1	uA

Electrical Characteristics (Continued)

(Unless otherwise noted, V_{VIN12}=$V_{LDO1/2}$+0.25V, V_{VSYS}=($V_{LDO1/2}$+1.6V) or 2.7V whichever greater, I_{OUT}=1mA, C_{VIN12}=10μF, C_{VSYS}=C_{VIN34}=C_{VIN5}=C_{VIN6}=C_{VIN7}=1uF, C_{LDO1}=C_{LDO2}=10μF, C_{LDO3}=C_{LDO4}=C_{LDO5}=C_{LDO6}=C_{LDO7}=1μF, C_{VREF}=0.1μF, Ta=-40°C~85°C. Typical values are at. Ta=25 ºC, V_{VSYS}=3.8V; V_{VIN12}=1.3V; V_{VIN34}, V_{VIN5}, V_{VIN6}, V_{VIN7}=3.8V; $V_{LDO1/2}$=1.05V, $V_{LDO3/4/5/6/7}$=2.8V.)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$I_{OUT_LDO5\sim7}$	Output Current		400			mA
$I_{LMT_LDO5\sim7}$	Over Current Limit	Default Ilimit register value, $V_{VIN5/6/7}$=V_{LDOx_VSET}+1V, Ta=25ºC	400	550	900	mA
$I_{SHORT_LDO5\sim7}$	Short Current Limit	Default Ilimit register value, $V_{LDO5\sim7}$=0V, Ta=25ºC	20	45	80	mA
$UVP_{LDO5\sim7}$[10]	OUTPUT Under Voltage Protection	Falling, V_{OUT}=2.8V @V_{VSYS}-V_{OUT}>1.1V	77	80		% $V_{_target}$
		Rising, V_{OUT}=2.8V @V_{VSYS}-V_{OUT}>1.1V		90	93	% $V_{_target}$
$TMR_{LDO5\sim7}$	LDO5~7 Protection Timer	V_{OUT}=2.8V, Time between V_{OUT} forced to 2.2V and INIT going low	50	80	110	us
$PSRR_{_LDO5\sim7}$[6]	Power Supply Rejection Ratio	f=100Hz, $C_{LDO5\sim7}$=1μF, I_{OUT}=20mA, V_{IN} to V_{OUT}, V_{VSYS}=V_{LDOx_VSET}+1V, Ripple 0.4Vp-p, Ta=25°C		90		dB
		f=1kHz, $C_{LDO5\sim7}$=1μF, I_{OUT}=20mA, V_{IN} to V_{OUT}, V_{VSYS}=V_{LDOx_VSET}+1V, Ripple 0.4Vp-p, Ta=25°C	70	90	110	
		f=10kHz, $C_{LDO5\sim7}$=1μF, I_{OUT}=20mA, V_{IN} to V_{OUT}, V_{VSYS}=V_{LDOx_VSET}+1V, Ripple 0.4Vp-p, Ta=25°C		90		
		f=100kHz, $C_{LDO5\sim7}$=1μF, I_{OUT}=20mA, V_{IN} to V_{OUT}, V_{VSYS}=V_{LDOx_VSET}+1V, Ripple 0.4Vp-p, Ta=25°C		60		
		f=1MHz, $C_{LDO5\sim7}$=1μF, I_{OUT}=20mA, V_{IN} to V_{OUT}, V_{VSYS}=V_{LDOx_VSET}+1V, Ripple 0.4Vp-p, Ta=25°C		40		
		f=1kHz, I_{OUT}=20mA, Ta=25°C V_{VSYS} to V_{OUT}, Ripple 0.4Vp-p,		105		
e_N[6]	Output Noise	10Hz to 100kHz, I_{OUT} =30mA, $V_{LDO5\sim7}$=2.8V, V_{VSYS}= $V_{VIN5\sim7}$=3.8V, $C_{LDO5\sim7}$=1μF, Ta=25°C		10	100	μV_{RMS}
$R_{LOW_LDO5\sim7}$	Output resistance of auto discharge at off state	V_{SYS}=$V_{IN5\sim7}$=3.8V, V_{RESET_N}=0V, or Shutdown by I^2C, I_{OUT}=10mA, Ta=25ºC	250	350	450	Ω
$T_{ON_LDO5\sim7}$[6][8]	Output Turn-on Delay Time	From enable to V_{OUT}=95% of V_{OUT}(NOM)		180	300	us

Note (4): Here V_{VINx} means internal circuit can work normal. If V_{VINx}<V_{LDOx}, Output voltage follow V_{VINx} (I_{OUT}=1mA), circuit is safety.

For the LDO1/2, when $I_{OUT_LDO1/2}$>800mA, (V_{VIN12}-$V_{LDO1/2}$) should be less than 0.5V.

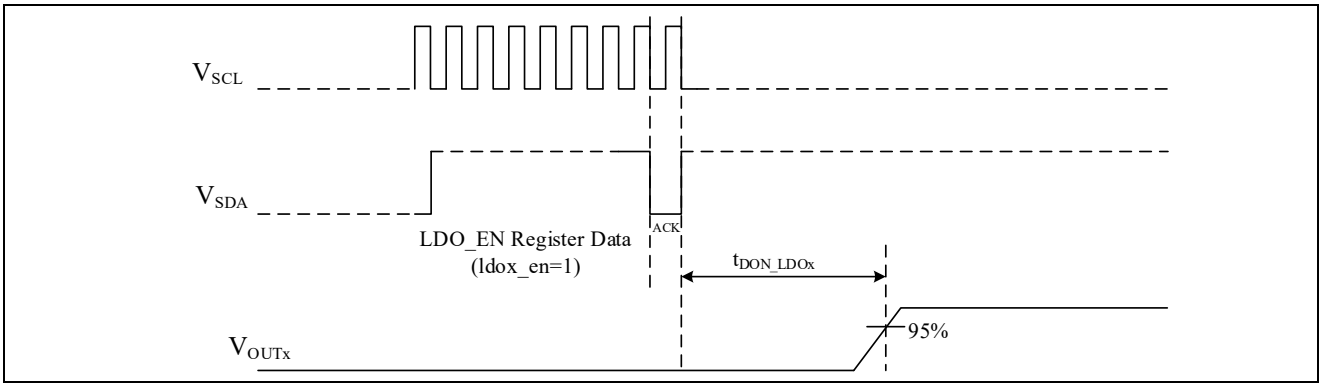
Note (5): Here V_{VSYS}>V_{UVLO_VSYS} means internal control circuit can work normal. If V_{VSYS}<2.7 or V_{VSYS} <$V_{LDO1/2}$+1.6V, some performance parameters cannot be guaranteed.

Note (6): Guaranteed by design and characterization. not a FT item.

Note (7): V_{DROP_LDOx} FT test method: test the V_{LDOx} voltage at V_{LDOx_vset} +$V_{DROPMAX}$ with output current.

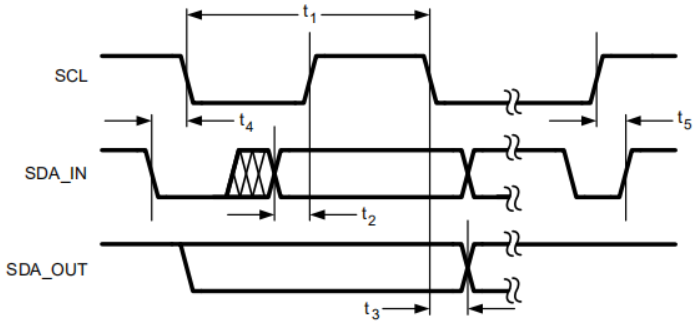
Note (8): T_{ON_LDOx} timing diagram shown as below(x=1~7)

Note (9): Since the power on process of VSYS needs a large current, the BIAS should have a current driving capacity of more than 100mA.



Fast Mode I2C Specification

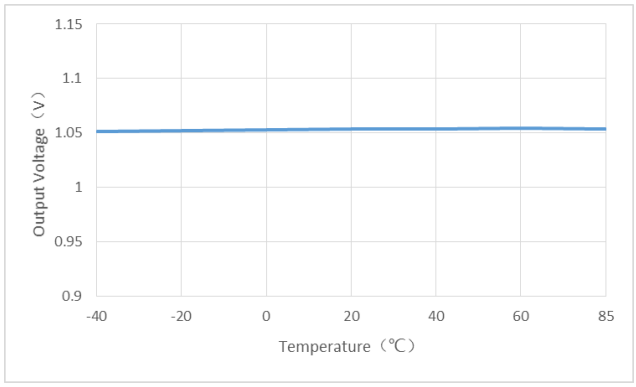
Symbol	Parameters	Min	Max	Unit
t1	SCL clock period, Recommended 50% duty.	0.96		us
t2	Data in set-up time to SCL high	100		ns
t3	Data out stable after SCL low	100		ns
t4	SDA low set-up time to SCL low (start)	100		ns
t5	SDA high hold time after SCL high (stop)	100		ns



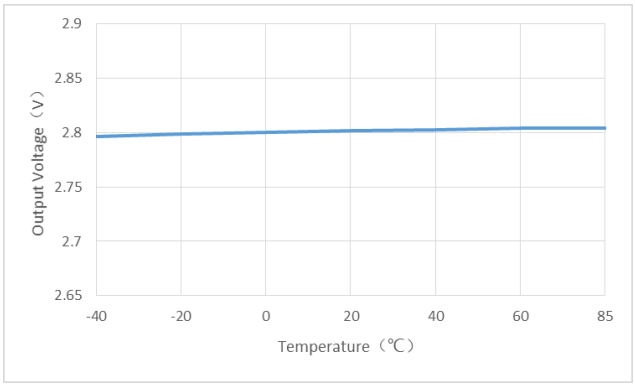
I2C-Compatible Interface Specifications

Typical Characteristics

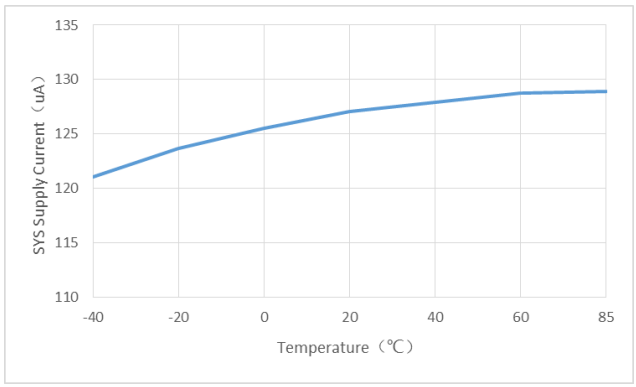
(Unless otherwise noted, V_{VIN12}=$V_{LDO1/2}$+0.25V, V_{VSYS}=($V_{LDO1/2}$+1.6V) or 2.7V whichever greater, I_{OUT}=1mA, C_{VIN12}=10μF, C_{VSYS}=C_{VIN34}=C_{VIN5}=C_{VIN6}=C_{VIN7}=1uF, C_{LDO1}=C_{LDO2}=10μF, C_{LDO3}=C_{LDO4}=C_{LDO5}=C_{LDO6}= C_{LDO7}=1μF, C_{VREF}=0.1μF, Ta=-40°C~85°C. Typical values are at. Ta=25 ºC, V_{VSYS}=3.8V; V_{VIN12}=1.3V; V_{VIN34}, V_{VIN5}, V_{VIN6}, V_{VIN7}=3.8V; $V_{LDO1/2}$=1.05V, $V_{LDO3/4/5/6/7}$=2.8V.)



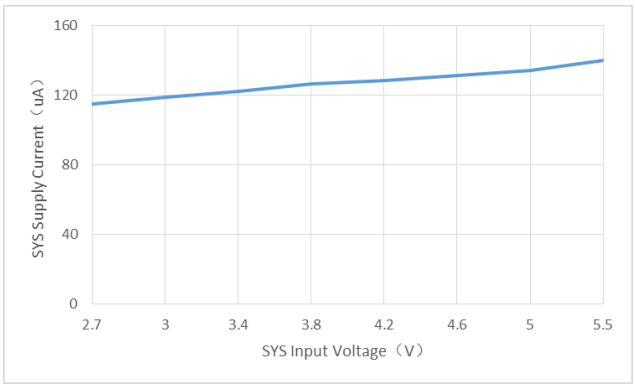
LDO1/2 Output Voltage vs. Temperature



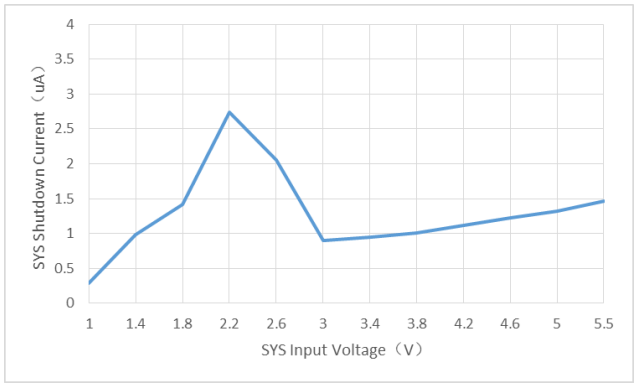
LDO3/4/5/6/7 Output Voltage vs. Temperature



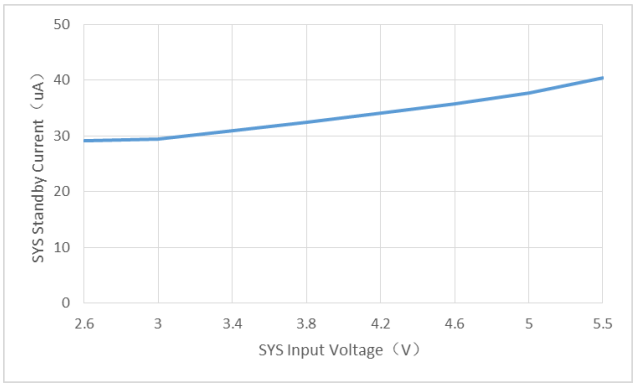
SYS Supply Current vs. Temperature



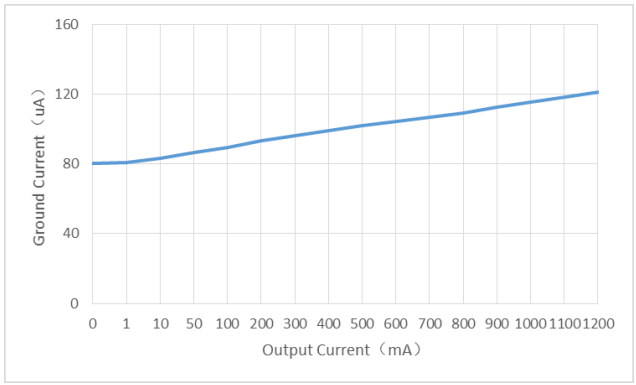
SYS Supply Current vs. SYS Input Voltage



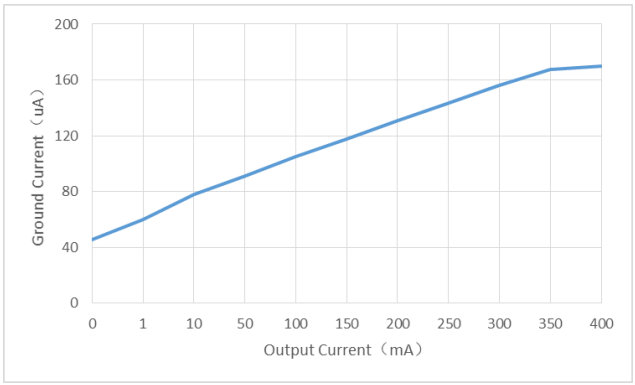
SYS Shutdown Current vs. SYS Input Voltage



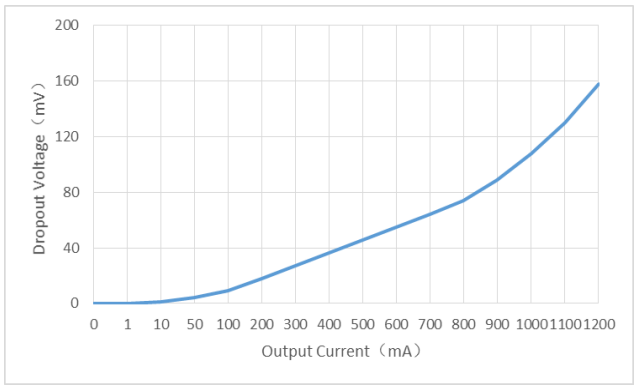
SYS Standby Current vs. SYS Input Voltage



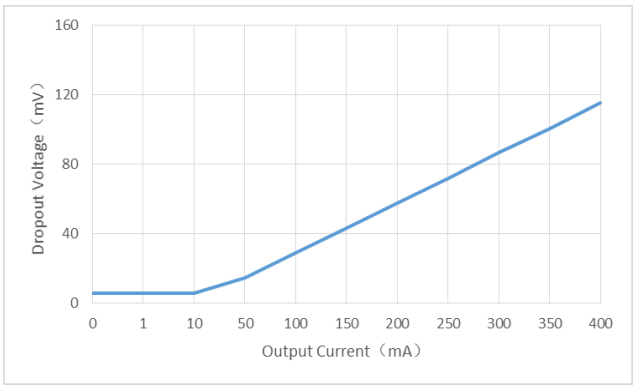
LDO1/2 Ground Current vs. Output Current



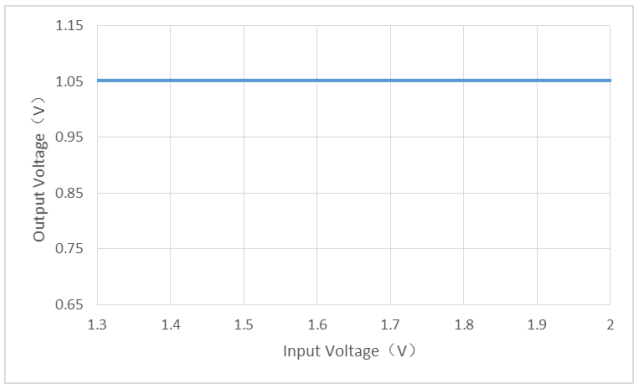
LDO3/4/5/6/7 Ground Current vs. Output Current



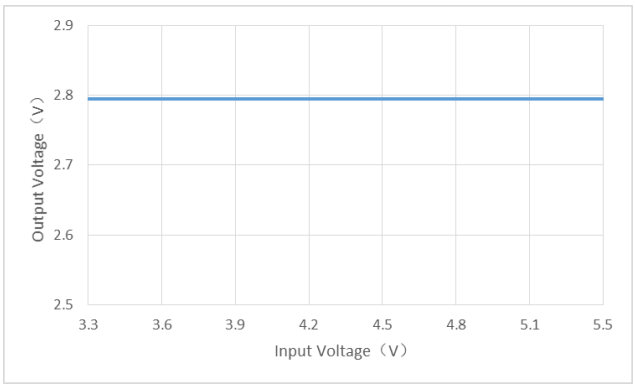
LDO1/2 Dropout Voltage vs. Output Current



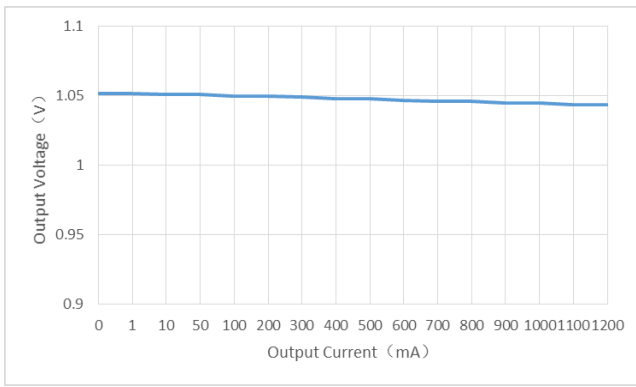
LDO3/4/5/6/7 Dropout Voltage vs. Output Current

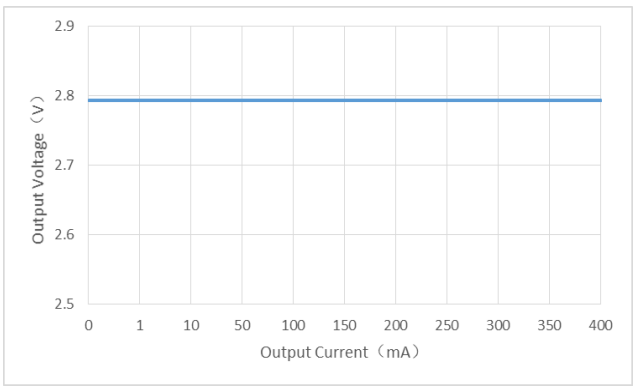


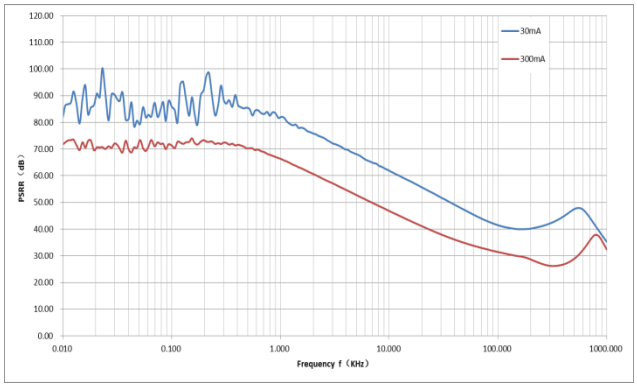
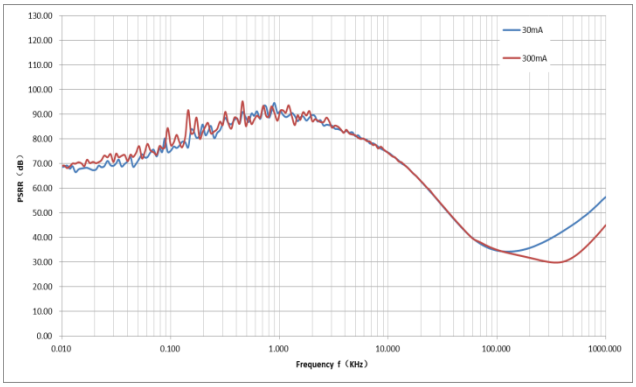
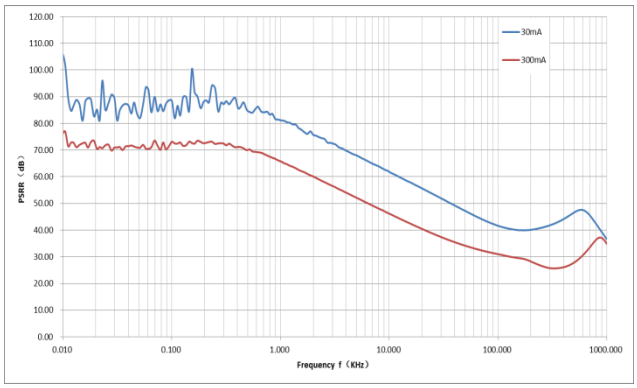
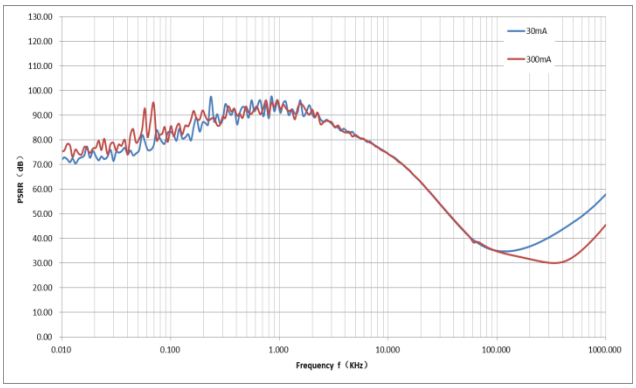
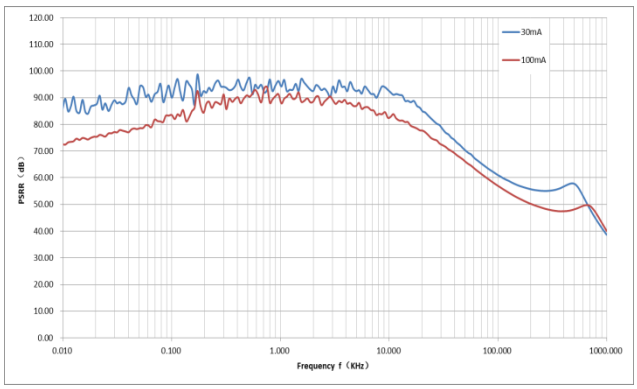
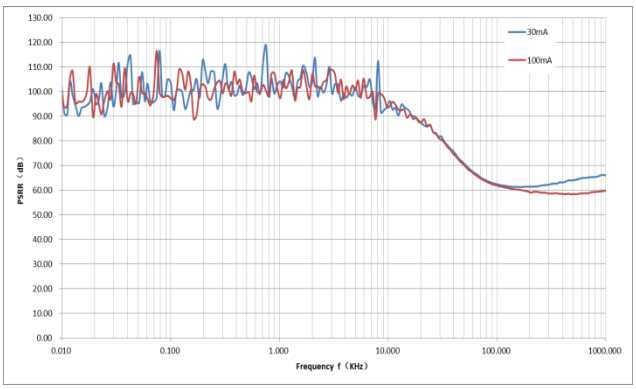
LDO1/2 Output Voltage vs. Input Voltage

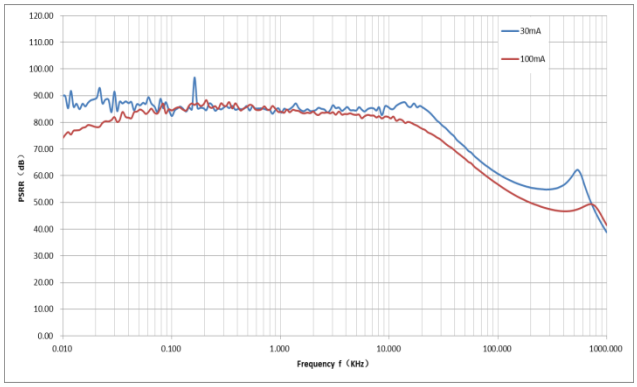


LDO3/4/5/6/7 Output Voltage vs. Input Voltage

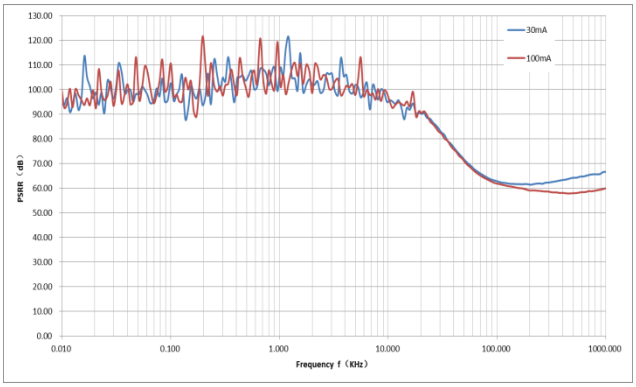




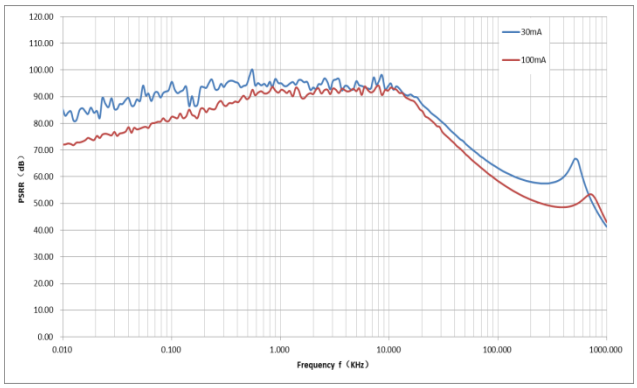
LDO1/2 Output Voltage vs. Output Current	LDO3/4/5/6/7 Output Voltage vs. Output Current
	
LDO1 PSRR-VIN	LDO1 PSRR-SYS
	
LDO2 PSRR-VIN	LDO2 PSRR-SYS
	
LDO3 PSRR-VIN	LDO3 PSRR-SYS



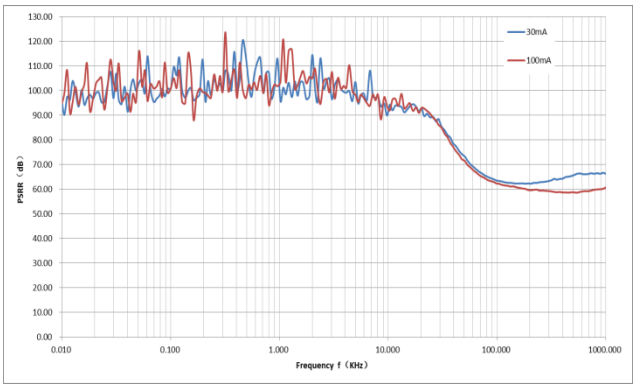
LDO4 PSRR-VIN



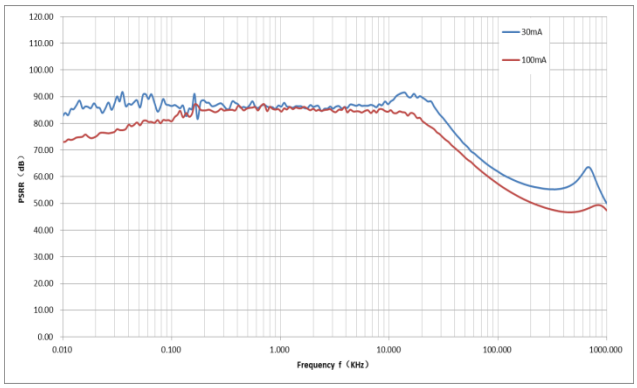
LDO4 PSRR-SYS



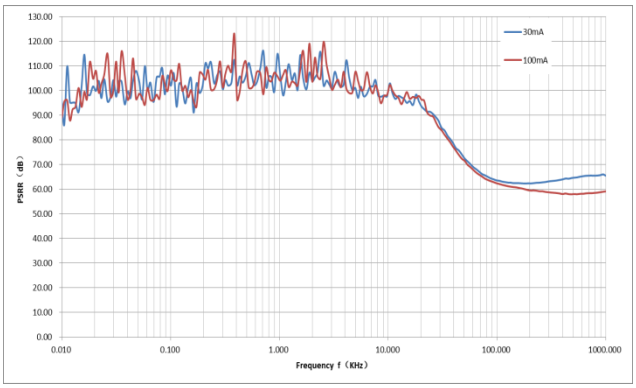
LDO5 PSRR-VIN



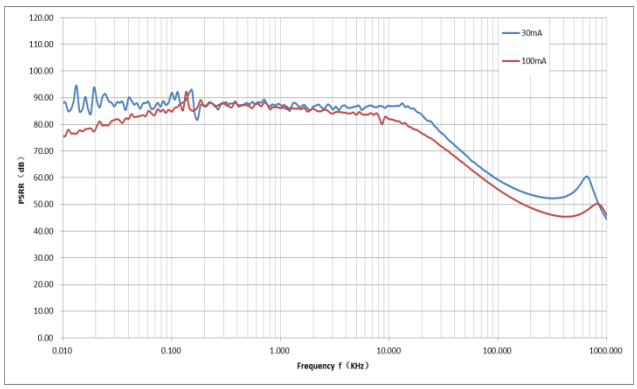
LDO5 PSRR-SYS

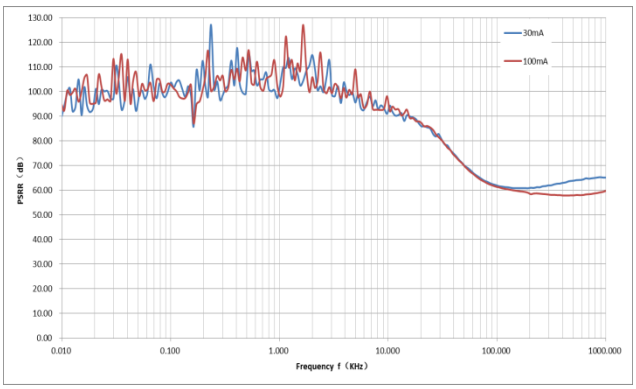


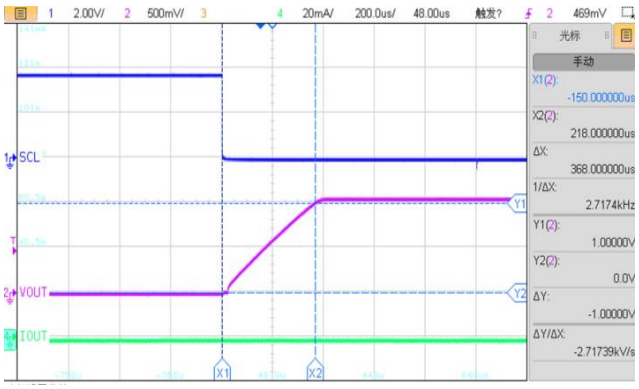
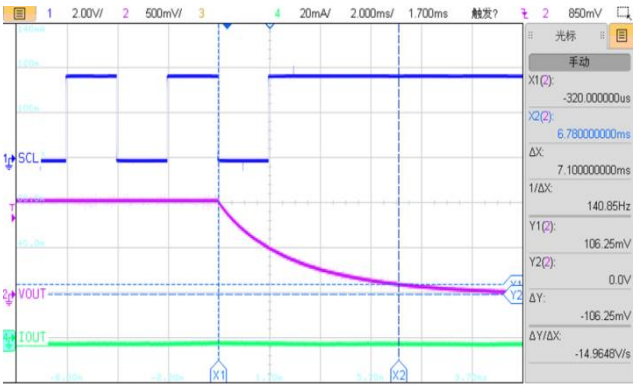
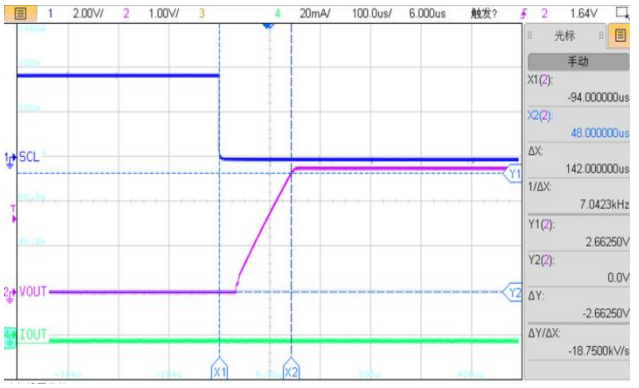
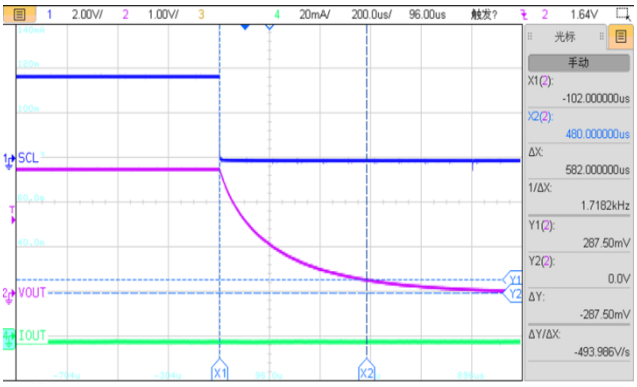
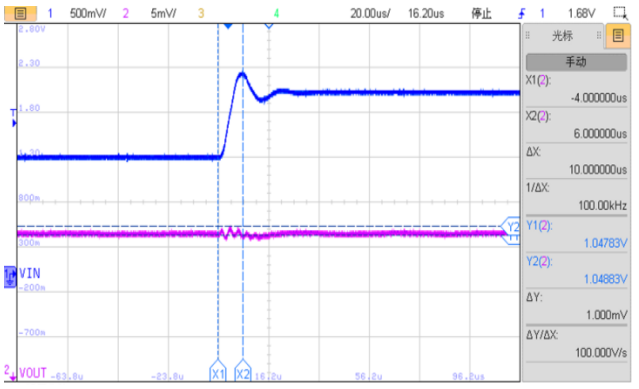
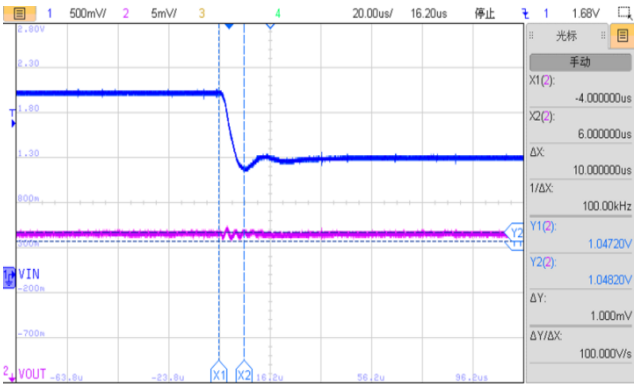
LDO6 PSRR-VIN

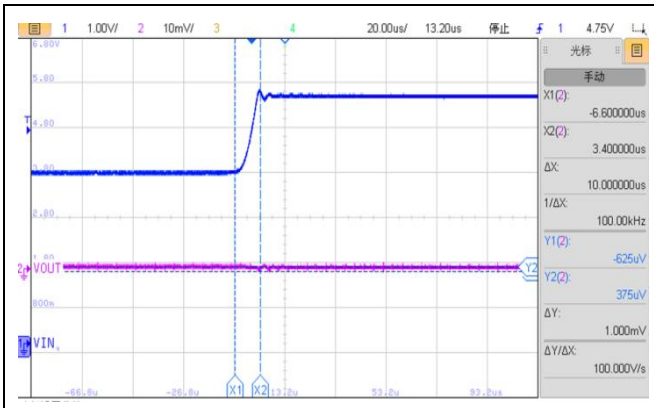


LDO6 PSRR-SYS

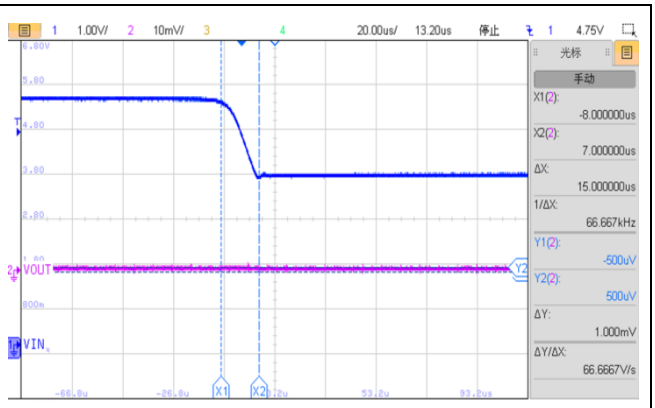




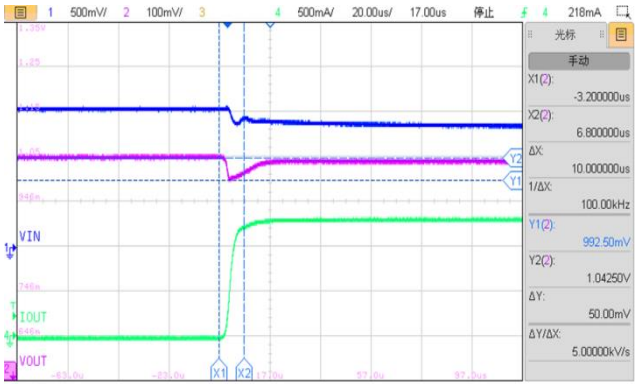
LDO7 PSRR-VIN	LDO7 PSRR-SYS
	
LDO1/2 Ton	LDO1/2 Toff
	
LDO3/4/5/6/7 Ton	LDO3/4/5/6/7 Toff
	
LDO1/2 Line Transient	LDO1/2 Line Transient



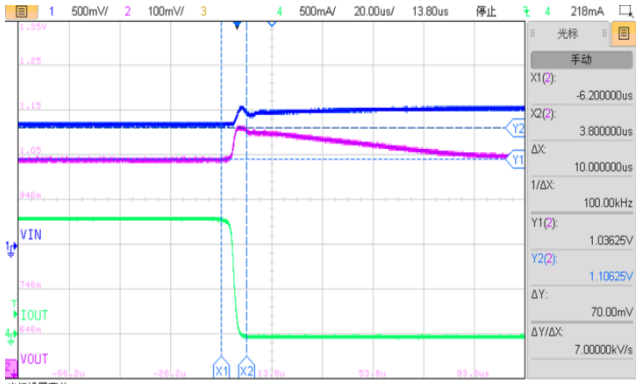
LDO3/4/5/6/7 Line Transient



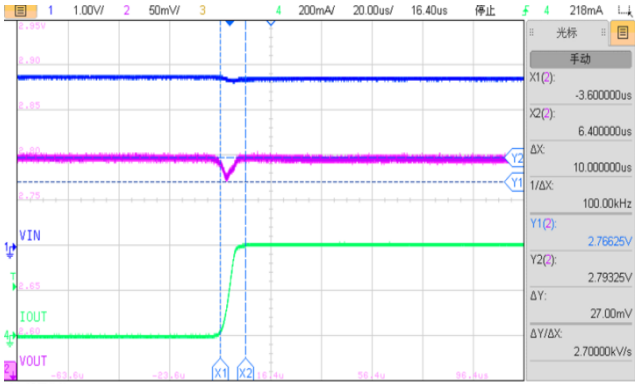
LDO3/4/5/6/7 Line Transient



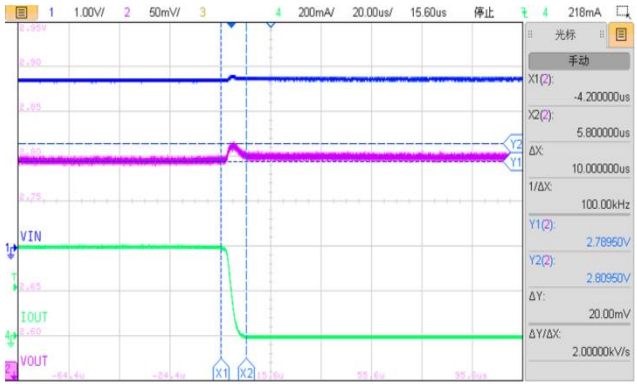
LDO1/2 Load Transient



LDO1/2 Load Transient

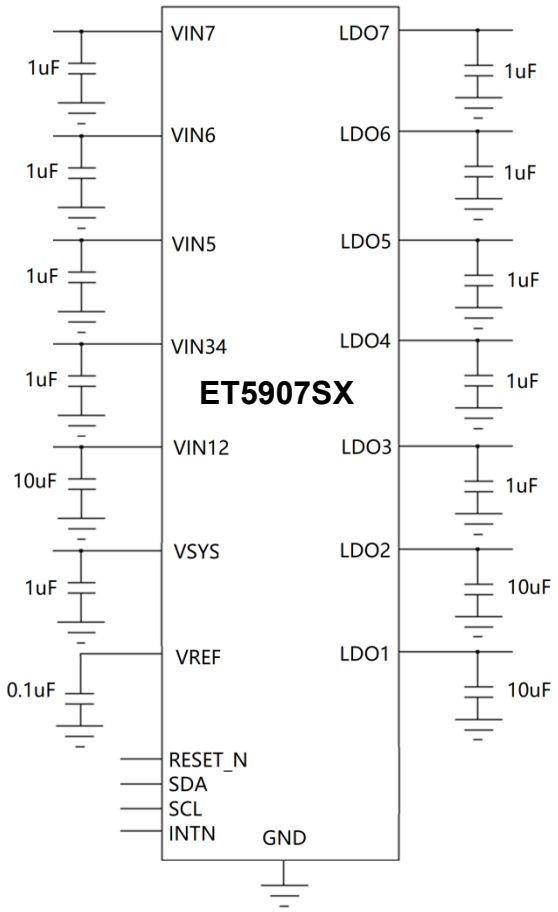


LDO3/4/5/6/7 Load Transient



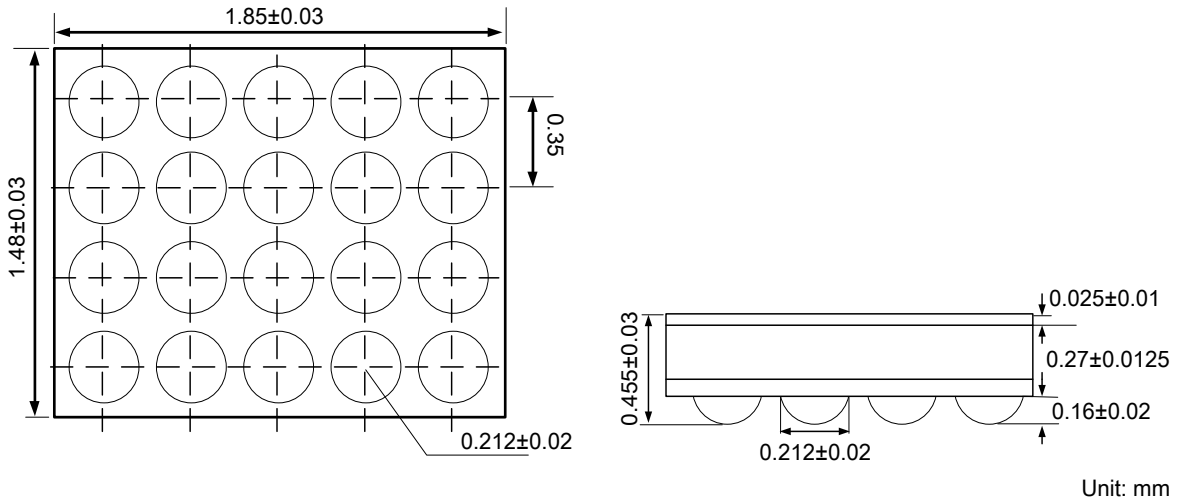
LDO3/4/5/6/7 Load Transient

Application Circuits

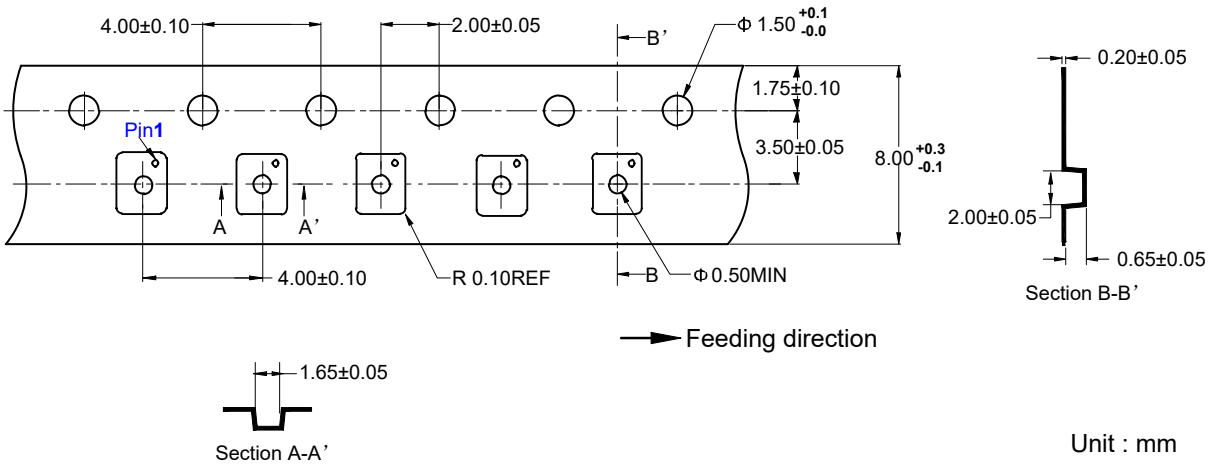


Note: INTN is Open drain output, a resistance is need to connect to DC power supply when use it.

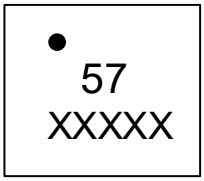
Package Dimension



Tape Information



Marking



57 = Part Number

XXXXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2020-10-22	Original Version	Yang Xiao Xu	Liu Yi Guo	Yang Xiao Xu
1.1	2022-8-4	Update Effective Output Ceramic Capacitor Value	Yang Xiao Xu	Liu Yi Guo	Yang Xiao Xu
1.2	2023-1-6	Update Typeset	Yang Xiao Xu	Liu Yi Guo	Yang Xiao Xu
1.3	2023-5-22	Add more PSRR parameter points	Yang Xiao Xu	Liu Yi Guo	Yang Xiao Xu
1.4	2023-10-23	Add Marking	Yang Xiao Xu	Liu Yi Guo	Yang Xiao Xu
1.5	2024-12-23	Update LDO1~7 AMR	Yang Xiao Xu	Liu Yi Guo	Liu Jia Ying