ET61064Y - Constant Current LED Matrix Driving Circuit

General Description

ET61064Y is a dedicated constant-current LED matrix driver IC, supporting display arrays of up to 8×8 pixels；IThe communication method is the standard I2C communication interface, and it also supports continuous read-write functions. Each pixel supports 256 levels of grayscale brightness adjustment. It is mainly applied in the display driver of household appliances.It is available in QFN20 package option.

Features

- 8 constant current driver channels, max output current 50mA
- Support 1～8 scan application, the maximum application matrix is 8×8, 64 LEDs
- Each LED supports 256 steps brightness adjustment
- I^2C interface, two chip-address can be set
- Oscillation mode: built in RC oscillation（1MHz±10%）
- Built in power on reset circuit
- Built in automatic blanking circuit
- Package: QFN20

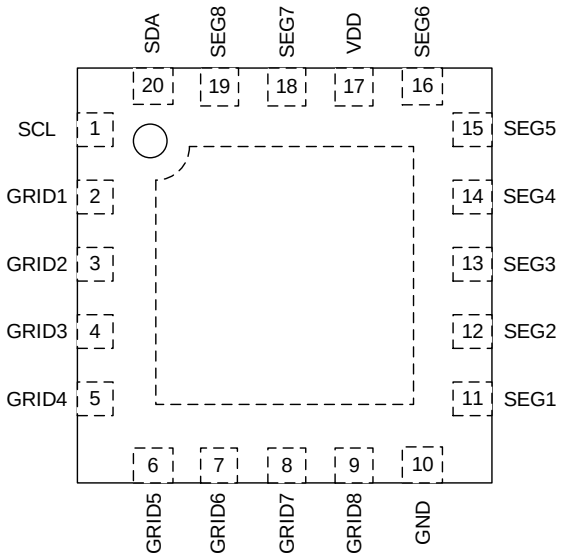
Device Information

Part No.	Package	Packaged form	MSL
ET61064Y	QFN20 (3mm*3mm)	Tape and reel, 3K/Reel	3

Application

- Household appliances, Toy display
- Smart portable devices, Smart audio

Pin Assignments



ET61064Y (QFN20)

Figure 1. Pin Assignments (Top View)

Pin. Function

Pin No.	Name	Function
1	SCL	I^2C clock input
2~9	GRID1~GRID8	Grid output, connected to LED cathode.
10	GND	GND
11~16,18,19	SEG1~SEG8	Segment output, connected to LED anode.
17	VDD	Supply voltage
20	SDA	I^2C data input/output

Block Diagram

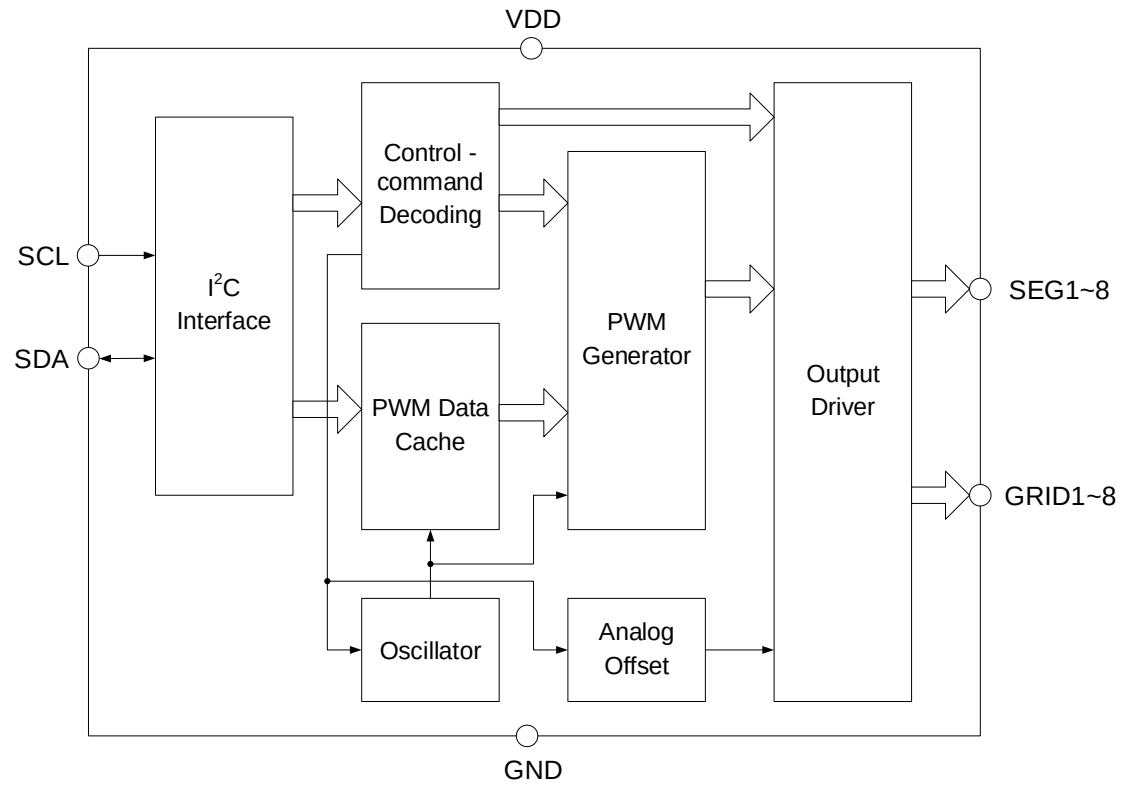


Figure 2. Block Diagram

Functions Description

Serial Port Interface

MCU can transmit data with ET61064Y each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected.

Data Validity

When the SCL signal is HIGH, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

Start (Re-start) and Stop Working Conditions

When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

Byte format

Each byte of data line contains 8 bits, which contains an acknowledge bit. The first data is transmitted MSB.

Acknowledge

During the writing mode, ET61064Y will send a low level response signal with one period width to the SDA port. During the reading mode, ET61064Y will not send response signal and the host will send a high response signal one period width to the SDA.

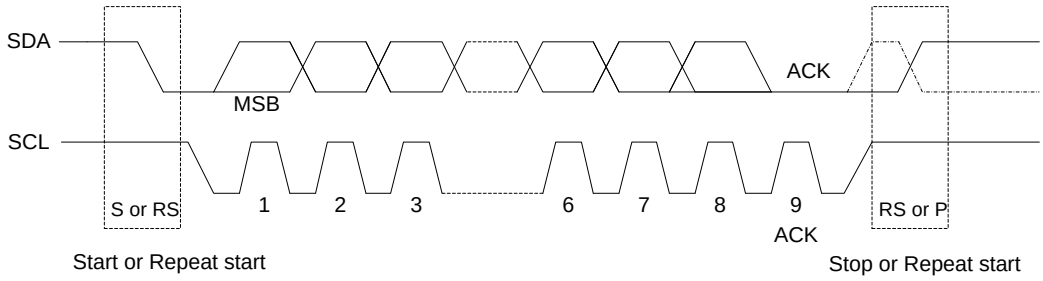


Figure 3. I²C Write Mode

Note：ACK=Acknowledge

MSB=Most Significant Bit

S=Start Conditions RS=Restart Conditions P=Stop Conditions

Fastest Transmission Speed =400KBITS/S

Restart: SDA-level turnover as expressed by the dashed line waveform

I2C Writing Command Register Interface Protocol (continuous)：

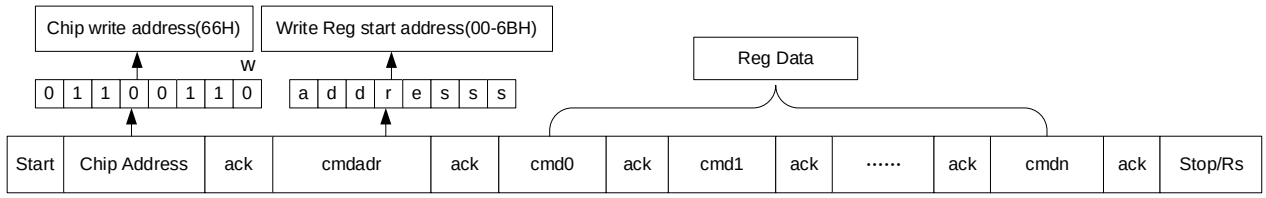


Figure 4. I²C Writing Command Register Protocol (continuous)

- Start = Start Conditions
- Chip Address = Write register address = 0110011+0(w)b
- ack = Acknowledge from ET61064Y
- Write Reg start address byte = cmdadr (REG's 8bit address)
- ack = Acknowledge from ET61064Y
- Command Reg data 0=cmd0(Command data)
- ack = Acknowledge from ET61064Y
- ……
- Command Reg data n=cmdn(Command data)
- ack = Acknowledge from ET61064Y
- Stop/Rs=Stop Condition/Restart Condition

I²C Writing Command Register Interface Protocol (single)：

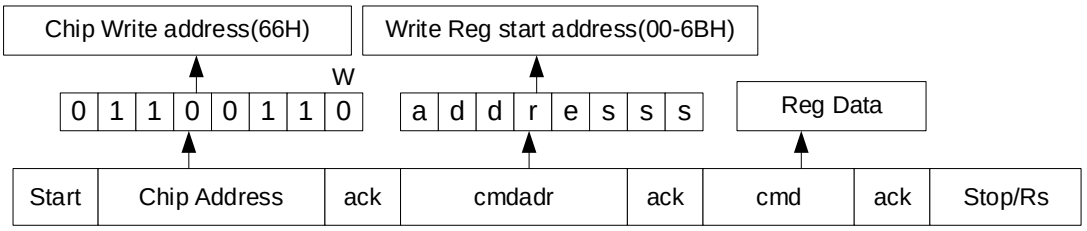


Figure 5. I²C Writing Command Register Protocol (single)

- Start =Start Conditions
- Chip Address = Write register address = 0110011+0(w)b
- ack = Acknowledge from ET61064Y
- Write Reg start address byte = cmdadr(REG's 8bit address)
- ack = Acknowledge from ET61064Y
- Command Reg data =cmd(Command data)
- ack = Acknowledge from ET61064Y
- Stop

I²C Reading Command Register Interface Protocol(continuous):

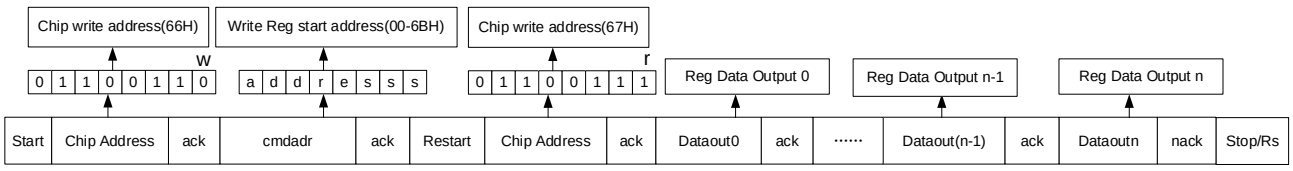


Figure 6. I²C Reading Command Register Interface Protocol(continuous)

- Start =Start Conditions
- Chip Address = Write register address = 0110011+0(w)b
- ack = Acknowledge from ET61064Y
- Write Reg start address byte = cmdadr(REG's 8bit address)
- ack = Acknowledge from ET61064Y
- Restart = Restart condition
- Chip Address = Write register address = 0110011+1(r)b
- ack = Acknowledge from ET61064Y
- Dataout0 = Register data output 0
- ack=Acknowledge from Host
- ……
- Dataoutn = Register data output n
- nack = No ACK

- Stop

I²C Reading Command Register Interface Protocol(single):

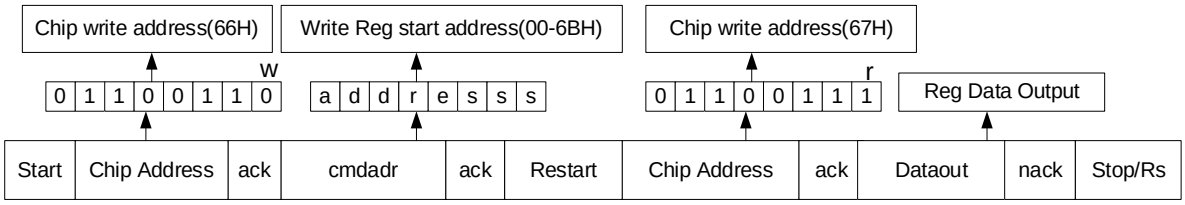


Figure 7. I²C Reading Command Register Interface Protocol(single)

- Start =Start Conditions
- Chip Address = Write register address = 0110011+0(w)b
- ack = Acknowledge from ET61064Y
- Write Reg start address byte = cmdadr(REG's 8bit address)
- ack = Acknowledge from ET61064Y
- Restart = Restart condition
- Chip Address = Write register address = 0110011+1(r)b
- ack = Acknowledge from ET61064Y
- Dataout = Register data output
- Nack = No ACK
- Stop

Register Map

Addr	Description
00H~03H	Control Register
10H~6BH	PWM Data Register

Control Register

Addr: 00h			Control Register 1			
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
00H	7:3	Soft_ Reset	00000	W/R	Write 11011b to reset all register, All other data are invalid	
	2:1	RFU	00	W/R	00	1MHz
					01	2MHz
					10	4MHz
					11	8MHz
	0	Shutdown	0	W/R	0	Shutdown
					1	Operating mode

Addr: 01h			Control Register 2			
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
01H	7：6	RFU	00	-	-	
	5：2	Scan rows	0110	W/R	1000	8 Grids
					0111	7 Grids
					0110	6 Grids (default)
					……	……
					0001	1 Grids
					Note	0000,1001~1111 is invalid
	1：0	Line feed time	00	W/R	00	4 PWM clock cycles
					01	8 PWM clock cycles
					10	12 PWM clock cycles
					11	16 PWM clock cycles

Addr: 02h			Control Register 3			
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
02H	7:4	Chip ID	0110	R	Chip ID	
	3:2	SEG Blanking	01	W/R	SEG Blanking	
					00	Disable blanking
					01	Weak level blanking
					10	Middle level blanking
					11	High level blanking
	1:0	GRID Blanking	00	W/R	GRID Blanking	
					0X	Disable blanking
					10	Weak blanking
					11	High level blanking

Addr: 03h			Control Register 4			
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
03H	7：6	RFU	0	-	-	
	5:1	Brightness	01111	W/R	SEG port output constant current	
					11111	50mA
					11110	48.75mA
					……	……
					01111	30mA (default)
					……	……
					0000	11.25mA
	0	Status control	0	W/R	0	Display off
					1	Display on

Addr: 10~6Bh			PWM Registers			
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
10~6BH	7:0	PWM DATA	00H	W/R	00H	0/255
					……	
					FFH	255/255

Note: After power on, you can configure other registers only after the 00 register is set to operating mode.

When the chip is in the shutdown state, other registers cannot be written.

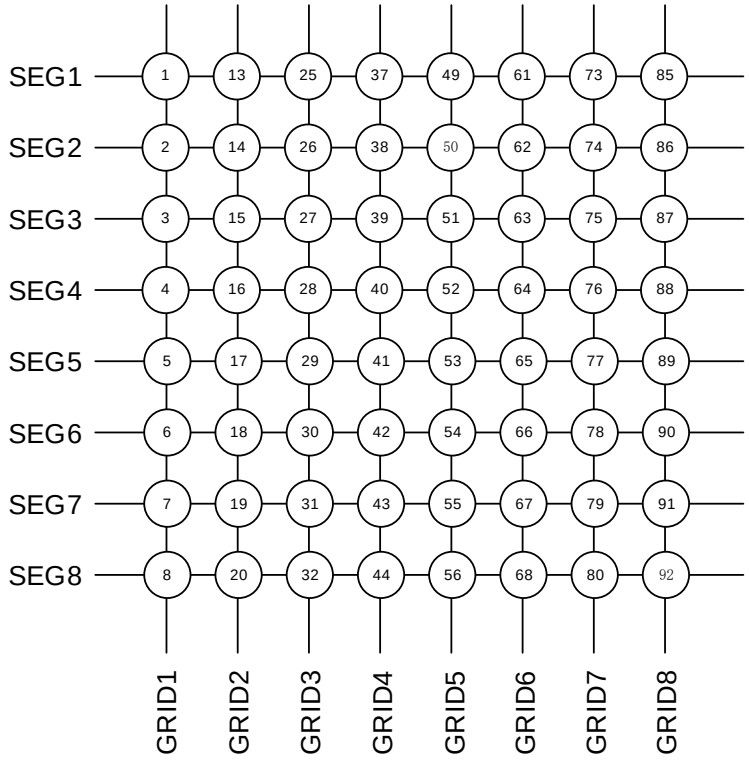


Figure 8. Output Matrix Diagram

PWM Data Register

Addr	Description	Addr	Description	Addr	Description	Addr	Description
10H	LED1PWM	11H	LED2PWM	12H	LED3PWM	13H	LED4PWM
14H	LED5PWM	15H	LED6PWM	16H	LED7PWM	17H	LED8PWM
1CH	LED13PWM	1DH	LED14PWM	1EH	LED15PWM	1FH	LED16PWM
20H	LED17PWM	21H	LED18PWM	22H	LED19PWM	23H	LED20PWM
28H	LED25PWM	29H	LED26PWM	2AH	LED27PWM	2BH	LED28PWM
2CH	LED29PWM	2DH	LED30PWM	2EH	LED31PWM	2FH	LED32PWM
34H	LED37PWM	35H	LED38PWM	36H	LED39PWM	37H	LED40PWM
38H	LED41PWM	39H	LED42PWM	3AH	LED43PWM	3BH	LED44PWM
40H	LED49PWM	41H	LED50PWM	42H	LED51PWM	43H	LED52PWM
44H	LED53PWM	45H	LED54PWM	46H	LED55PWM	47H	LED56PWM

4CH	LED61PWM	4DH	LED62PWM	4EH	LED63PWM	4FH	LED64PWM
50H	LED65PWM	51H	LED66PWM	52H	LED67PWM	53H	LED68PWM
58H	LED73PWM	59H	LED74PWM	5AH	LED75PWM	5BH	LED76PWM
5CH	LED77PWM	5DH	LED78PWM	5EH	LED79PWM	5FH	LED80PWM
64H	LED85PWM	65H	LED86PWM	66H	LED87PWM	67H	LED88PWM
68H	LED89PWM	69H	LED90PWM	6AH	LED91PWM	6BH	LED92PWM

Note: Each address has 8bits of data corresponding to the PWM order of that point (256 steps).

The default value for each set of registers is 00H.

Display cycle

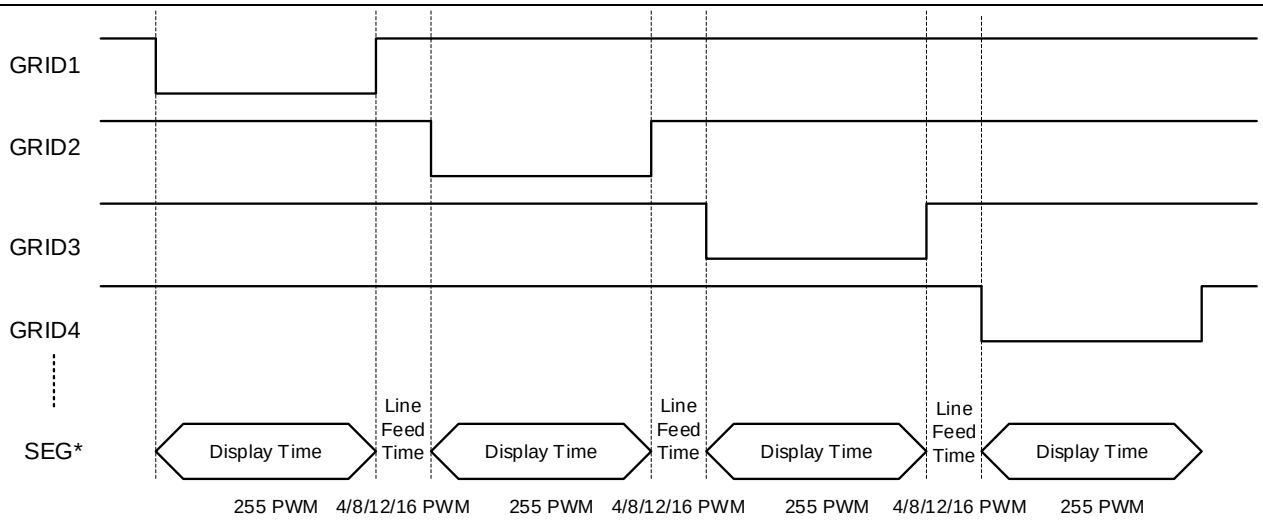


Figure 9. Display Cycle: Scan line × (4/8/12/16 Line feed time+255 steps PWM time)

Absolute Maximum Ratings

(Unless otherwise noted ,T_A=25°C)

Symbol	Characteristic	Rating	Unit
V_{DD}	Supply voltage	-0.5~6.0	V
V_I	Input Voltage	-0.5~V_{DD}+0.5	V
I_{O1}	LED SEG drive output current	-55	mA
I_{O2}	LED GRID drive output current	660	mA
P_D	Power Dissipation	450	mW
T_J	Junction Temperature	-40～150	°C
T_{STG}	Storing Temperature	-65～150	°C
ESD	HBM	±2	KV
	CDM	±1	KV

Recommended Operating Conditions

Symbol	Characteristic	Min	Typ	Max	Unit
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{IH}	Logic high level	0.6V_{DD}	—	V_{DD}	V
V_{IL}	Logic low level	0	—	0.25V_{DD}	*V*
T_A	Operating Temperature	-40		+85	°C

Electrical Characteristics

(Unless otherwise noted, V_{DD}=5V ,T_A=25°C)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage			5.0		V
V_{IH}	Logic high level	SCL, SDA	0.6*V_{DD}		V_{DD}	V
V_{IL}	Logic low level	SCL, SDA	0		0.25*V_{DD}	V
I_I	Input current	SDA, SCL: V_I=V_{DD}			±1	μA
I_{OH}	LED SEG drive output current	Default set is 30mA，SEGn, V_O=V_{DD} -1V	-27	-30	-33	mA
I_{OL}	LED GRID drive output current	GRIDn, V_O=0.5V	600			mA
I_{DD_DYN}	Dynamic current Dissipation	No load, Display off		3		mA
V_{RST}	Reset voltage			2.3		V
I_{SD}	Shutdown current			2	8	μA
Switching Characteristics						
T_{TZH}	SEGn Rising Time	C_L=300pF, R_L=1K			0.5	μs
T_{THZ}	GRIDn Falling Time	C_L=300pF			120	μs
C_I	Input capacitance	SDA , SCL			15	pF

I²C Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCL}	SCL Clock Frequency	0	-	400	KHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	1.3	-	-	μs
$t_{HD:STA}$	Hold Time(Repeated) START Condition	0.6	-	-	μs
t_{LOW}	Low Period of SCL Clock	1.3	-	-	μs
t_{HIGH}	HIGH Period of SCL Clock	0.6	-	-	μs
$t_{SU:STA}$	Setup Time for a Repeated START Condition	0.6	-	-	μs
$t_{HD:DAT}$	Data Hold Time	0.1	-	-	μs
$t_{SU:DAT}$	Data Setup Time	100	-	-	ns
t_R	Data Hold Time2	-	20+0.1Cb[(1)]	300	ns
t_F	Data Hold Time2	-	20+0.1Cb[(1)]	300	ns
$t_{SU:STO}$	Setup Time for STOP Condition	0.6	-	-	μs

Note: Cb=total capacitance of one bus line in PF unit.

I²C Timing Waveform

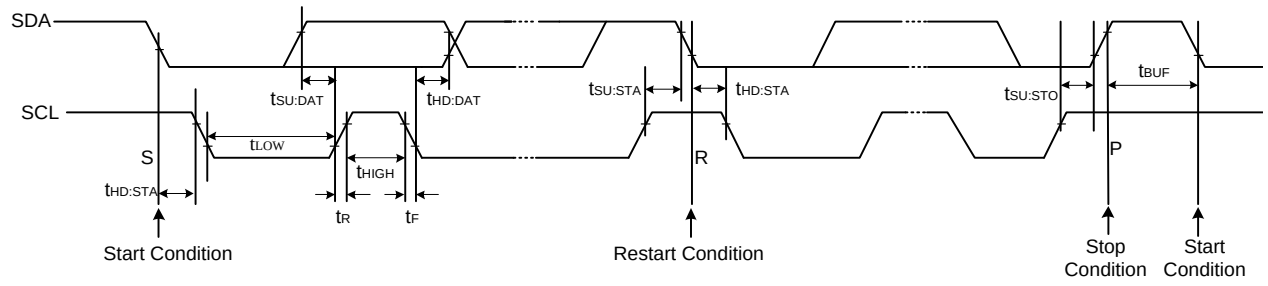


Figure 10. Definition of Timing for I²C Bus

Application circuit

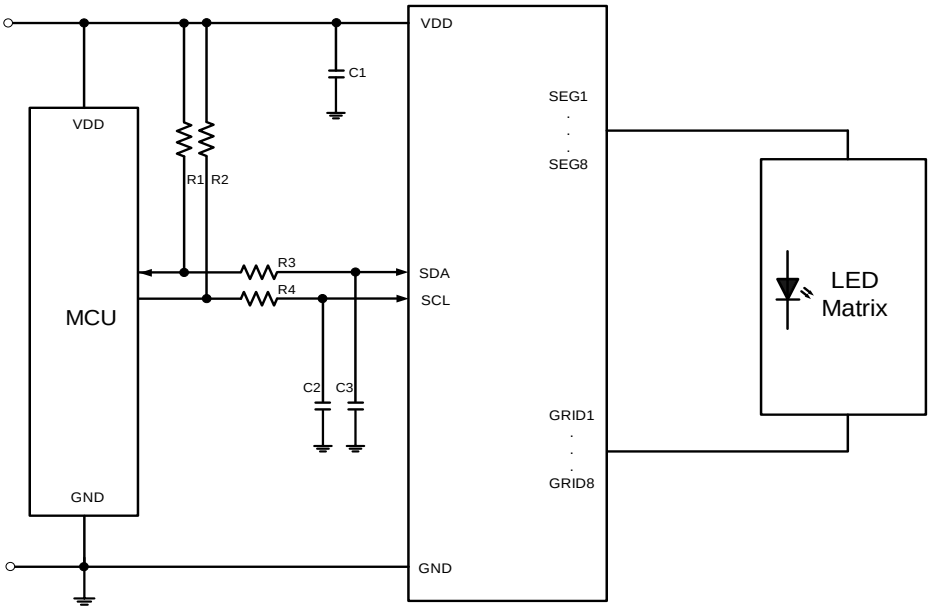


Figure 11. 8×8 LED Matrix Display Application Circuit

Note：This application circuit is only for reference.

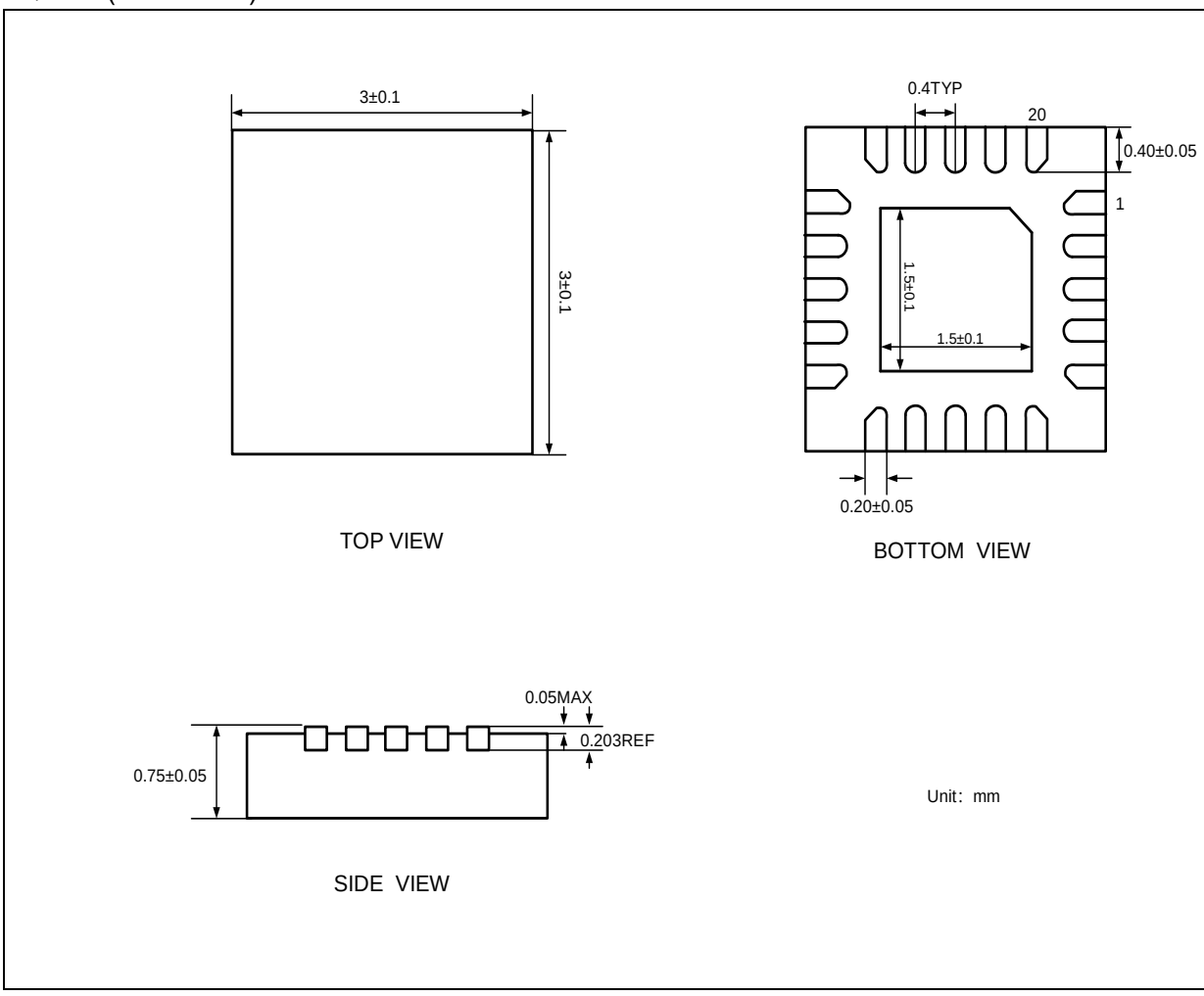
1: The filter capacitor C1 ≥ 1uF and placed as close as possible to VDD;

2: Communication filtering network values recommendation: R1~R2 = 4.7kΩ, R3~R4 = 100Ω, C2~C3 = 100pF;

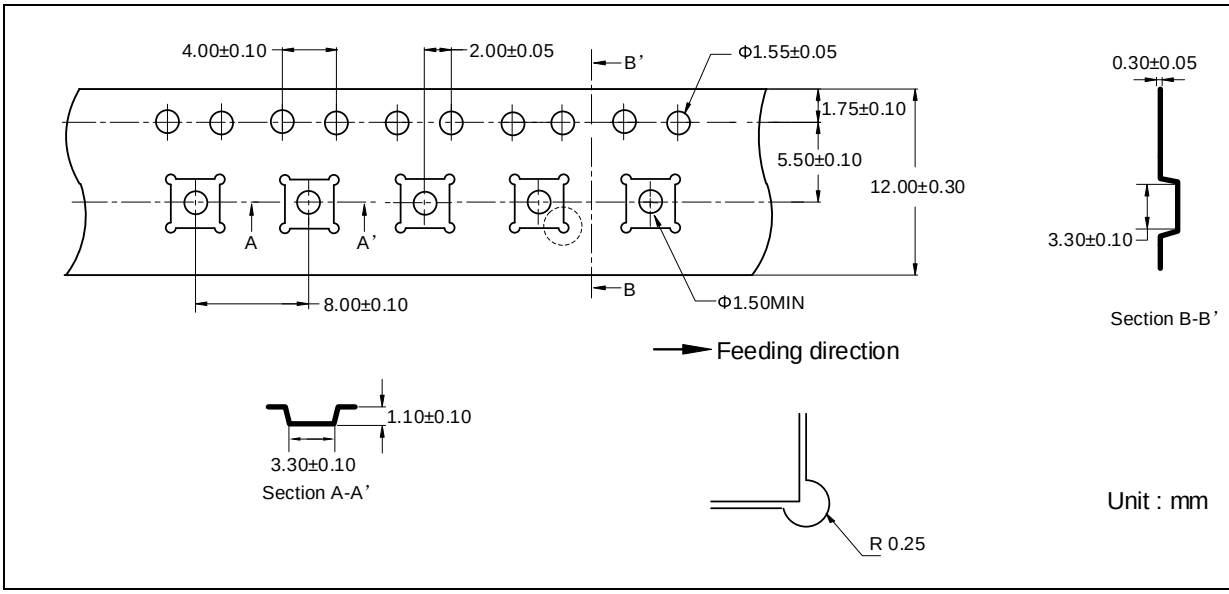
3: The capacitance and resistance values of the filtering network at the communication port should be placed as close as possible to ET61064Y. The values of the filtering network's capacitance and resistance can be adjusted according to the actual anti-interference requirements and verification results.

Package

QFN20(3mm*3mm)

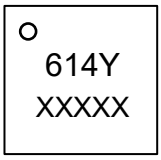


Tape Information



Marking

ET61064Y



XXXXX=Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2026-03-12	Original Version	Wu Yu Chen	Li Chen Xuan	Shi Bo