Low-Power Configurable Multiple Function Gate

General Description

The ET74AHC1G58 is a configurable multiple function gate with Schmitt trigger inputs. The device can be configured as any of the following logic functions MUX, AND, OR, NAND, NOR, inverter and buffer; using the 3-bit input. All inputs can be connected to V_{CC} or GND.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in mixed 3.3V and 5V environments.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging back-flow current through the device when it is powered down.

Features

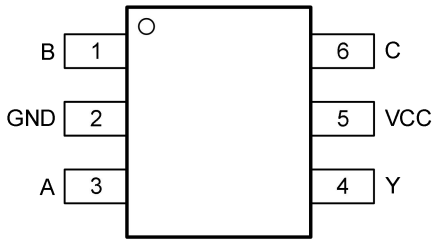
- Designed for 2V to 5.5V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 5.5V
- ±8mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- These Devices are Pb-Free RoHS Compliant
- ESD Protection Complies with JESD22 Standard
  -- HBM: ±4000V Pass (JEDEC JS-001)
  -- CDM: ±1000V Pass (JEDEC JS-002)
- Latch-up Performance Exceeds ±100mA per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET74AHC1G58	SC70-6 (1.3mm × 2.1mm)	Tape and Reel, 3K/Reel	1
ET74AHC1G58T	SOT23-6 (1.6mm × 2.9mm)	Tape and Reel, 3K/Reel	3

Applications

- Active Noise Cancellation (ANC)
- Bar-code Scanners
- Blood Pressure Monitors
- CPAP Machines
- Cable Solutions
- Embedded PCs
- Field Transmitter: Temperature or Pressure Sensors
- HVAC: Heating, Ventilating and Air Conditioning
- TVs: High-Definition (HDTV), LCD and Digital
- Video Communications Systems

Pin Configuration



SC70-6/SOT23-6

Figure1. Pin Configuration

Pin Function

SC70-6/SOT23-6

Pin No.	Pin Name	Function
1	B	Input B
2	GND	Ground
3	A	Input A
4	Y	Output Y
5	VCC	Supply Voltage
6	C	Input C

Block Diagram

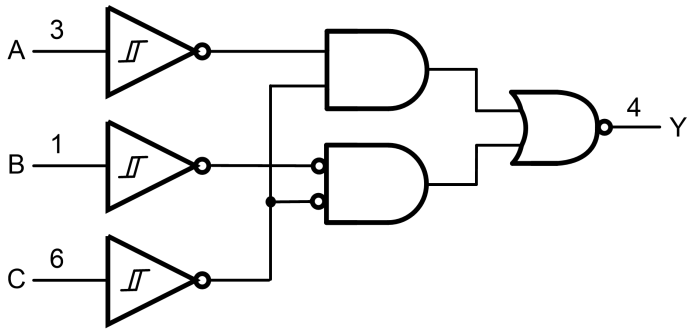


Figure2. Logic Symbol

Functional Table

Input			Output
C	**B**	**A**	**Y**
L	L	L	L
L	L	H	H
L	H	L	L
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	L
H	H	H	L

H = HIGH voltage level; L = LOW voltage level.

Function Selection Table

Logic function	Figure
2-input NAND	See Figure3
2-input NAND with both Inputs Inverted	See Figure6
2-input AND with Inverted Input	See Figure4 and Figure5
2-input NOR with Inverted Input	See Figure4 and Figure5
2-input OR	See Figure6
2-input OR with both Inputs Inverted	See Figure3
2-input XOR	See Figure7
Buffer	See Figure8
Inverter	See Figure9

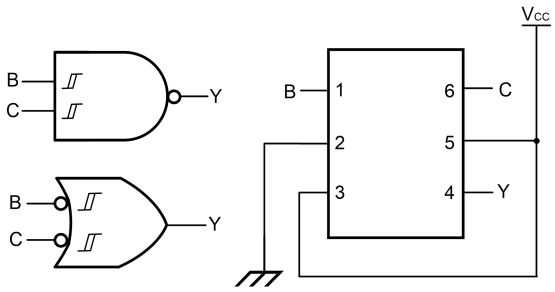


Figure3. 2-input NAND gate or
2-input OR gate with both inputs inverted

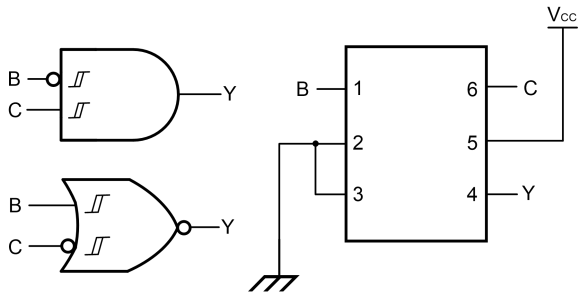


Figure4. 2-input AND gate with input B inverted or
2-input NOR gate with inverted C input

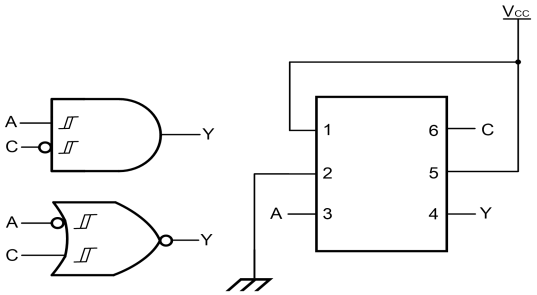


Figure5. 2-input AND gate with input C inverted or
2-input NOR gate with inverted A input

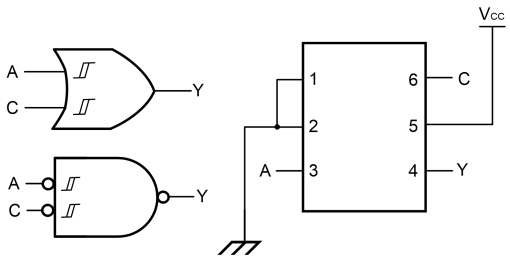


Figure6. 2-input OR gate or
2-input NAND gate with both inputs inverted

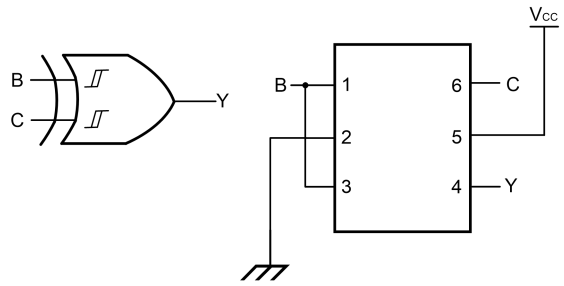


Figure7. 2-input XOR gate

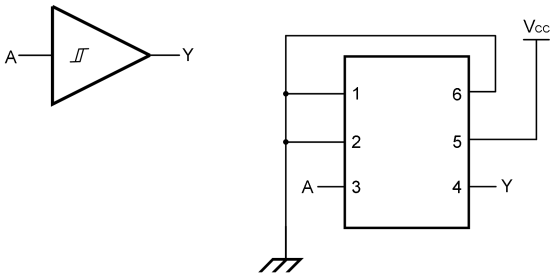


Figure8. Buffer

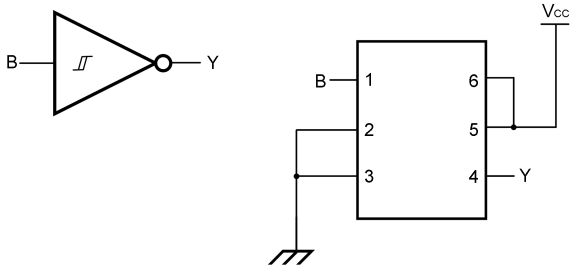


Figure9. Inverter

Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage (VCC Pin)		-0.5 to 7.0	V
V_I	DC Input Voltage (1)		-0.5 ≤ V_I ≤ 7.0	V
V_O	DC Output Voltage Output in Higher or Low State		-0.5 to 7.0	V
I_{IK}	DC Input Diode Current, V_I < GND		-50	mA
I_{OK}	DC Output Diode Current, V_O < GND, V_O > V_{CC}		±50	mA
I_O	DC Output Sink Current		±50	mA
I_{CC}	DC Supply Current per Supply Pin		100	mA
I_{GND}	DC Ground Current per Supply Pin		-100	mA
T_{STG}	Storage Temperature Range		-65 to 150	°C
T_L	Lead Temperature, Soldering 10 Seconds		260	°C
T_J	Max Junction Temperature		150	°C
V_{ESD}	ESD Classification	Human Body Model (2)	±4000	V
		Charged Device Model (3)	±1000	
I_{LU}	Max Latch Up Current Above V_{CC} and GND at 125°C (4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch up Current Maximum Rating tested per JEDEC JESD78F.

Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
$R_{\theta JA}$	SC70-6	Thermal Characteristics, Thermal Resistance, Junction-to-air	280	°C/W
	SOT23-6		180	
P_D	SC70-6	Power Dissipation in Still Air at 85°C	230	mW
	SOT23-6		360	

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage Operating	2	5.5	V
V_I	DC Input Voltage	0	V_{CC}	V
V_O	DC Output Voltage (High or Low State)	0	V_{CC}	V
T_A	Operating Temperature Range	-40	125	°C

Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameters	Conditions	V_{CC}(V)	T_A = 25°C			-40°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V_{OL}	LOW-Level Output Voltage	V_I = V_{T+} or V_{T-}							
		I_{OL} = 100μA	2			0.1		0.1	V
		I_{OL} = 4mA	3			0.36		0.55	V
		I_{OL} = 8mA	4.5			0.36		0.55	V
V_{OH}	HIGH-Level Output Voltage	V_I = V_{T+} or V_{T-}							
		I_{OH} = -100μA	2	V_{CC} - 0.1	V_{CC}		V_{CC} - 0.1		V
		I_{OH} = -4mA	3	2.58			2.4		V
		I_{OH} = -8mA	4.5	3.54			3.7		V
I_I	Input Leakage Current	V_I = 5.5V or GND	0~5.5		±0.1	±1		±1	μA
I_{OFF}	Power-Off Leakage Current	V_I = 5.5V or V_O = 5.5V	0		±0.1	±2		±2	μA
I_{CC}	Supply Current	V_I = 5.5V or GND; I_O = 0mA	5.5		0.1	4		4	μA

Electrical Characteristics(Continued)

AC Electrical Characteristics

Symbol	Parameter	Condition	V_{CC}(V)	T_A = 25°C			-40°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
t_{PHL}, t_{PLH}	Propagation Delay (Figure 10 and 11)	C_L = 15pF	3~3.6		4.3	8.4	1	9.5	ns
		C_L = 50pF	3~3.6		4.8	9.3	1	10.5	
		C_L = 15pF	4.5~5.5		3.8	7.3	1	8.1	
		C_L = 50pF	4.5~5.5		4.2	8.2	1	9.5	

Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.5V, V_I = 0V or V_{CC}	3.8	pF
C_{PD}	Power Dissipation Capacitance (5)	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	10	pF

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

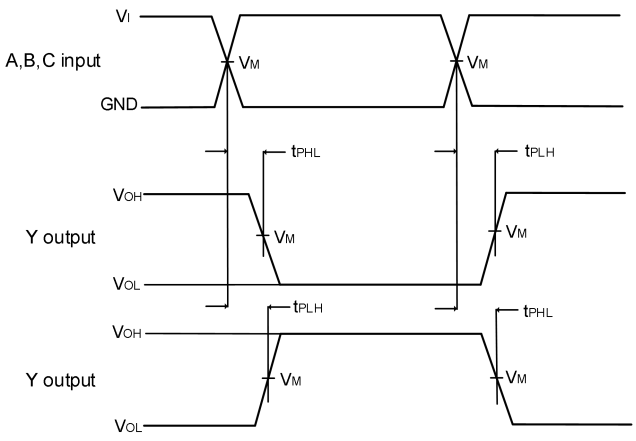
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

Test Waveform



Measurement points are given in Table1.

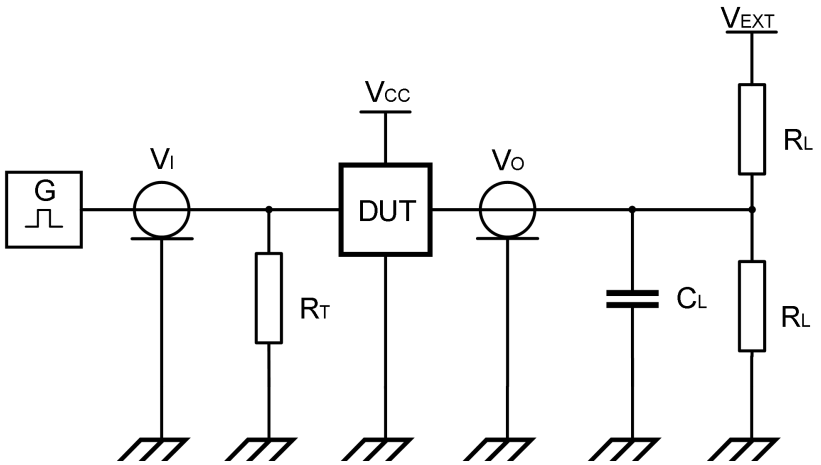
V_{OL} and V_{OH} is typical output voltage levels that occur with the output load.

Figure10. Input A, B, C to Output xY Propagation Delay Times

Table1. Measurement Points

Supply Voltage	Input	Output
V_{CC}	V_M	V_M
3.0V to 3.6V	0.5 × V_{CC}	0.5 × V_{CC}
4.5V to 5.5V	0.5 × V_{CC}	0.5 × V_{CC}

Test Circuit



Measurement points are given in Table2.

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Figure11. Test Circuit for Measuring Switching Times

Table2. Test Data

Supply Voltage	Input		Load		V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}
3.0V to 3.6V	V_{CC}	3.0ns	15pF, 50pF	1kΩ	OPEN
4.5V to 5.5V	V_{CC}	3.0ns	15pF, 50pF	1kΩ	OPEN

Electrical Characteristics(Continued)

Transfer Characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0V).

Symbol	Parameters	Conditions	T_A =25°C			-40°C ≤ T_A ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	
V_{T+}	Positive-going Threshold Voltage	See Figure12, 13, 14, 15						
		V_{CC} = 2.0V	0.85		1.45	0.75	1.4	V
		V_{CC} = 2.3V	1.05		1.75	0.95	1.7	V
		V_{CC} = 3.0V	1.4		2.15	1.3	2.1	V
		V_{CC} = 4.5V	2.0		2.95	1.9	2.9	V
		V_{CC} = 5.5V	2.4		3.35	2.3	3.3	V
V_{T-}	Negative-going Threshold Voltage	See Figure12, 13, 14, 15						
		V_{CC} = 2.0V	0.4		0.8	0.4	0.83	V
		V_{CC} = 2.3V	0.58		1	0.58	1.03	V
		V_{CC} = 3.0V	0.8		1.3	0.8	1.33	V
		V_{CC} = 4.5V	1.21		1.9	1.21	1.93	V
		V_{CC} = 5.5V	1.5		2.34	1.5	2.36	V
V_H	Hysteresis Voltage	See Figure12, 13, 14, 15						
		V_{CC} = 2.0V	0.3		0.95	0.25	0.95	V
		V_{CC} = 2.3V	0.4		0.97	0.33	0.97	V
		V_{CC} = 3.0V	0.5		1.05	0.44	1.05	V
		V_{CC} = 4.5V	0.6		1.3	0.54	1.3	V
		V_{CC} = 5.5V	0.7		1.55	0.64	1.55	V

Wave-forms Transfer Characteristics

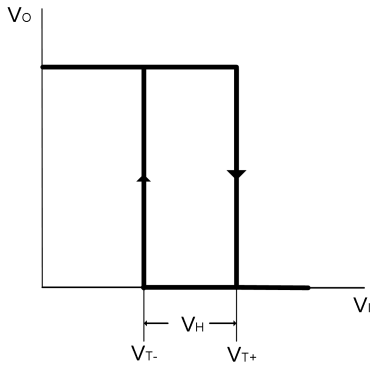
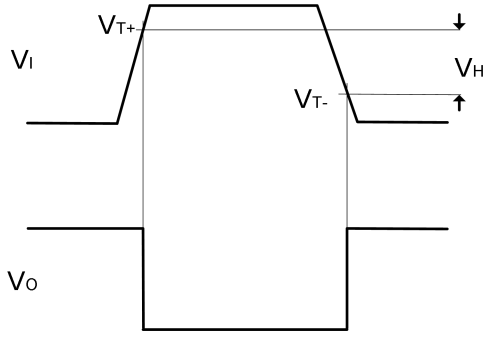


Figure12. Transfer characteristic



V_{T+} and V_{T-} limits are at 70% and 20%

Figure13. Definition of V_{T+} , V_{T-} and V_H

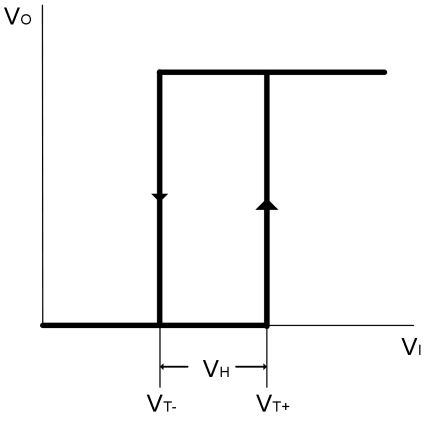
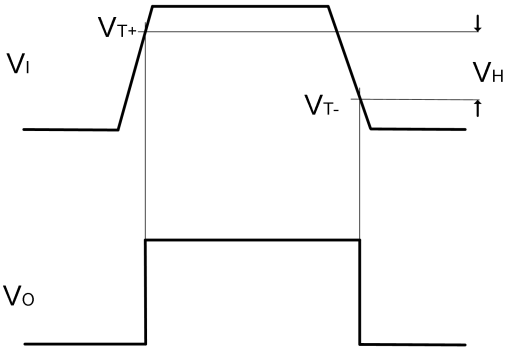


Figure14. Transfer characteristic



V_{T+} and V_{T-} limits are at 70% and 20%

Figure15. Definition of V_{T+} , V_{T-} and V_H

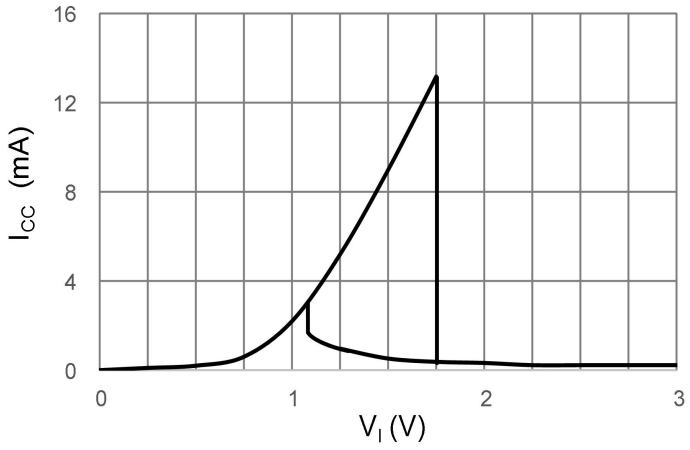


Figure16. Typical ET74AHC1G58 transfer characteristic; V_{CC} = 3.0V

Application Circuits

This application shows the ET74AHC1G58 configured as an NOR gate with an inverted input. This particular configuration is helpful for dual sensor or switch applications where one of the inputs is normally closed or a logic high 1. Normally this application would require two external gates, but because the ET74AHC1G58 can be configured to meet this function the application can be implemented with a single chip solution.

This application circuit is for reference only.

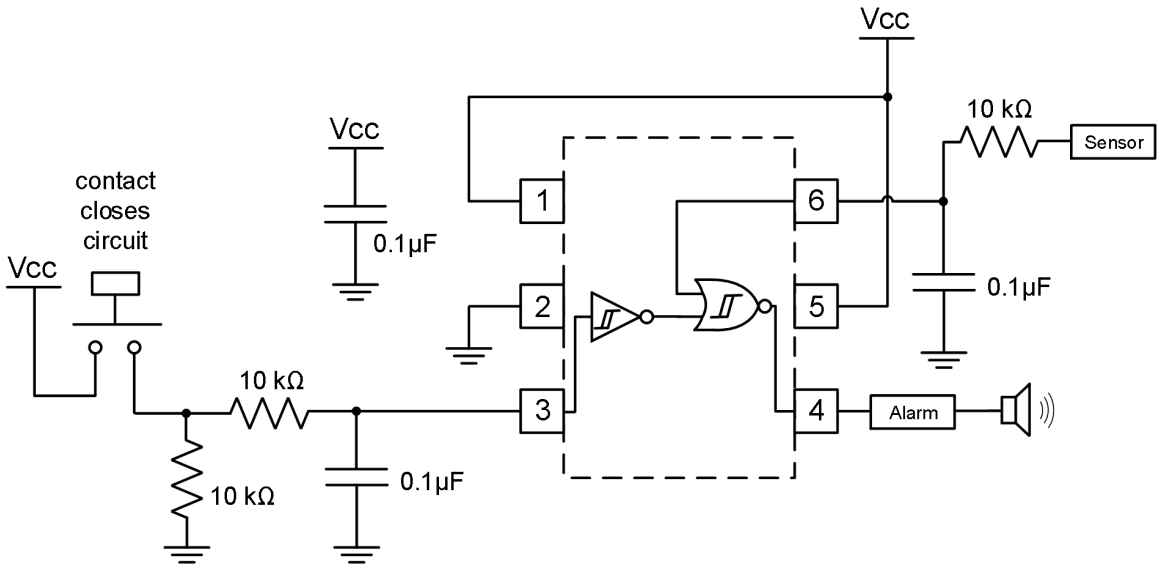
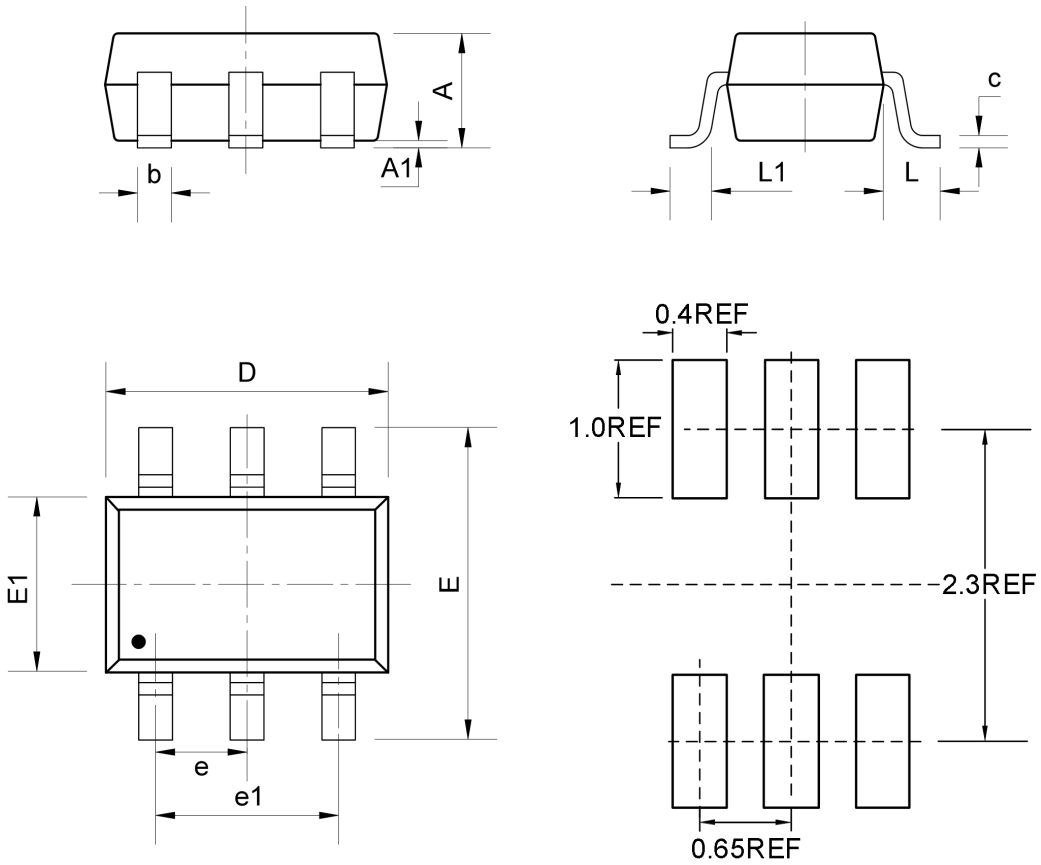


Figure17. Dual-sensor Alarm Trigger

Package Dimension

SC70-6 (1.3mm × 2.1mm)

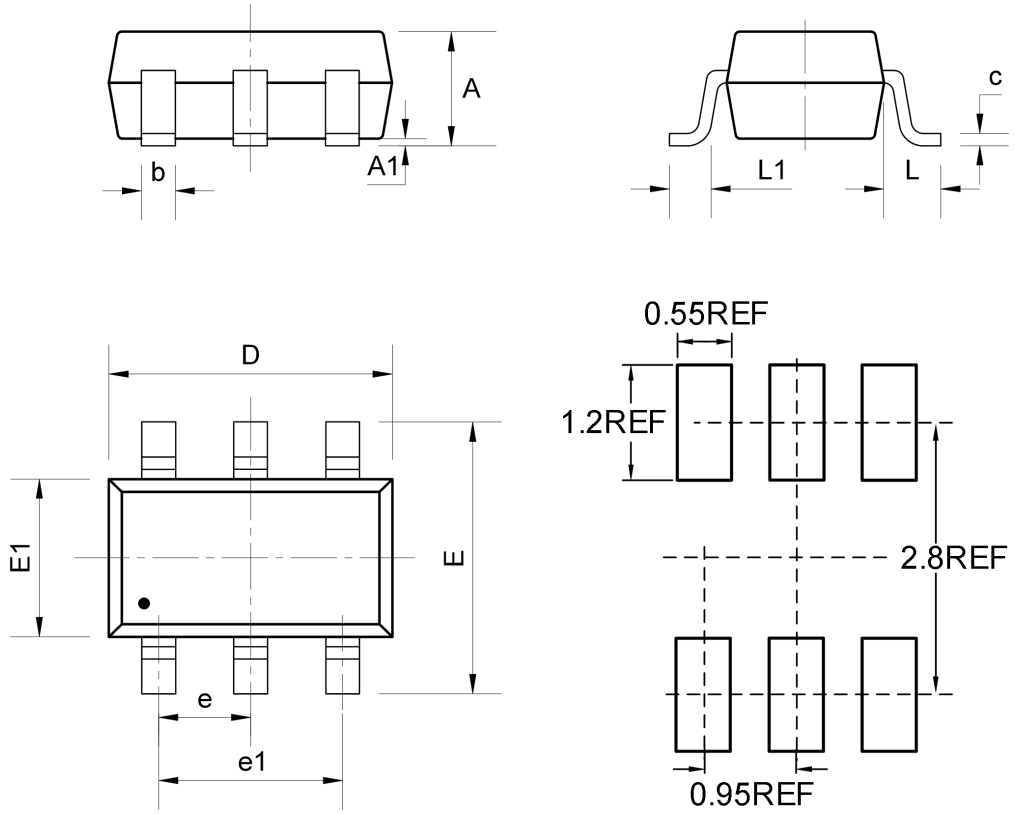


COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	-	0.15
b	0.15	-	0.35
c	0.08	-	0.20
D	2.00	2.10	2.30
e	0.65BSC		
e1	1.30BSC		
E	2.15	2.30	2.50
E1	1.15	1.30	1.45
L	0.50REF		
L1	0.33REF		

SOT23-6 (1.6mm × 2.9mm)



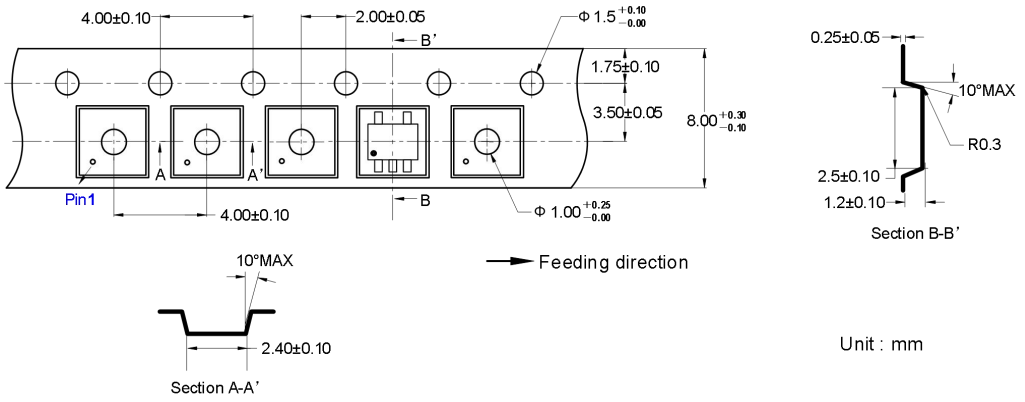
COMMON DIMENSIONS

(Unit: mm)

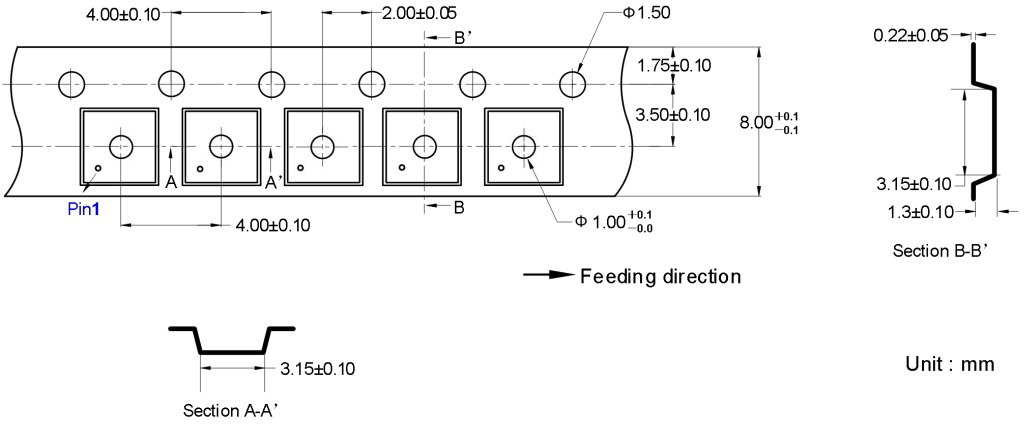
SYMBOL	MIN	NOM	MAX
A	-	-	1.45
A1	0.00	-	0.15
b	0.28	0.35	0.50
c	0.08	0.15	0.22
D	2.75	2.9	3.05
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
E	2.60	2.80	3.00
E1	1.45	1.6	1.75
L	0.60REF		
L1	0.30	0.45	0.60

Tape Information

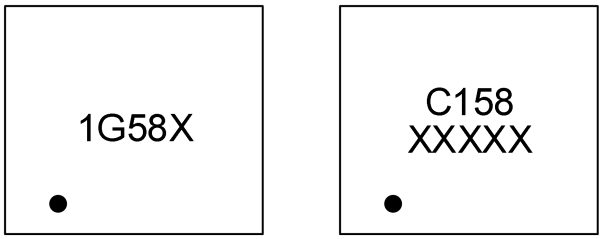
SC70-6 (1.3mm × 2.1mm)



SOT23-6 (1.6mm × 2.9mm)



Marking Information



ET74AHC1G58
1G58 = Part Number
X = Tracking Number

ET74AHC1G58T
C158 = Part Number
XXXXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025-12-25	Official Version	Xu tao	Yang xiaoxu	Liu jiaying