Dual Buffer with Open Drain Output

General Description

The ET74LV2T07 is a high-performance dual buffer with open drain outputs operating from a 1.6V to 6V supply. The internal circuit is composed of multiple stages, including an open drain output. The open drain output provides the capability to set the output switching level to a user optional value with an external resistor and power supply.

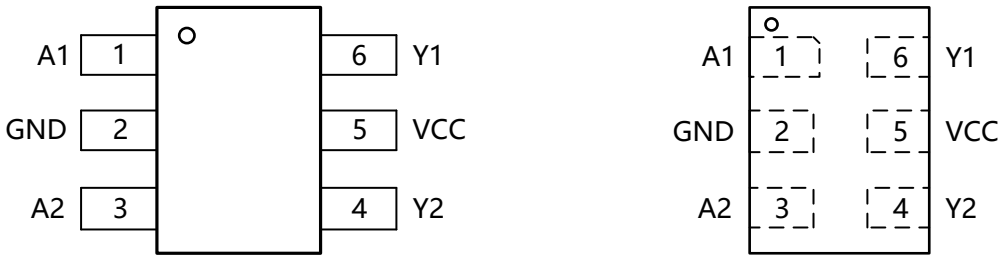
The logic high output value is set by the external power supply and can be less than, equal or greater than the V_{CC} power supply, provided the voltage supply is less than 6V.

Features

- Designed for 1.6V to 5.5V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 5.5V
- 8mA Output Sink Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- These Devices are Pb-Free and RoHS Compliant
- ESD Protection Complies with JESD22 Standard
  -- HBM: ±4000V Pass (JEDEC JS-001)
  -- CDM: ±1000V Pass (JEDEC JS-002)
- Latch-up Performance Exceeds ±100mA per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET74LV2T07	SC70-6 (1.3mm × 2.1mm)	Tape and Reel, 3K/Reel	1
ET74LV2T07T	SOT23-6 (1.6mm × 2.9mm)	Tape and Reel, 3K/Reel	3
ET74LV2T07Y	DFN6 (1.0mm × 1.5mm)	Tape and Reel, 3K/Reel	1

Pin Configuration



SC70-6/SOT23-6 DFN6

Figure1. Pin Configuration

Pin Function

SC70-6/ SOT23-6/ DFN6

Pin No.	Pin Name	Function
1	A1	Input CH1
2	GND	Ground
3	A2	Input CH2
4	Y2	Output CH2
5	VCC	Supply Voltage
6	Y1	Output CH1

Block Diagram

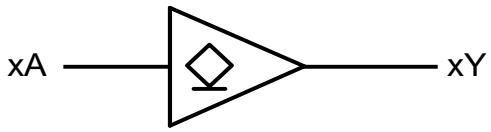


Figure2. Logic Symbol

Function Table

Input xA	Output xY
L	L
H	Z

Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage(VCC Pin)		-0.5 to 7.0	V
V_I	DC Input Voltage[1]		$-0.5 \le V_I \le 7.0$	V
V_O	DC Output Voltage Output in Higher or Low State		-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current, $V_I < GND$		-50	mA
I_{OK}	DC Output Diode Current, $V_O < GND$, $V_O > V_{CC}$		±50	mA
I_O	DC Output Sink Current		±50	mA
I_{CC}	DC Supply Current Per Supply Pin		100	mA
I_{GND}	DC Ground Current Per Supply Pin		-100	mA
T_{STG}	Storage Temperature Range		-65 to 150	°C
T_L	Lead Temperature, Soldering 10 Seconds		260	°C
T_J	Max Junction Temperature		150	°C
V_{ESD}	ESD Classification	Human Body Model [2]	±4000	V
		Charged Device Model [3]	±1000	
I_{LU}	Max Latch Up Current Above V_{CC} and GND at 125°C [4]		±100	mA

Stresses exceeding those listed in this table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch Up Current Maximum Rating tested per JEDEC JESD78F.

Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
$R_{\theta JA}$	SC70-6	Thermal Characteristics, Thermal Resistance, Junction-to-Air	280	°C/W
	SOT23-6		180	
	DFN6		440	
P_D	SC70-6	Power Dissipation in Still Air at 85°C	230	mW
	SOT23-6		360	
	DFN6		150	

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	1.6	5.5	V
V_I	DC Input Voltage	0	V_{CC}	V
V_O	DC Output Voltage(High or Low State)	0	V_{CC}	V
T_A	Operating Temperature Range	-40	125	°C

Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Condition	V_{CC}(V)	T_A = 25°C			-40°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High-level Input Voltage		1.65~1.8	0.94			1.0		V
			2.0	0.99			1.03		
			2.25~2.5	1.135			1.18		
			2.75	1.21			1.23		
			3.0~3.3	1.35			1.37		
			3.6	1.47			1.48		
			4.5~5.0	2.02			2.03		
			5.5	2.10			2.11		
V_{IL}	Low-level Input Voltage		1.65~2.0			0.45		0.40	V
			2.25~2.75			0.75		0.71	
			3.0~3.6			0.80		0.65	
			4.5~5.5			0.80		0.80	
V_{OL}	Low-level Output Voltage	I_{OL} = 20μA	1.65~5.5			0.1		0.1	V
		I_{OL} = 2mA	1.65			0.2		0.25	
		I_{OL} = 2.3mA	2.3			0.1		0.15	
		I_{OL} = 3mA	2.3			0.15		0.2	
		I_{OL} = 3mA	3.0			0.1		0.15	
		I_{OL} = 5.5mA	3.0			0.2		0.252	
		I_{OL} = 4mA	4.5			0.15		0.2	
		I_{OL} = 8mA	4.5			0.3		0.35	
I_I	Input Leakage Current	V_I = 5.5V or GND	0~5.5			±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	V_I = 5.5 V or GND	5.5			1.0		10	μA
ΔI_{CC}	Additional Supply Current	Per Input Pin; V_I = 0.3V or 1.1V; I_O = 0mA; Other Pins at V_{CC} or GND	1.8			10		10	μA
		Per Input Pin; V_I = 0.3V or 3.4V; I_O = 0mA; Other Pins at V_{CC} or GND	5.5			1.35		1.5	mA

Electrical Characteristics (Continued)

AC Electrical Characteristics

Symbol	Parameter	Condition	V_{CC}(V)	T_A = 25°C			-40°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLZ} t_{PZL}	Propagation Delay (Figure3 & 4)	C_L = 15pF	1.8		12.2	15.4		17.4	ns
		C_L = 30pF	1.8		13.1	16.6		17.6	
		C_L = 15pF	2.5		8.4	10.4		12	
		C_L = 30pF	2.5		9.1	11.3		13	
		C_L = 15pF	3.3		6.7	8.3		9.4	
		C_L = 30pF	3.3		7.3	8.9		10.2	
		C_L = 15pF	5.0		5.6	6.5		7.3	
		C_L = 30pF	5.0		6	7		7.9	

Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.5V, V_I = 0V or V_{CC}	2.5	pF
C_{PD}	Power Dissipation Capacitance (5)	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	26	pF
		10MHz, V_{CC} = 5.5V, V_I = 0V or V_{CC}	30	

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

AC Test Circuit

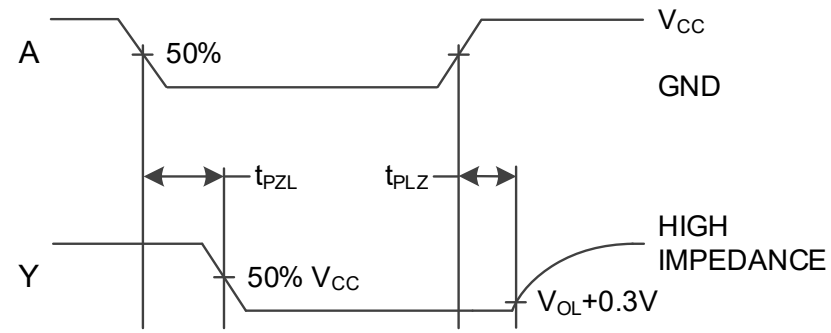
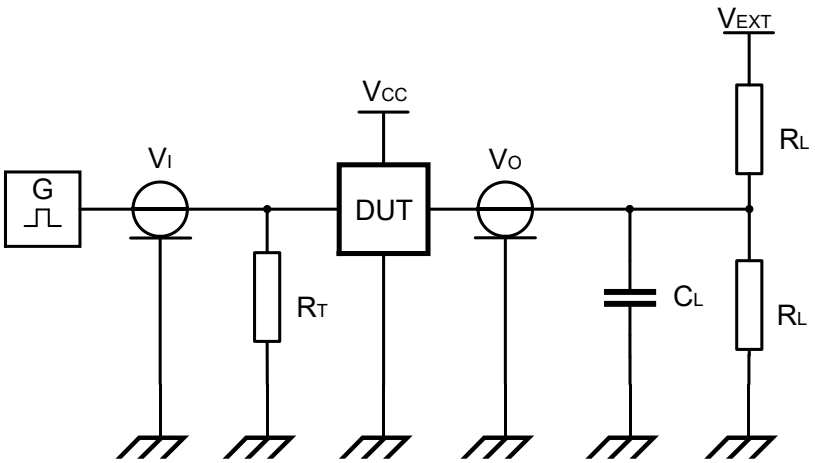


Figure3. Switching Waveform



Measurement points are given in Table1.

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

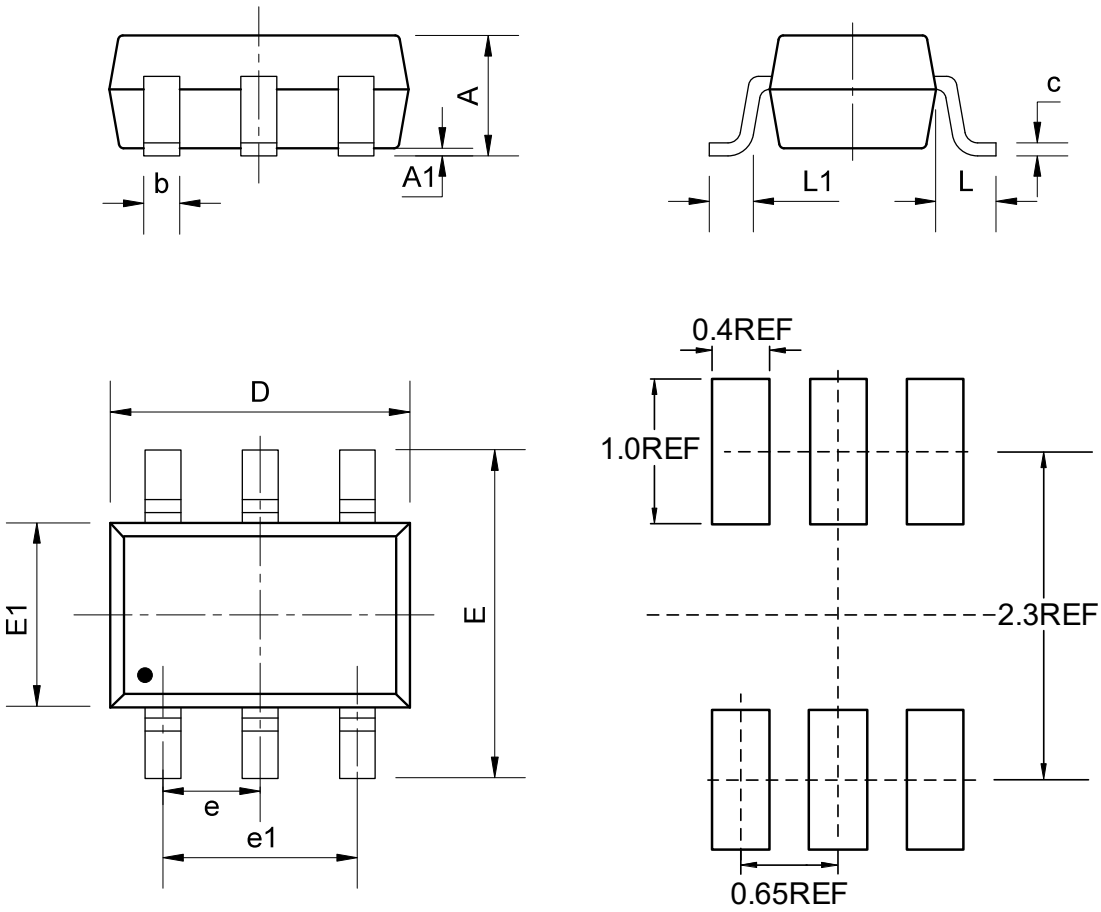
Figure.4 Test circuit for measuring switching times

Table1. Test Data

Supply Voltage	Input			Load		V_{EXT}
V_{CC}	V_I	$t_r = t_f$	f_{max}	C_L	R_L	t_{PLZ}, t_{PZL}
1.8V	V_{CC}	≤ 3ns	15MHz	15pF, 30pF	1kΩ	$2V_{CC}$
2.5V	V_{CC}	≤ 3ns	25MHz	15pF, 30pF	1kΩ	$2V_{CC}$
3.3V	3V	≤ 3ns	50MHz	15pF, 30pF	1kΩ	$2V_{CC}$
5.0V	3V	≤ 3ns	50MHz	15pF, 30pF	1kΩ	$2V_{CC}$

Package Dimension

SC70-6 (1.3mm × 2.1mm)

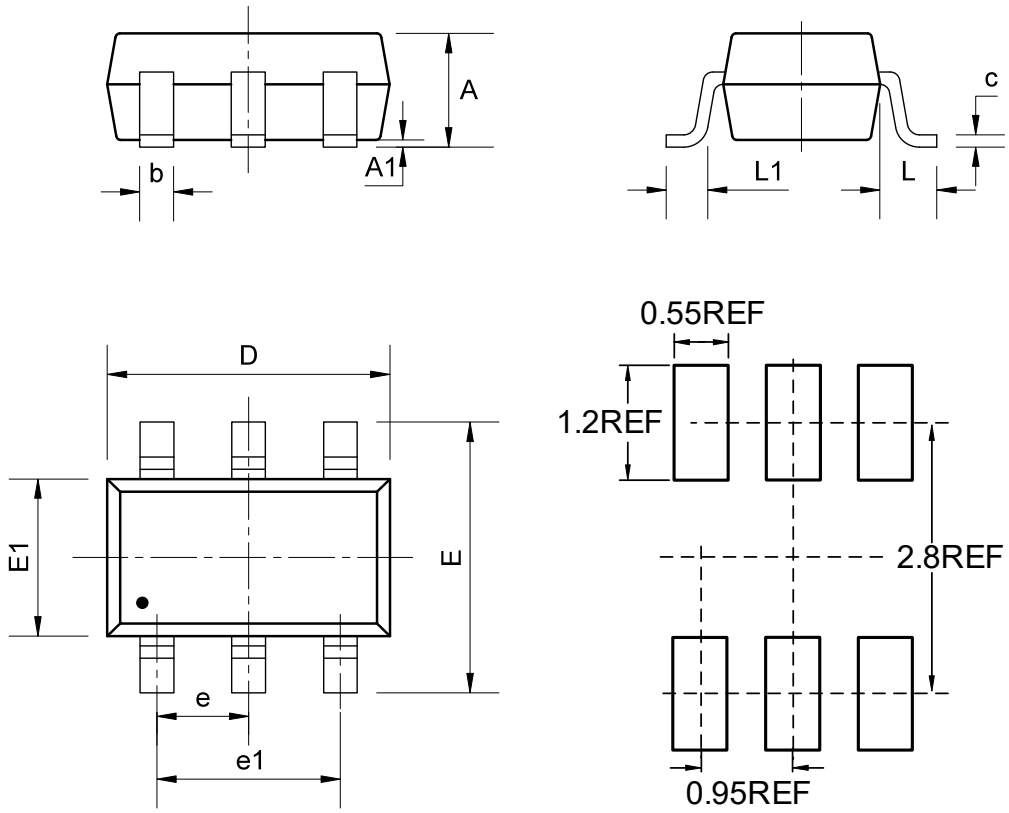


COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	-	0.15
b	0.15	-	0.35
c	0.08	-	0.20
D	2.00	2.10	2.30
e	0.65BSC		
e1	1.30BSC		
E	2.15	2.30	2.50
E1	1.15	1.30	1.45
L	0.50REF		
L1	0.33REF		

SOT23-6 (1.6mm × 2.9mm)

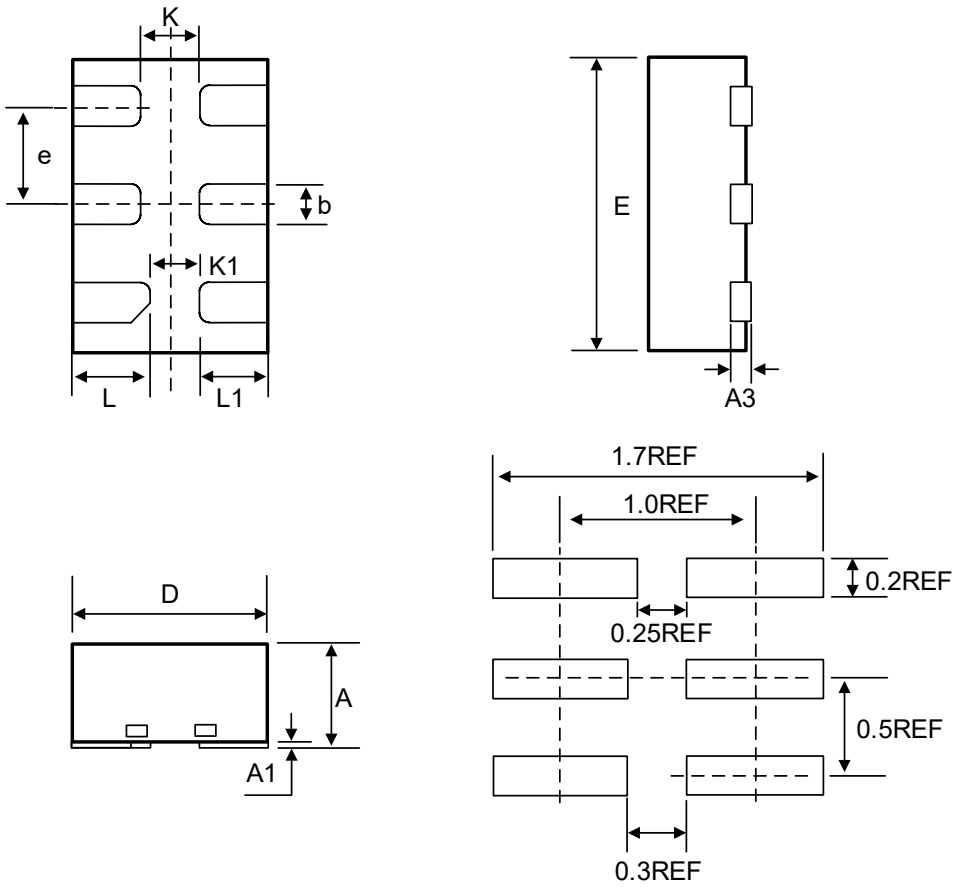


COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.45
A1	0.00	-	0.15
b	0.28	0.35	0.50
c	0.08	0.15	0.22
D	2.75	2.9	3.05
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
E	2.60	2.80	3.00
E1	1.45	1.6	1.75
L	0.60REF		
L1	0.30	0.45	0.60

DFN6 (1.0mm × 1.5mm)



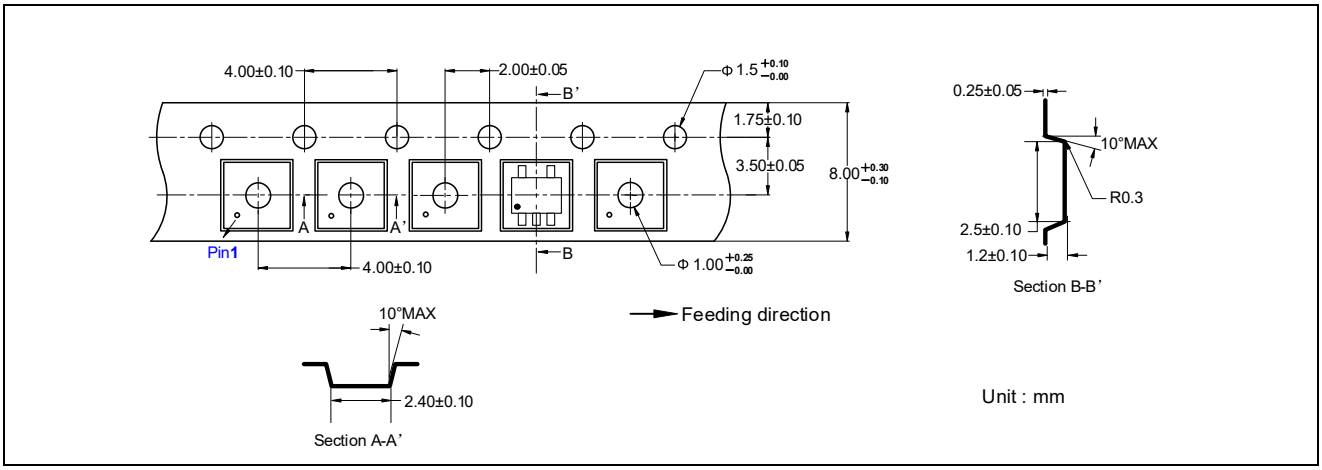
COMMON DIMENSIONS

(Unit: mm)

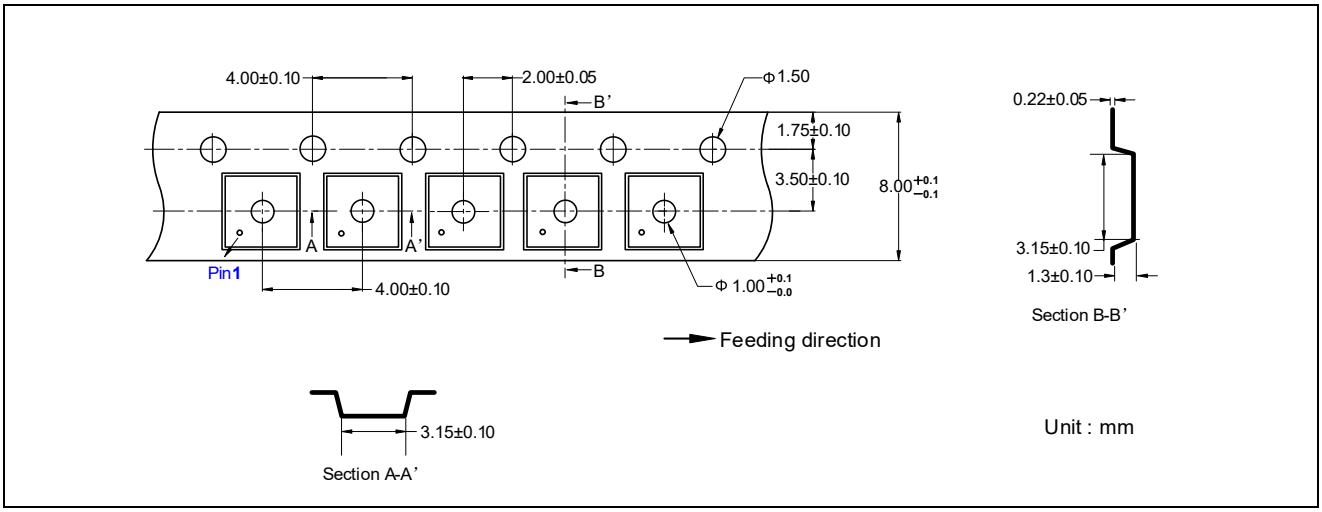
SYMBOL	MIN	NOM	MAX
A	0.50	--	0.60
A1	0.00	0.02	0.05
A3		0.10REF	
b	0.15	0.20	0.25
D	0.90	1.00	1.10
E	1.40	1.50	1.60
e		0.50BSC	
K		0.30REF	
K1		0.25REF	
L	0.35	0.40	0.45
L1	0.30	0.35	0.40

Tape Information

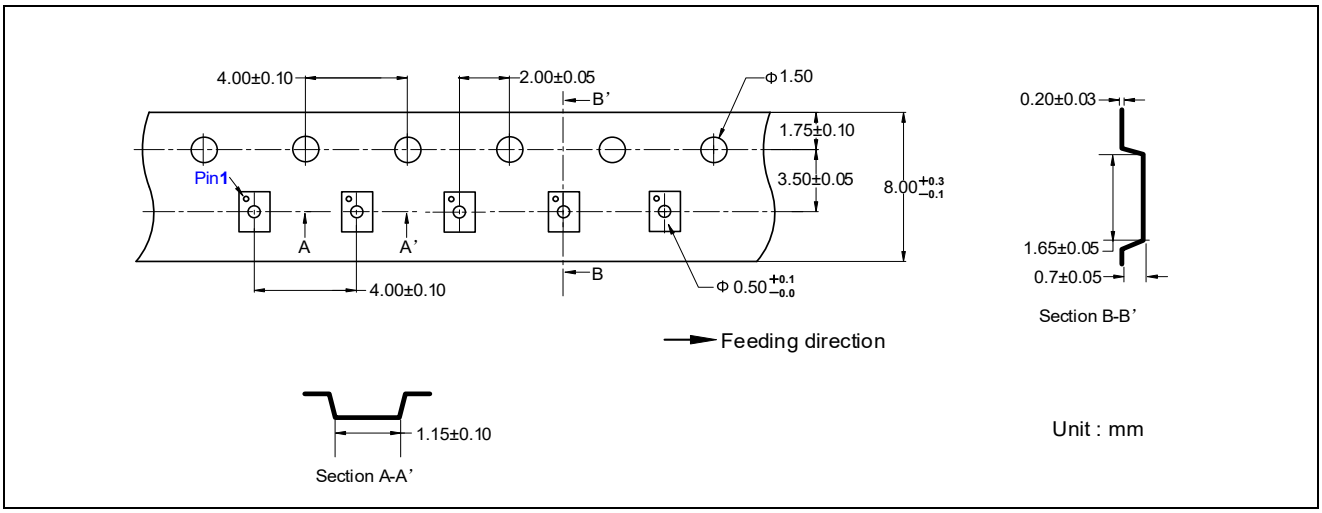
SC70-6 (1.3mm × 2.1mm)



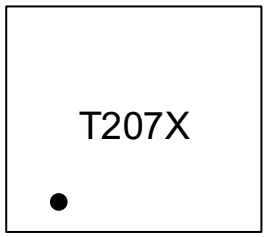
SOT23-6 (1.6mm × 2.9mm)



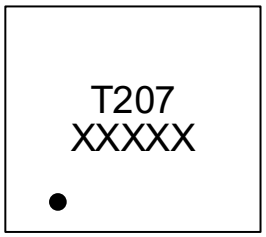
DFN6 (1.0mm × 1.5mm)



Marking Information



ET74LV2T07
T207 = Part Number
X = Tracking Number



ET74LV2T07T
T207 = Part Number
XXXXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025-12-02	Official Version	Wang anran	Yang xiaoxu	Liu jiaying
1.0.a	2026-01-06	Update Format, Add Tape and Marking	Xu tao	Yang xiaoxu	Liu jiaying
1.0.b	2026-04-22	Correct Words	Xu tao	Yang xiaoxu	Liu jiaying