High-Current Over-Voltage Protectors with Adjustable OVLO and Input Voltage Detection

General Description

ET9540CL can disconnect the systems from its output pin(OUT) in case wrong input operating conditions are detected. The system is positive over-voltage protected up to 28V. The internal over-voltage threshold(OVLO) is 6.8V.

ET9540CL has internal Thermal-Shutdown Protection and Input Voltage detection.

The device is packaged in advanced full-Green compliant WLCSP12 package.

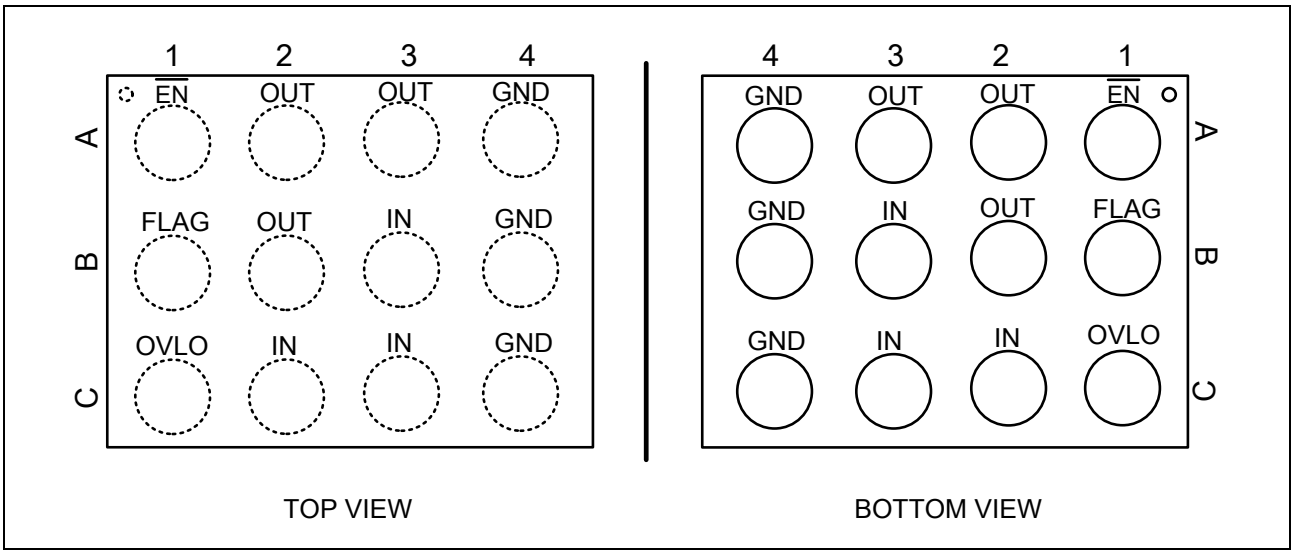
Features

- 4.5A Continuous Current Capability
- Typical R_{ON}: 30mΩ N-Channel MOSFET
- VIN Operating Range: 2.5V to 28V
- Internal Over-voltage Lockout: 6.8V
- Over-voltage-Protection Response Time：50ns(TYP)
- Startup Debounce Time:15ms(TYP)
- Internal Thermal-Shutdown Protection
- Surge Immunity to ±100V
- ESD Protected: Human Body Model (JESD22-A114) All pins ±2KV Pass
- WLCSP12 (1.55mm×1.10mm 0.4mm pitch) Package
- MSL 1

Application

- Smartphones, Tablet PC
- HDD, Storage and Solid State Memory Devices
- Portable Media Devices, Laptop & MID
- SLR Digital Cameras
- GPS and Navigation Equipment
- Industrial Handheld and Enterprise Equipment

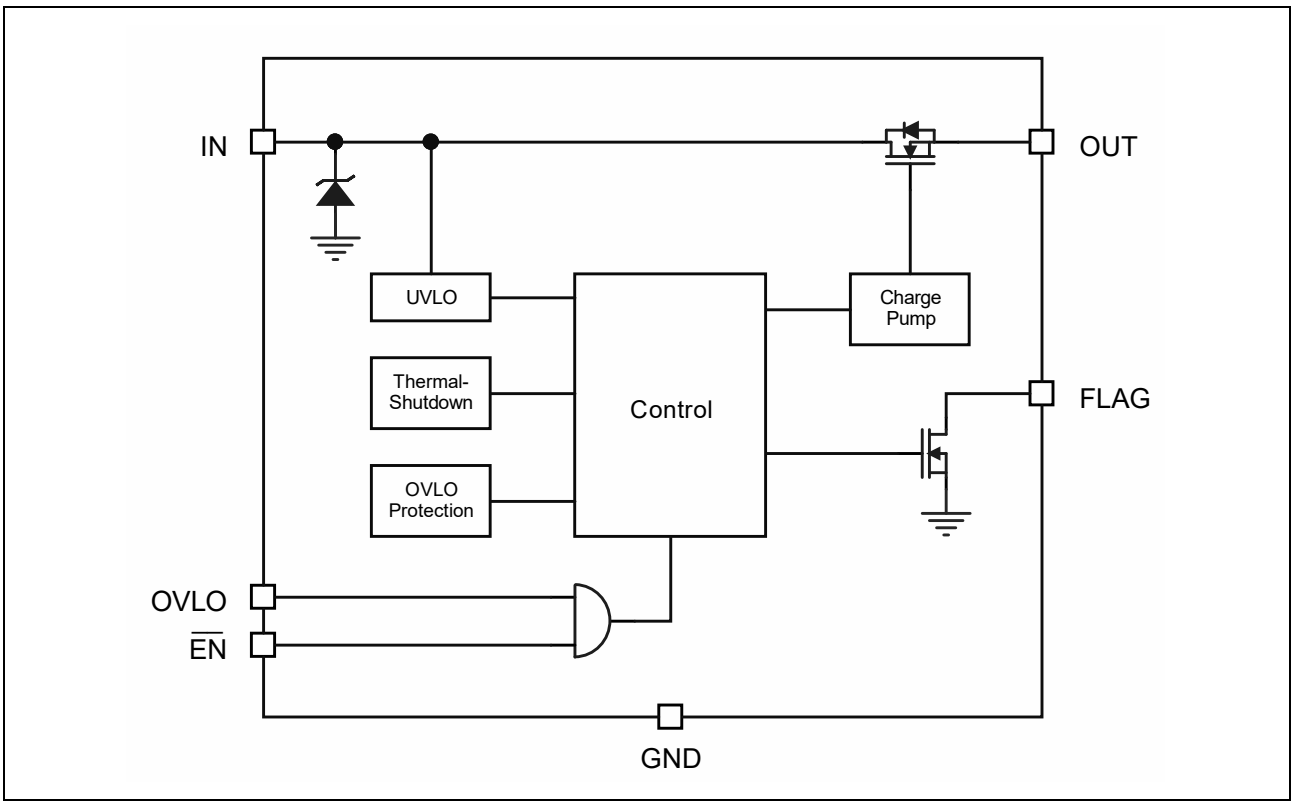
Pin Configuration



Pin Function

Pin	Name	Description		
A1	$\overline{EN}$	Device Enable. Active low.		
A2,A3,B2	OUT	Output Voltage. Output of internal switch. Connect OUT pins together for proper operation.		
A4,B4,C4	GND	Ground. Connect GND pins together for proper operation.		
B1	FLAG	Power status indicator	1	$V_{IN}<V_{UVLO}$ or $V_{IN}>V_{OVLO}$
			0	V_{IN} Stable
B3,C2,C3	IN	Voltage Input. Connect IN pins together for proper operation.		
C1	OVLO	External OVLO Adjustment. Connect OVLO to GND when using the internal threshold. Connect a resistor-divider to OVLO to set a different OVLO threshold; this external resistor-divider is completely independent of the internal threshold.		

Block Diagram



Functional Description

The OVP switch with over-voltage protection feature a low 30mΩ (TYP) on-resistance (R_{ON}) internal FET and protect low-voltage systems against voltage faults up to 28 V_{DC}. If $\overline{EN}$ is in the logic low state, when the input voltage(VIN) exceeds 6.8V, the internal FET is quickly turned off to prevent damage to the protected downstream components and the flag pin will output logic high state. If $\overline{EN}$ is in the logic high state, the switch will be shutdown. If there is no input voltage at IN pin, the flag pin output logic high state.

When input (OVLO) is set lower than 0.2V. The over-voltage protection threshold is 6.8V.

The over-voltage protection threshold can also be adjusted by external resistors when input (OVLO) is set higher than 0.3V.

$$\mathbf{V_{IN_OVLO} = V_{OVLO_TH} \times (1+R1/R2)}$$

Note: V_{OVLO_TH} = 1.2V(TYP)

The internal FET turns off when the junction temperature exceeds +155ºC (TYP). The device exits thermal shutdown after the junction temperature cools by 20ºC (TYP).

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into a discharged load capacitor or short-circuit, a capacitor 0.1μF or lager must be placed between the VIN and GND pins.

Output Capacitor

A 1μF or lager capacitor should be placed between the OUT and GND pins.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameters			Min	Max	Unit
V_{IN}	VIN to GND			-0.3	29	V
V_{OUT}	VOUT to GND			-0.3	V_{IN}+0.3	V
V_{OVLO}	OVLO to GND			-0.3	7	V
$V_{/EN}$	$\overline{EN}$ to GND			-0.3	7	V
V_{FLAG}	FLAG to GND			-0.3	7	V
I_{SW1}	Maximum Continuous Current of switch IN-OUT				4.5	A
I_{SW2}	Maximum Peak Current of switch IN-OUT(10ms)				7	A
P_D	Power Dissipation at T_A= +25°C				1.0	W
T_{STG}	Storage Junction Temperature			-65	+150	°C
T_A	Operating Temperature Range			-40	+85	°C
T_{SOLD}	Soldering Temperature (reflow).				+260	°C
T_J	Junction Temperature				+150	°C
V_{ESD}	Electrostatic Discharge Capability	IEC 61000-4-2 System Level ESD	Air Discharge	-15	+15	kV
			Contact Discharge	-8	+8	
		Human Body, ANSI/ESDA/JEDEC JS-001-2012	All Pins	-2	+2	
		Charged Device Model, JESD22-C101	All Pins	-1.5	+1.5	
Surge		IEC 61000-4-5, Surge Protection	VBUS	-100	100	V

Electrical Characteristics

T_A=-40°C to 85°C unless otherwise noted, typical values are at V_{IN}=5V, I_{IN}≤2A, C_{IN}=0.1uF and T_A=25°C.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Basic Operation						
V_{IN}	Input Voltage		2.5		28	V
V_{IN_CLAMP}	Input Clamping Voltage	I_{IN}=10mA		36		V
I_{IN}	V_{IN} Quiescent Current	V_{IN}=5V, OUT Floating		95		μA
R_{ON}	On-Resistance of Switch IN-OUT	V_{IN}=5.0V, I_{OUT}=1A, T_A=25°C		30	39	mΩ
V_{OVLO}	Over-voltage protect of V_{IN}	V_{IN} Rising, OVLO=GND	6.6	6.8	7.0	V
	Over-voltage protect hysteresis of V_{IN}			0.25		V
	Adjustable OVLO Threshold Range	V_{IN}=2.5V to V_{OVLO}	4		20	V
V_{OVLO_TH}	OVLO Set Threshold	V_{IN}=2.5V to V_{OVLO}	1.18	1.2	1.22	V
V_{OVLO_SELECT}	External OVLO Select Threshold		0.2		0.3	V
V_{UVLO_R}	Under Voltage Lockout Threshold	V_{IN} Rising		2.1		V
V_{UVLO_F}		V_{IN} Falling		1.9		V
V_{OL_FLAG}	FLAG Output Logic Low Voltage	V_{PU}=1.8V, I_{SINK}=1mA		0.1	0.2	V
I_{FLAG_LEAK}	FLAG Output HIGH Leakage Current	V_{FLAG}=5V,			0.5	uA
I_{OVLO}	OVLO Input Leakage Current	V_{OVLO}=V_{OVLO_TH}	-100		100	nA
V_{IH}	$\overline{EN}$ Input Logic High Voltage		1.4			V
V_{IL}	$\overline{EN}$ Input Logic Low Voltage	V_{IN}=2.5V			0.3	V
T_{SHDN}	Thermal Shutdown(1)			155		°C
T_{SHDN_HYS}	Thermal-shutdown Hysteresis(1)			20		°C
Dynamic Characteristics						
t_{DEB}	Debounce Time	Time from V_{UVLO_R}<V_{IN}< V_{OVLO} to V_{OUT}=10% of V_{IN}		15		ms
t_{SS}	Soft-start time	Time from V_{UVLO_R}<V_{IN}< V_{OVLO} to 0.2×FLAG, VIO=1.8V with 10kΩ Pull-up Resistor		30		ms

Electrical Characteristics(Continued)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
t_{ON}	Switch Turn-On Time	R_L=100Ω, C_L=22uF, V_{OUT} from 0.1×V_{IN} to 0.9×V_{IN}		2		ms
t_{OFF_RES}[(1)]	Switch turn-off response time	V_{IN} > V_{OVLO} to V_{OUT} stop rising		50		ns

Note1: Guaranteed by characterization and design.

Timing Waveform

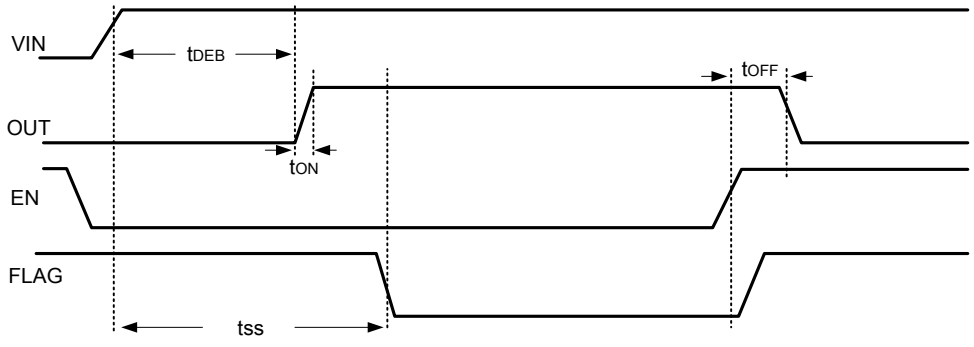


Figure1. Timing for Power Up and Normal Operation

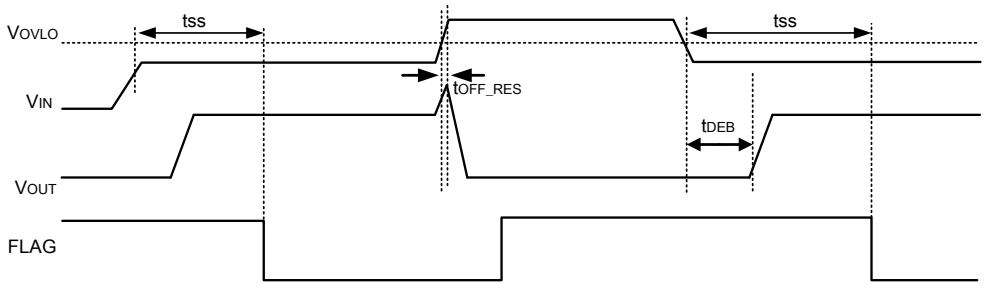


Figure2. Timing for OVLO Trip

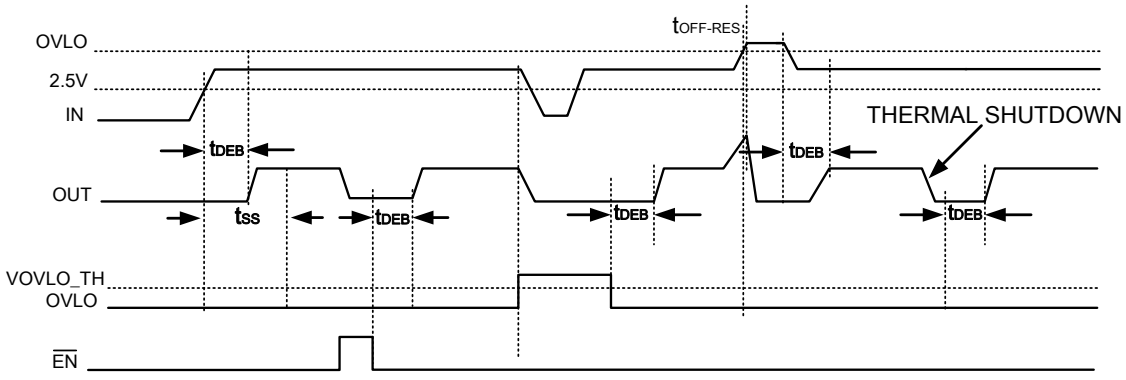
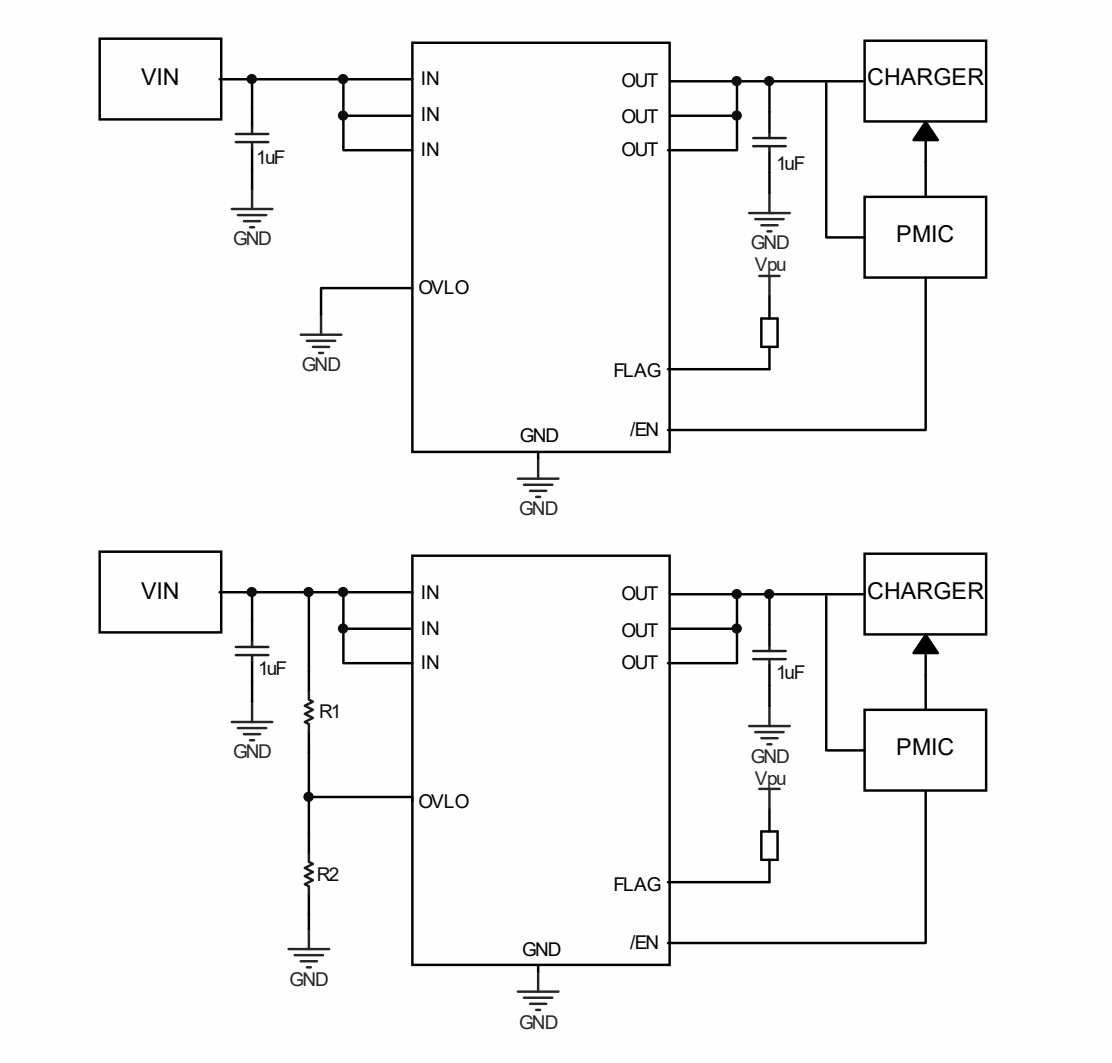


Figure3. Timing Waveform

Application Circuits



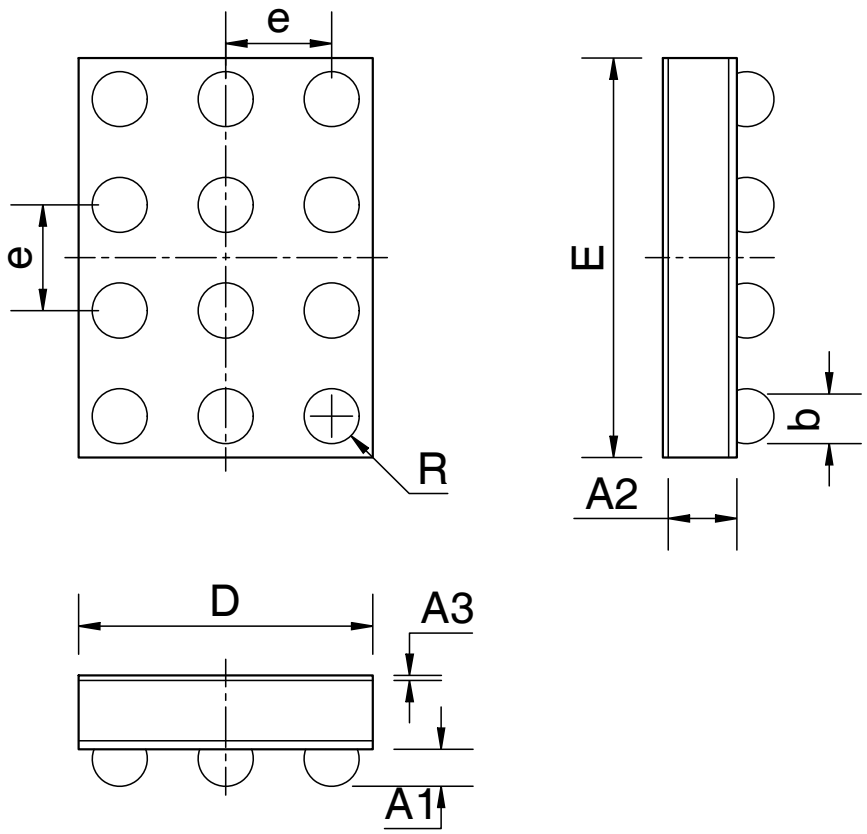
R1 and R2 are only required for adjustable OVLO; otherwise connect OVLO to GND

Recommend 30K ≤ R2 ≤ 51K

Note*:* This electric circuit only supplies for reference.

Package Dimension

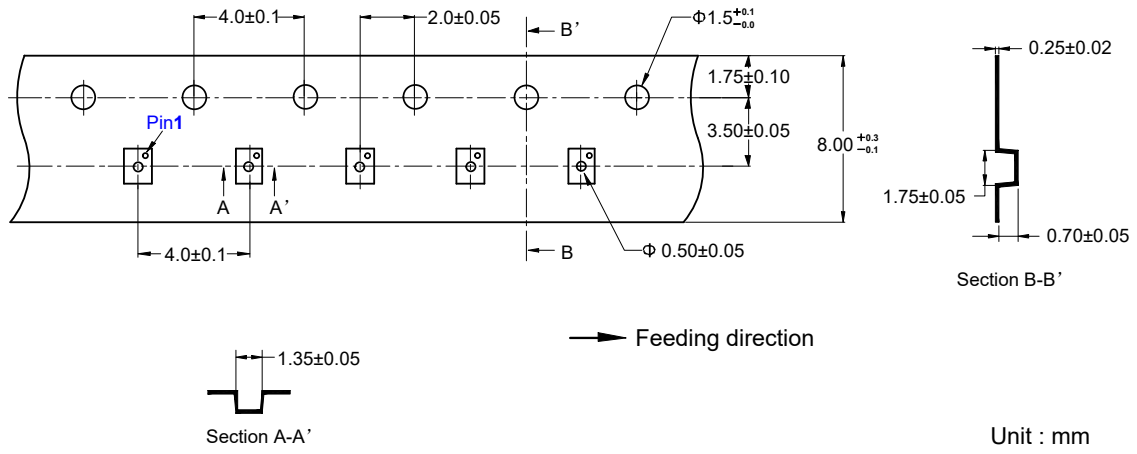
WLCSP12



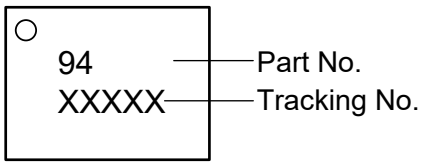
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A1	0.12	0.14	0.16
A2	0.39	0.40	0.41
A3	0.028	0.035	0.042
b	0.15	0.18	0.21
D	1.05	1.10	1.15
E	1.50	1.55	1.60
e	0.40BSC		
R	0.15	0.18	0.21

Tape Information



Marking



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2018-01-22	Original Version	Wu Min	Wu Min	Zhu Jun Li
1.1	2018-03-20	Add Ron Max	Wuxj	Wuxj	Zhu Jun Li
1.2	2019-12-27	Update some electrical parameters	Wu Min	Wuxj	Liu Jia Ying
1.3	2021-8-11	Add Tape Information	Wuxj	Wuxj	Zhu Jun Li
1.4	2022-11-18	Update Typeset	Shibo	Wum	Liujy
1.5	2026-05-23	Update Timing Waveform	Caojc	Wuhs	Liujy