Single D-type Flip-Flop with Set and Reset; Positive Edge Trigger

General Description

The ET74AHC1G74 is a single positive edge triggered D-type flip-flop with individual data (D), clock (CP), set ($\overline{SD}$) and reset ($\overline{RD}$) inputs, and complementary Q and $\overline{Q}$ outputs. Data at the D-input that meets the set-up and hold time requirements on the Low-to-High clock transition will be stored in the flip-flop and appear at the Q output. Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in mixed 3.3V and 5V environments.

Schmitt trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging back-flow current through the device when it is powered down.

Features

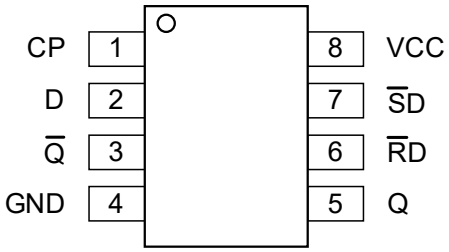
- Designed for 2V to 5.5V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 5.5V
- High Noise Immunity
- ±8mA Balanced Output Sink and Source Capability
- CMOS Low Power Consumption
- Direct Interface with TTL Levels
- I_{OFF} Circuitry Provides Partial Power-down Mode Operation
- ESD Protection Complies with JESD22 Standard
  -- HBM: ±4000V Pass (JEDEC JS-001)
  -- CDM: ±1500V Pass (JEDEC JS-002)
- Latch-up Performance Exceeds ±200mA per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET74AHC1G74U	MSOP8 (3.0mm × 3.0mm)	Tape and Reel, 4K/Reel	3

Applications

- Server
- LED Display Screen
- Network Switches
- Telecommunications Infrastructure
- Motor Driver
- I/O Extender

Pin Configuration



MSOP8

Figure2. Logic Symbol

Pin Function

MSOP8

Pin No.	Pin Name	Pin Function
1	CP	Clock Input (Low-to-High, Edge-Triggered)
2	D	Data Input
3	$\overline{Q}$	Complement Output
4	GND	Ground
5	Q	True Output
6	$\overline{RD}$	Asynchronous Reset-direct Input (Active Low)
7	$\overline{SD}$	Asynchronous Set-direct Input (Active Low)
8	VCC	Supply Voltage

Functional Diagram

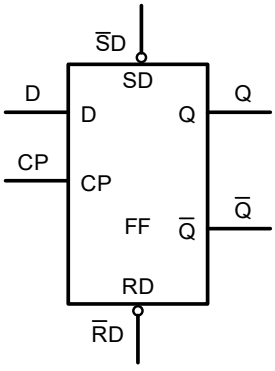


Figure2. Logic Symbol

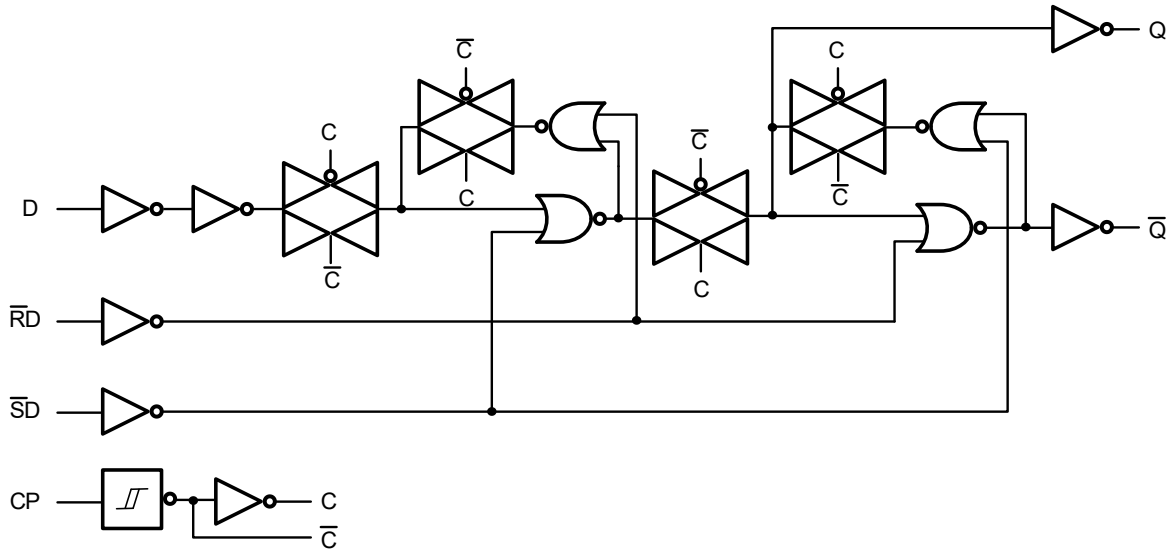


Figure3. Logic Diagram

Functional Description

Table1. Function Table for Asynchronous Operation

H = High voltage level; L = Low voltage level; X = Don't care.

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

Table2. Function Table for Synchronous Operation

H = High voltage level; L = Low voltage level; ↑ = Low-to-High CP transition;

Q_{n+1} = state after the next Low-to-High CP transition.

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L
H	H	L	X	Q_n	$\overline{Q}_n$

Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage (VCC Pin)		-0.5 to 6.5	V
I_{IK}	DC Input Diode Current, V_I < GND		-20	mA
V_I	DC Input Voltage (1)		-0.5 ≤ V_I ≤ 6.5	V
I_{OK}	DC Output Diode Current, V_O < GND		±20	mA
V_O	DC Output Voltage Output in Higher or Low State		-0.5 to V_{CC} + 0.5	V
I_O	DC Output Sink Current, V_O = 0V to V_{CC}		±25	mA
I_{CC}	DC Supply Current per Supply Pin		75	mA
I_{GND}	DC Ground Current per Supply Pin		-75	mA
T_J	Max Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-65 to 150	°C
V_{ESD}	ESD Classification	Human Body Model (2)	±4000	V
		Charged Device Model (3)	±1500	
I_{LU}	Max Latch Up Current Above V_{CC} and GND at 125°C (4)		±200	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch up Current Maximum Rating tested per JEDEC JESD78F.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage Operating		2	5.5	V
V_I	DC Input Voltage		0	V_{CC}	V
V_O	DC Output Voltage (High or Low State)		0	V_{CC}	V
T_A	Operating Temperature Range		-40	125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.0V to 3.6V		100	ns/V
		V_{CC} = 4.5V to 5.5V		20	

Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			-40°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High-Level Input Voltage		2	1.5			1.5		V
			3	2.1			2.1		
			5.5	3.85			3.85		
V_{IL}	Low-Level Input Voltage		2			0.5		0.5	V
			3			0.9		0.9	
			5.5			1.65		1.65	
V_{OH}	High-Level Output Voltage	I_{OH} = -50uA	2	1.9	2		1.9		V
		I_{OH} = -50uA	3	2.9	3		2.9		
		I_{OH} = -50uA	4.5	4.4	4.5		4.4		
		I_{OH} = -4mA	3	2.58			2.4		
		I_{OH} = -8mA	4.5	3.94			3.7		
V_{OL}	Low-Level Output Voltage	I_{OL} = 50uA	2		0	0.1		0.1	V
		I_{OL} = 50uA	3		0	0.1		0.1	
		I_{OL} = 50uA	4.5		0	0.1		0.1	
		I_{OL} = 4mA	3			0.36		0.55	
		I_{OL} = 8mA	4.5			0.36		0.55	
I_I	Input Leakage Current	V_I = 5.5V or GND	0~5.5			0.1		2.0	uA
I_{CC}	Quiescent Supply Current	V_I = 5.5V or GND	5.5			1.0		40	uA

AC Electrical Characteristics

Voltages are referenced to GND (ground = 0V); for test circuit see Figure6.

All typical values are measured at corresponding V_{CC} and T_A = 25°C.

Symbol	Parameter	Conditions	T_A = 25°C			-40°C ≤ T_A ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	
t_{pd}	Propagation Delay	CP to Q,$\overline{Q}$; See Figure4						ns
		V_{CC} = 3V~3.6V, C_L = 15pF		3.3	5.7		6.5	
		V_{CC} = 4.5V~5.5V, C_L = 15pF		3.0	4.2		4.7	
		V_{CC} = 3V~3.6V, C_L = 50pF		3.6	6.5		7.5	
		V_{CC} = 4.5V~5.5V, C_L = 50pF		2.9	4.1		4.7	
		$\overline{SD}$/$\overline{RD}$ to Q,$\overline{Q}$; See Figure5						
		V_{CC} = 3V~3.6V, C_L = 15pF		3.4	4.7		5.4	
		V_{CC} = 4.5V~5.5V, C_L = 15pF		3.0	3.6		4.0	
		V_{CC} = 3V~3.6V, C_L = 50pF		3.4	5.5		6.5	
		V_{CC} = 4.5V~5.5V, C_L = 50pF		2.8	4.7		4.7	
t_W	Pulse Width	CP High or Low; See Figure4						ns
		V_{CC} = 3V~3.6V	2.7			2.7		
		V_{CC} = 4.5V~5.5V	2.0			2.0		
		$\overline{SD}$ and $\overline{RD}$ Low; See Figure5						
		V_{CC} = 3V~3.6V	2.7			2.7		
		V_{CC} = 4.5V~5.5V	2.0			2.0		
t_{rec}	Recovery Time	$\overline{SD}$ and $\overline{RD}$; See Figure5						ns
		V_{CC} = 3V~3.6V	1.2			1.2		
		V_{CC} = 4.5V~5.5V	1.0			1.0		
t_{su}	Set-up Time	D to CP; See Figure4						ns
		V_{CC} = 3V~3.6V,	1.0			1.0		
		V_{CC} = 4.5V~5.5V	1.0			1.0		
t_h	Hold Time	D to CP; See Figure4						ns
		V_{CC} = 3V~3.6V,	1.0			1.0		
		V_{CC} = 4.5V~5.5V	1.0			1.0		
f_{max}	Maximum Frequency	CP; See Figure4						MHz
		V_{CC} = 3V~3.6V,	175			175		
		V_{CC} = 4.5V~5.5V	200			200		

Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.5V, V_I = 0V or V_{CC}	4.5	pF
C_{PD}	Power Dissipation Capacitance (5)	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	37	pF

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}{}^2 \times f_o)$ where:

f_i = Input Frequency in MHz;

f_o = Output Frequency in MHz;

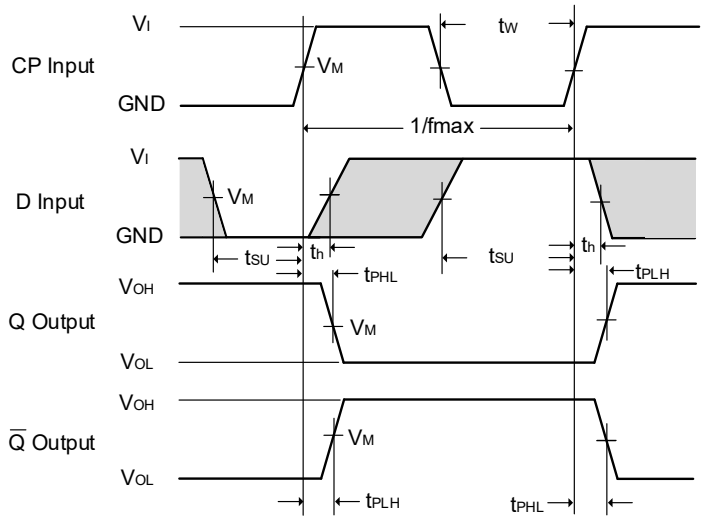
C_L = Output Load capacitance in pF;

V_{CC} = Supply Voltage in V;

N = Number of Inputs Switching;

$\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = Sum of Outputs.

Test Waveform

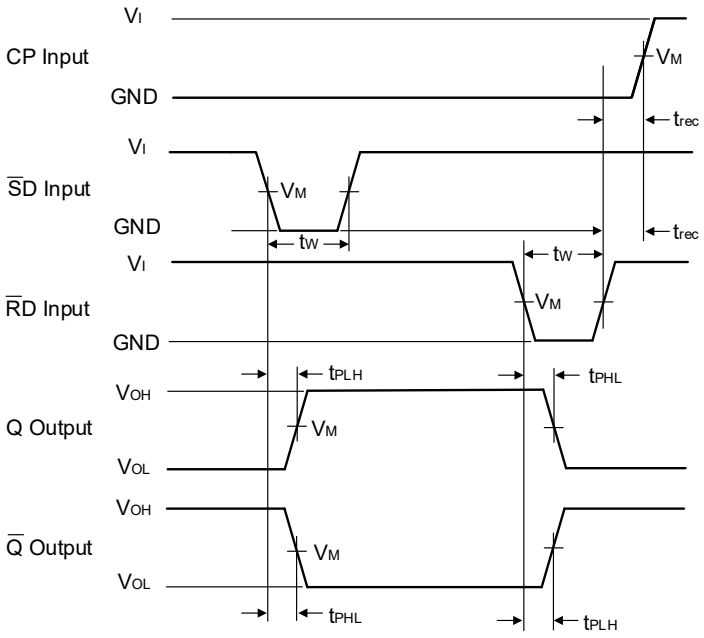


Measurement points are given in Table3.

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure4. The clock input (CP) to output (Q, $\overline{Q}$) propagation delays and pulse width, D to CP set-up, CP to D hold times and the maximum frequency



Measurement points are given in Table3.

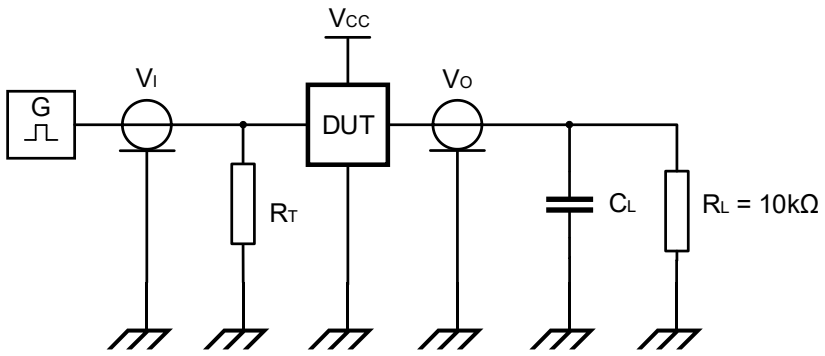
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure5. The set ($\overline{SD}$) and reset ($\overline{RD}$) input to output (Q, $\overline{Q}$) propagation delays, pulse widths and the $\overline{RD}$ to CP recovery time

Table3. Measurement Points

Supply Voltage	Input	Output
V_{CC}	V_M	V_M
2.0V to 5.5V	0.5 × V_{CC}	0.5 × V_{CC}

Test Circuit



Measurement points are given in Dynamic Characteristics.

Definitions test circuit:

R_L = Load resistance;

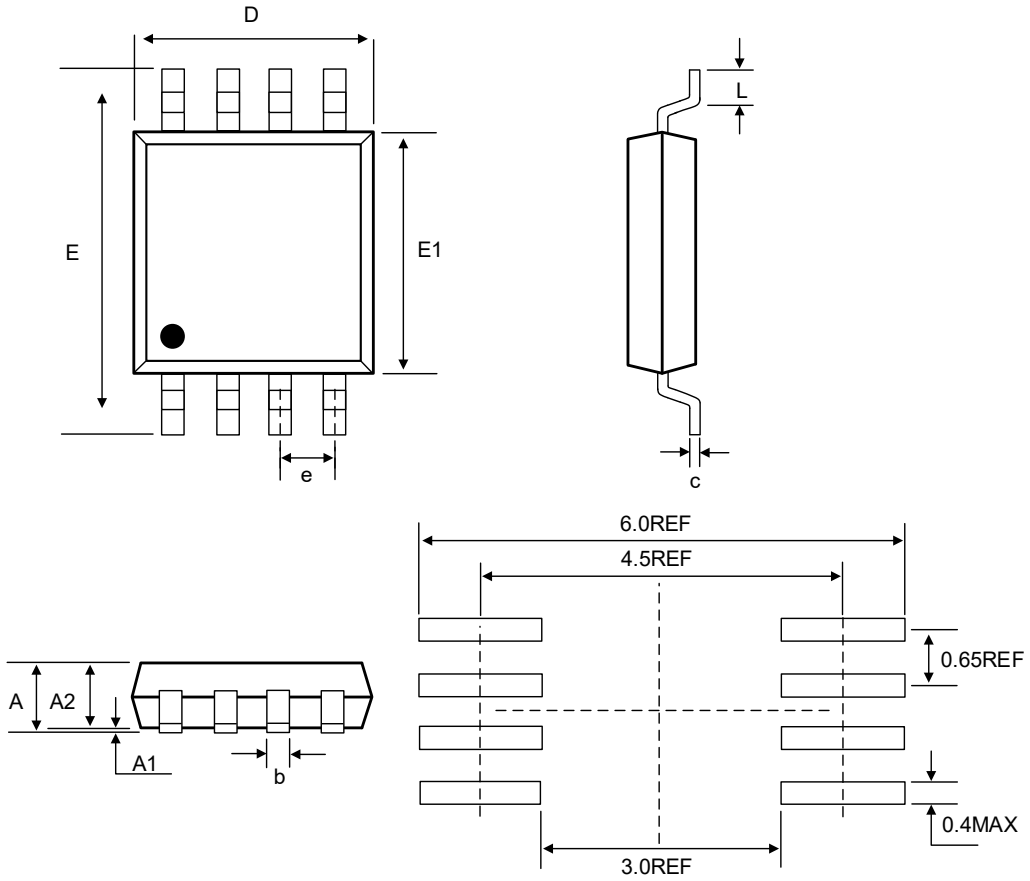
C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator;

Figure6. Test circuit for measuring switching times

Package Dimension

MSOP8 (3.0mm × 3.0mm)



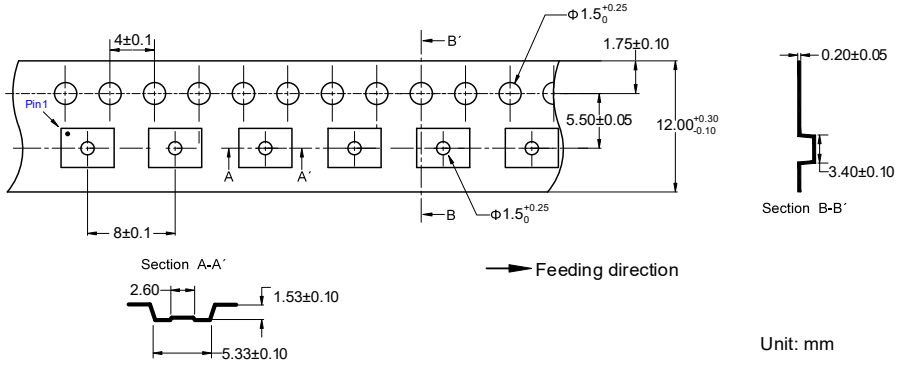
COMMON DIMENSIONS

(Unit: mm)

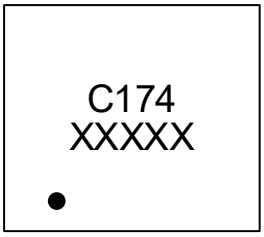
SYMBOL	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	-	0.15
A2	0.75	0.85	0.95
b	0.22	0.30	0.38
c	0.08	0.1	0.20
D	2.90	3.00	3.10
E	3.90	-	5.10
E1	2.90	3.00	3.10
e	0.65BSC		
L	0.33	-	0.7

Tape Information

MSOP8 (3.0mm × 3.0mm)



Marking Information



ET74AHC1G74U

C174 = Part Number

XXXXXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025-05-07	Official Version	Xu tao	Yang xiaoxu	Liu jiaying