# Single D-type Flip-Flop; Positive Edge Trigger

## General Description

The ET74AHC1G79 is a single positive edge triggered D-type flip-flop, Data at the D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the Q output. Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in mixed 3.3V and 5V environments.

Schmitt trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using $I_{OFF}$. The $I_{OFF}$ circuitry disables the output, preventing the potentially damaging back-flow current through the device when it is powered down.

## Features

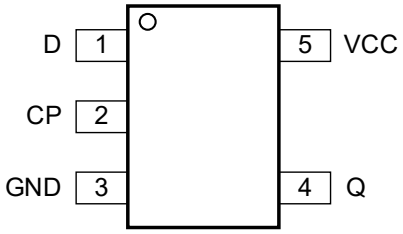
- Designed for 2V to 5.5V $V_{CC}$ Operation
- Over-voltage Tolerant Inputs Accept Voltages to 5.5V
- ±8mA Balanced Output Sink and Source Capability
- Near-zero Static Supply Current Substantially Reduces System Power Requirements
- These Devices are Pb-Free and RoHS Compliant
- ESD Protection Complies with JESD22 Standard
  -- HBM: ±4000V Pass (JEDEC JS-001)
  -- CDM: ±1500V Pass (JEDEC JS-002)
- Latch-up Performance Exceeds ±200mA per JEDEC JESD78F
- Part No. and Package Information

| Part No. | Package | Packing Option | MSL |
|---|---|---|---|
| ET74AHC1G79 | SC70-5 (1.3mm × 2.1mm) | Tape and Reel, 3K/Reel | 1 |
| ET74AHC1G79T | SOT23-5 (1.6mm × 2.9mm) | Tape and Reel, 3K/Reel | 3 |

## Applications

- Server
- LED Display Screen
- Network Switches
- Telecommunications Infrastructure
- Motor Driver
- I/O Extender

## Pin Configuration




SC70-5/SOT23-5

Figure1. Pin Configuration

## Pin Function

SC70-5/SOT23-5

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1 | D | Data Input |
| 2 | CP | Clock Pulse Input |
| 3 | GND | Ground |
| 4 | Q | Data Output |
| 5 | VCC | Supply Voltage |

## Functional Diagram

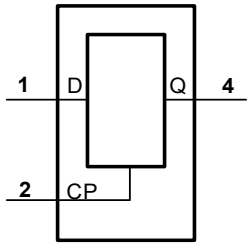



Figure2. Logic Symbol

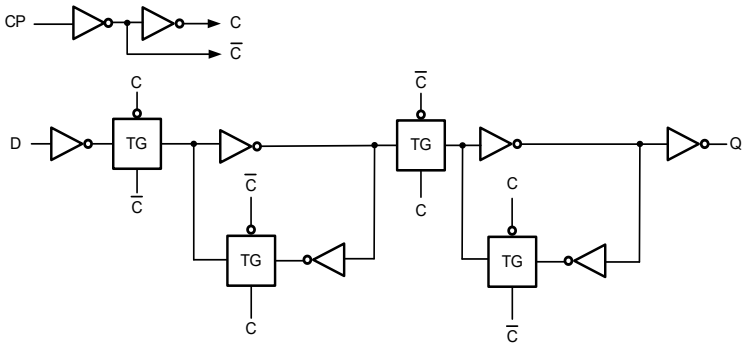



Figure3. Logic Diagram

## Function Table

H = High voltage level; L = Low voltage level; ↑ = Low-to-High CP transition; X = don't care;
q = lower case letter indicates the state of referenced input, one set-up time prior to the LOW-to-HIGH CP transition.

| Input | | Output |
|---|---|---|
| **CP** | **D** | **Q** |
| ↑ | L | L |
| ↑ | H | H |
| L | X | q |

## Absolute Maximum Ratings

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (VCC Pin) | | -0.5 to 6.5 | V |
| $I_{IK}$ | DC Input Diode Current, $V_I$ < GND | | -20 | mA |
| $V_I$ | DC Input Voltage (1) | | -0.5 ≤ $V_I$ ≤ 6.5 | V |
| $I_{OK}$ | DC Output Diode Current, $V_O$ < GND | | ±20 | mA |
| $V_O$ | DC Output Voltage Output in Higher or Low State | | -0.5 to $V_{CC}$ + 0.5 | V |
| $I_O$ | DC Output Sink Current, $V_O$ = 0V to $V_{CC}$ | | ±25 | mA |
| $I_{CC}$ | DC Supply Current per Supply Pin | | 75 | mA |
| $I_{GND}$ | DC Ground Current per Supply Pin | | -75 | mA |
| $T_J$ | Max Junction Temperature | | 150 | °C |
| $T_{STG}$ | Storage Temperature Range | | -65 to 150 | °C |
| $V_{ESD}$ | ESD Classification | Human Body Model (2) | ±4000 | V |
| | | Charged Device Model (3) | ±1500 | |
| $I_{LU}$ | Max Latch Up Current Above $V_{CC}$ and GND at 125°C (4) | | ±200 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

***Note1:*** $I_O$ absolute maximum rating must be observed.

***Note2:*** HBM tested per JEDEC JS-001;

***Note3:*** CDM tested per JEDEC JS-002;

***Note4:*** Latch up Current Maximum Rating tested per JEDEC JESD78F.

## Thermal Characteristics

| Symbol | Package | Ratings | Value | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | SC70-5 | Thermal Characteristics, Thermal Resistance, Junction-to-Air | 280 | °C/W |
| | SOT23-5 | | 180 | |
| $P_D$ | SC70-5 | Power Dissipation in Still Air at 85°C | 230 | mW |
| | SOT23-5 | | 360 | |

## Recommended Operating Conditions

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage Operating | | 2.0 | 5.5 | V |
| $V_I$ | DC Input Voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | DC Output Voltage (High or Low State) | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature Range | | -40 | 125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time | $V_{CC}$ = 3.0V to 3.6V | | 100 | ns/V |
| | | $V_{CC}$ = 4.5V to 5.5V | | 20 | |

## Electrical Characteristics

### DC Electrical Characteristics

| Symbol | Parameter | Condition | $V_{CC}$(V) | $T_A$ = 25°C | | | -40°C ≤ $T_A$ ≤ 125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IH}$ | High-Level Input Voltage | | 2 | 1.5 | | | 1.5 | | V |
| | | | 3 | 2.1 | | | 2.1 | | |
| | | | 5.5 | 3.85 | | | 3.85 | | |
| $V_{IL}$ | Low-Level Input Voltage | | 2 | | | 0.5 | | 0.5 | V |
| | | | 3 | | | 0.9 | | 0.9 | |
| | | | 5.5 | | | 1.65 | | 1.65 | |
| $V_{OH}$ | High-Level Output Voltage | $I_{OH}$ = -50uA | 2 | 1.9 | 2 | | 1.9 | | V |
| | | $I_{OH}$ = -50uA | 3 | 2.9 | 3 | | 2.9 | | |
| | | $I_{OH}$ = -50uA | 4.5 | 4.4 | 4.5 | | 4.4 | | |
| | | $I_{OH}$ = -4mA | 3 | 2.58 | | | 2.4 | | |
| | | $I_{OH}$ = -8mA | 4.5 | 3.94 | | | 3.7 | | |
| $V_{OL}$ | Low-Level Output Voltage | $I_{OL}$ = 50uA | 2 | | 0 | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 50uA | 3 | | 0 | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 50uA | 4.5 | | 0 | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4mA | 3 | | | 0.36 | | 0.55 | |
| | | $I_{OL}$ = 8mA | 4.5 | | | 0.36 | | 0.55 | |
| $I_I$ | Input Leakage Current | $V_I$ = 5.5V or GND | 0~5.5 | | | 0.1 | | 2.0 | uA |
| $I_{CC}$ | Quiescent Supply Current | Per Pin: $V_I$ = 5.5V or GND; $I_O$ = 0mA | 5.5 | | | 1.0 | | 40 | uA |

## AC Electrical Characteristics

Voltages are referenced to GND (ground = 0V); for test circuit see Figure6

| Symbol | Parameter | Conditions | $T_A$ = 25°C | | | -40°C ≤ $T_A$ ≤ 125°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $t_{pd}$ | Propagation Delay (See Figure4) | CP to Q | | | | | | ns |
| | | $V_{CC}$ = 3V~3.6V, $C_L$ = 15pF | | 3.3 | 5.7 | | 6.5 | |
| | | $V_{CC}$ = 3V~3.6V, $C_L$ = 50pF | | 3.0 | 4.2 | | 4.7 | |
| | | $V_{CC}$ = 4.5V~5.5V, $C_L$ = 15pF | | 3.6 | 6.5 | | 7.5 | |
| | | $V_{CC}$ = 4.5V~5.5V, $C_L$ = 50pF | | 2.9 | 4.1 | | 4.7 | |
| $t_W$ | Pulse Width (See Figure5) | CP High or Low | | | | | | ns |
| | | $V_{CC}$ = 3V~3.6V | 2.5 | | | 2.5 | | |
| | | $V_{CC}$ = 4.5V~5.5V | 2.0 | | | 2.0 | | |
| $t_{su}$ | Set-up Time (See Figure5) | D to CP | | | | | | ns |
| | | $V_{CC}$ = 3V~3.6V | 1.3 | | | 1.2 | | |
| | | $V_{CC}$ = 4.5V~5.5V | 1.2 | | | 1.2 | | |
| $t_h$ | Hold time (See Figure5) | D to CP | | | | | | ns |
| | | $V_{CC}$ = 3V~3.6V | 0.5 | | | 0.5 | | |
| | | $V_{CC}$ = 4.5V~5.5V | 0.5 | | | 0.5 | | |
| $f_{max}$ | Maximum Frequency (See Figure5) | CP | | | | | | MHz |
| | | $V_{CC}$ = 3V~3.6V | 160 | | | 160 | | |
| | | $V_{CC}$ = 4.5V~5.5V | 200 | | | 200 | | |

## Capacitance Characteristics

| Symbol | Parameter | Condition | Typ | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = 5V, $V_I$ = 0V or $V_{CC}$ | 5 | pF |
| $C_{PD}$ | Power Dissipation Capacitance (5) | 10MHz, $V_{CC}$ = 3.3V, $V_I$ = 0V or $V_{CC}$ | 25 | pF |

***Note5:*** $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

$f_i$ = Input Frequency in MHz;

$f_o$ = Output Frequency in MHz;

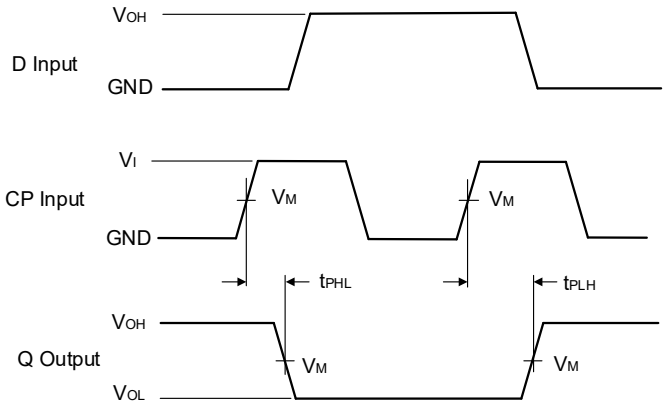
$C_L$ = Output Load capacitance in pF;

$V_{CC}$ = Supply Voltage in V;

N = Number of Inputs Switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of Outputs.

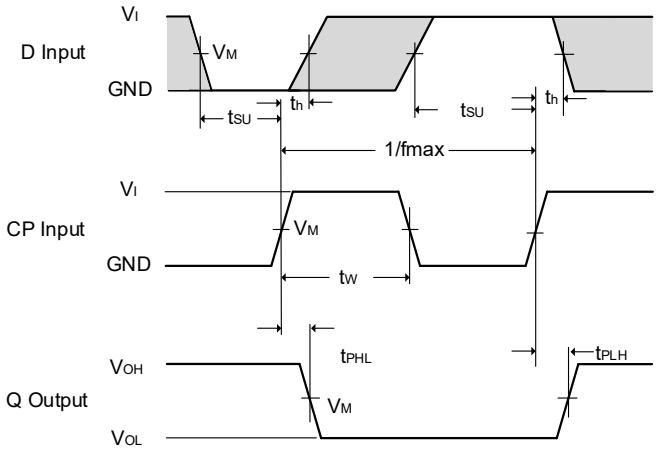
## Test Waveform




Measurement points are given in Table1.

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

Figure4. Clock (CP) to output (Q) propagation delay times




Measurement points are given in Table1.

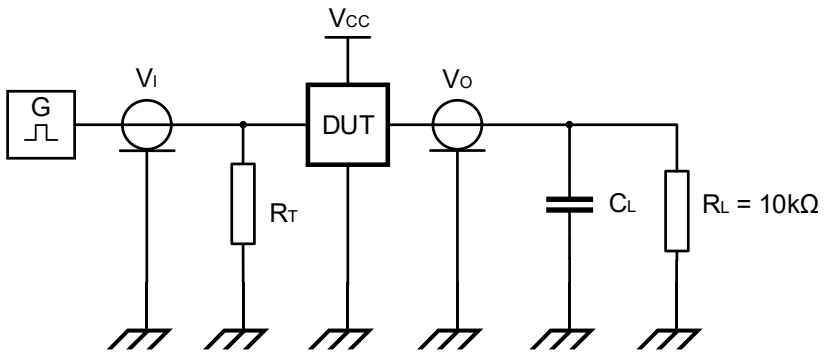
$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output.

Figure5. Clock (CP) to output (Q) propagation delay times, clock pulse width, D to CP set-up times,CP to D hold times and maximum clock pulse frequency

Table1.Measurement Points

| Supply Voltage | Input | Output |
|---|---|---|
| $V_{CC}$ | $V_M$ | $V_M$ |
| 2V to 5.5V | 0.5 × $V_{CC}$ | 0.5 × $V_{CC}$ |

## Test Circuit




Measurement points are given in Dynamic Characteristics.

Definitions test circuit:

$R_L$ = Load resistance;

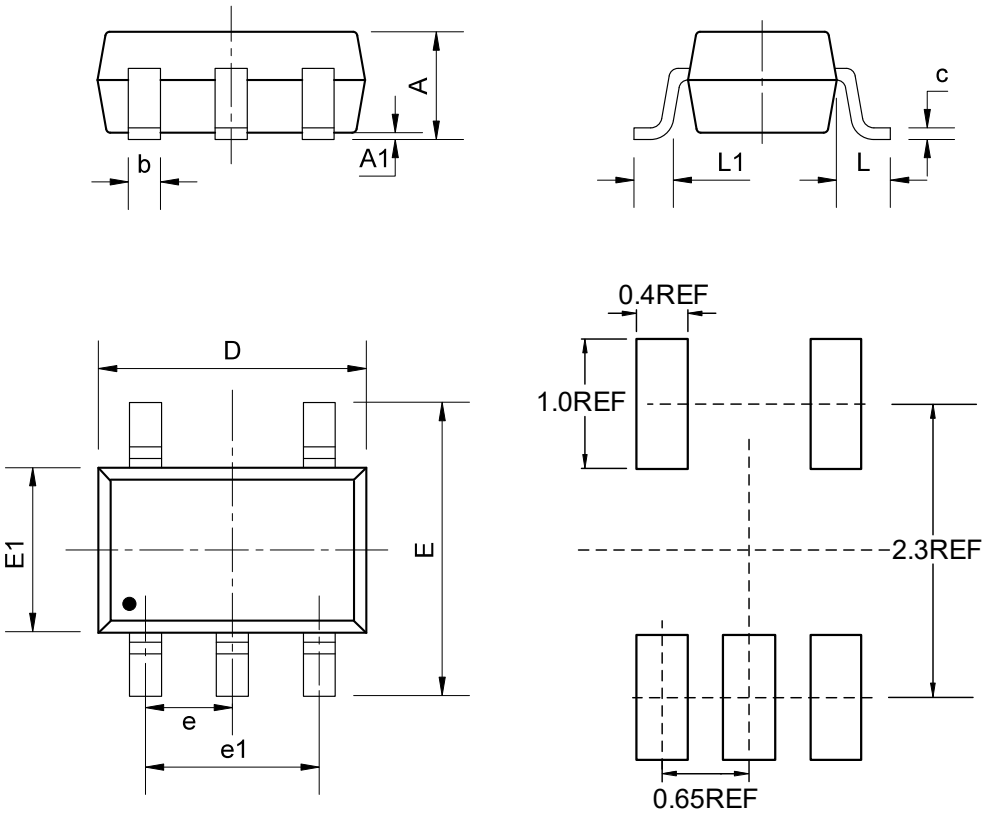
$C_L$ = Load capacitance including jig and probe capacitance;

$R_T$ = Termination resistance should be equal to output impedance $Z_O$ of the pulse generator;

Figure6. Test circuit for measuring switching times

## Package Dimension

SC70-5 (1.3mm × 2.1mm)

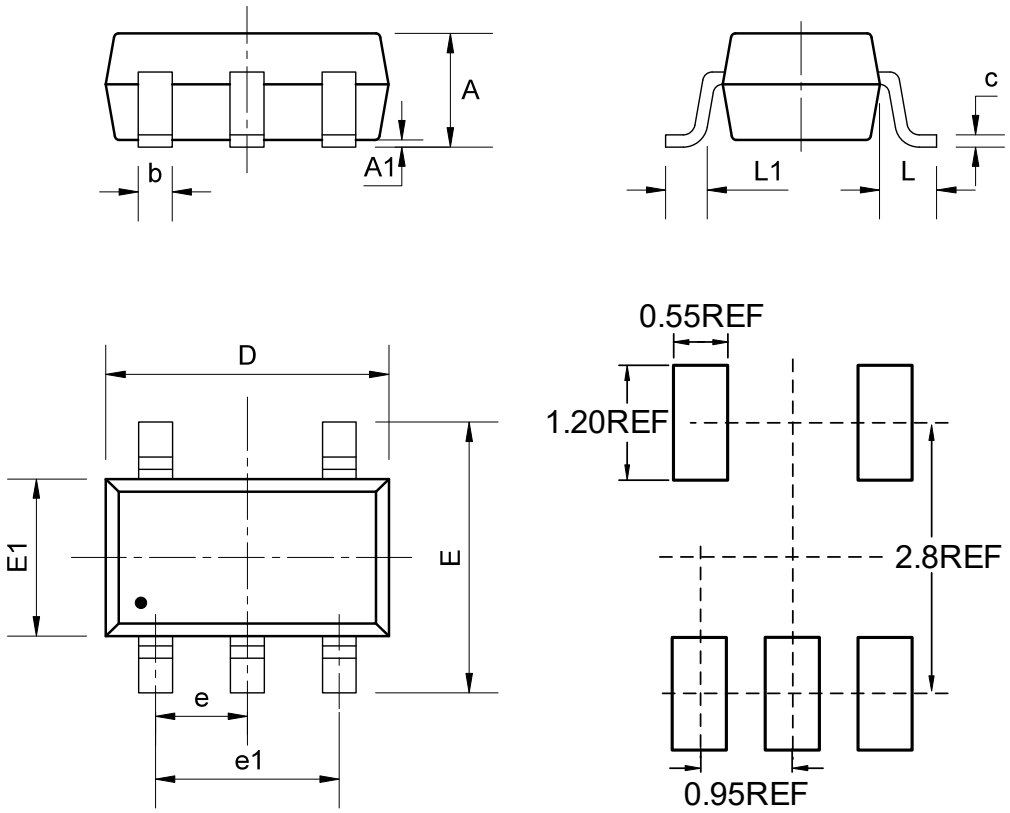



COMMON DIMENSIONS

(Unit: mm)

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | - | - | 1.10 |
| A1 | 0.00 | - | 0.15 |
| b | 0.15 | - | 0.35 |
| c | 0.08 | - | 0.20 |
| D | 2.00 | 2.10 | 2.30 |
| e | 0.65BSC | | |
| e1 | 1.30BSC | | |
| E | 2.15 | 2.30 | 2.50 |
| E1 | 1.15 | 1.30 | 1.45 |
| L | 0.50REF | | |
| L1 | 0.33REF | | |

SOT23-5 (1.6mm × 2.9mm)



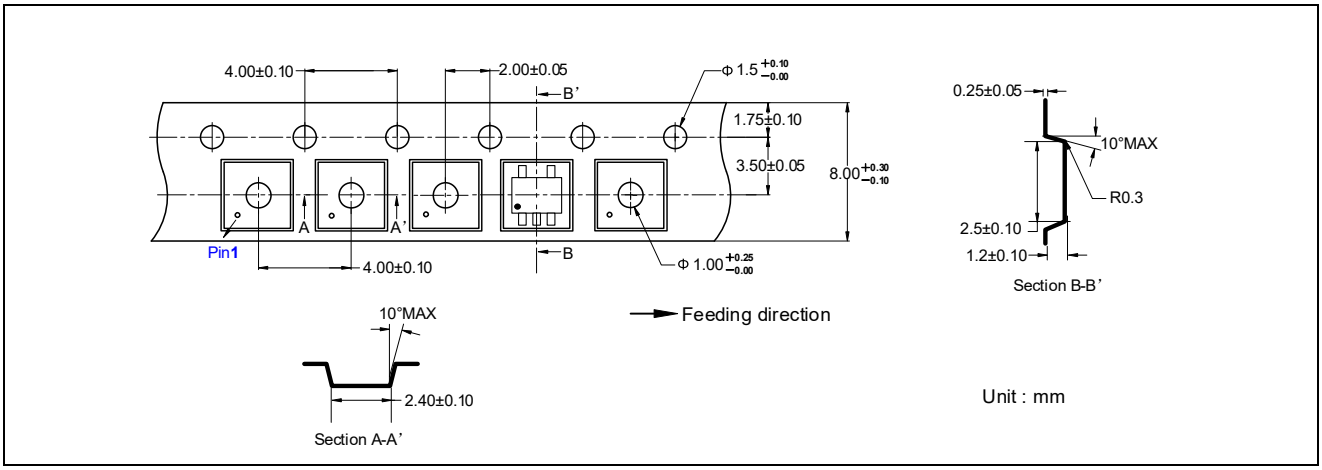

COMMON DIMENSIONS

(Unit: mm)

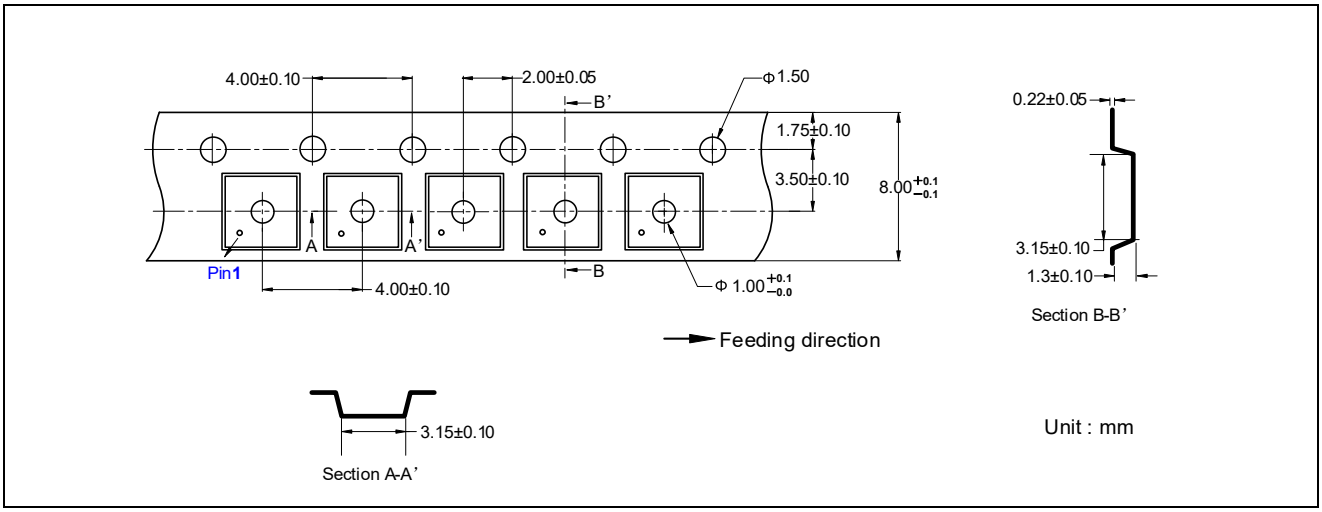
| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | - | - | 1.45 |
| A1 | 0.00 | - | 0.15 |
| b | 0.28 | 0.35 | 0.50 |
| c | 0.08 | 0.15 | 0.22 |
| D | 2.75 | 2.9 | 3.05 |
| e | 0.90 | 0.95 | 1.00 |
| e1 | 1.80 | 1.90 | 2.00 |
| E | 2.60 | 2.80 | 3.00 |
| E1 | 1.45 | 1.6 | 1.75 |
| L | 0.60REF | | |
| L1 | 0.30 | 0.45 | 0.60 |

## Tape Information

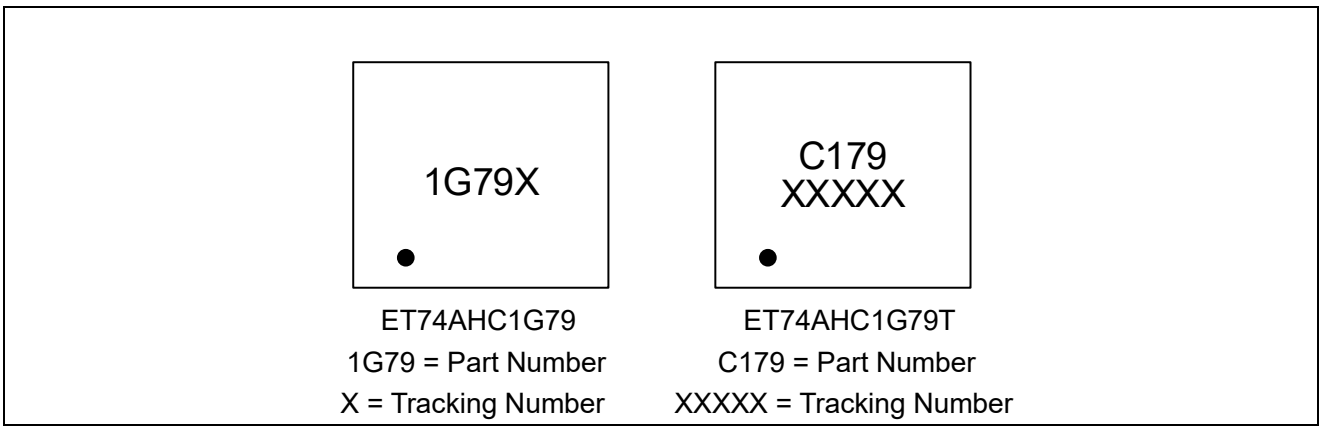
SC70-5 (1.3mm × 2.1mm)




SOT23-5 (1.6mm × 2.9mm)




## Marking Information




ET74AHC1G79
1G79 = Part Number
X = Tracking Number

ET74AHC1G79T
C179 = Part Number
XXXXX = Tracking Number

## Revision History and Checking Table

| Version | Date | Revision Item | Modifier | Function & Spec Checking | Package & Tape Checking |
|---|---|---|---|---|---|
| 1.0 | 2026-05-08 | Official Version | Xu tao | Yang xiaoxu | Liu jiaying |