Quadruple 2-Input AND Gates

General Description

The ET74AHCT08 contains four independent 2-input AND gates operating from a 4.5V to 5.5V supply.

Features

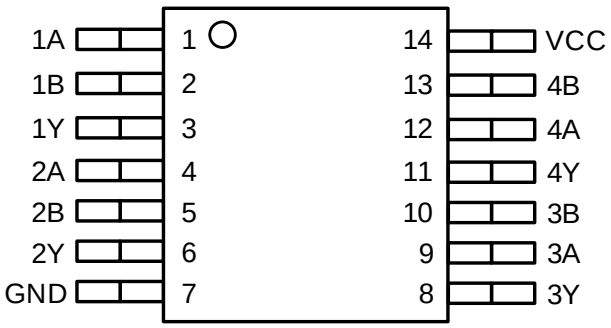
- Designed for 4.5V to 5.5V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 5.5V
- ±8mA Balanced Output Sink and Source Capability
- Near-zero Static Supply Current Substantially Reduces System Power Requirements
- These Devices are Pb-Free and RoHS Compliant
- ESD Protection Complies with JESD22 Standard
  -- HBM: ±2000V Pass (JEDEC JS-001)
  -- CDM: ±1000V Pass (JEDEC JS-002)
- Latch-up Performance Exceeds ±200mA per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET74AHCT08M	SOP14 (3.9mm × 8.65mm)	Tape and Reel, 4K/Reel	3
ET74AHCT08V	TSSOP14 (4.4mm × 5.0mm)	Tape and Reel, 4K/Reel	3

Applications

- Mobile Device

Pin Configuration



SOP14/TSSOP14

Figure1. Pin Configuration

Pin Function

Pin		I/O	Description
Name	No.		
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
1Y	3	Output	Channel 1, Output Y
2A	4	Input	Channel 2, Input A
2B	5	Input	Channel 2, Input B
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
4Y	11	Output	Channel 4, Output Y
4A	12	Input	Channel 4, Input A
4B	13	Input	Channel 4, Input B
VCC	14	—	Positive Supply

Block Diagram

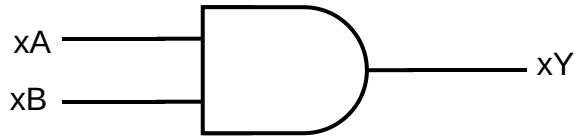


Figure2. Logic Symbol

Functional Table

Input		Output
xA	xB	xY
L	L	L
L	H	L
H	L	L
H	H	H

Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage (VCC Pin)		-0.5 to 6.5	V
I_{IK}	DC Input Diode Current, V_I < GND		-50	mA
V_I	DC Input Voltage (1)		-0.5 ≤ V_I ≤ 6.5	V
I_{OK}	DC Output Diode Current, V_O < GND		±50	mA
V_O	DC Output Voltage Output in Higher or Low State		-0.5 to V_{CC} + 0.5	V
I_O	DC Output Sink Current, V_O = 0V to V_{CC}		±50	mA
I_{CC}	DC Supply Current per Supply Pin		100	mA
I_{GND}	DC Ground Current per Supply Pin		-100	mA
T_J	Max Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-65 to 150	°C
V_{ESD}	ESD Classification	Human Body Model (2)	±2000	V
		Charged Device Model (3)	±1000	
I_{LU}	Max Latch Up Current Above V_{CC} and GND at 125°C (4)		±200	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch up Current Maximum Rating tested per JEDEC JESD78F.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage Operating	4.5	5.5	V
V_I	DC Input Voltage	0	V_{CC}	V
V_O	DC Output Voltage (High or Low State)	0	V_{CC}	V
T_A	Operating Temperature Range	-40	125	°C

Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Condition	V_{CC}(V)	T_A = 25°C			-40°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High-Level Input Voltage		4.5	2			2		V
			5.5	2			2		
V_{IL}	Low-Level Input Voltage		4.5			0.8		0.8	V
			5.5			0.8		0.8	
V_{OH}	High-Level Output Voltage	I_{OH} = -50uA	4.5	4.4	4.5		4.4		V
		I_{OH} = -8mA		3.94			3.8		
V_{OL}	Low-Level Output Voltage	I_{OL} = 50uA	4.5			0.1		0.1	V
		I_{OL} = 8mA				0.36		0.44	
I_I	Input Leakage Current	V_I = 5.5V or GND	0~5.5			±0.1		±1.0	uA
I_{OFF}	Power Off Leakage Current	V_I = 5.5V or V_O = 5.5V	0			1		10	uA
I_{CC}	Quiescent Supply Current	V_I = 5.5V or GND	5.5			1		10	uA

AC Electrical Characteristics

$t_r = t_f$ = 3ns, over recommended operating free-air temperature range, V_{CC} = 5V ± 0.5V (unless otherwise noted)

Symbol	Parameter	Condition	T_A = 25°C			-40°C ≤ T_A ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	C_L = 15pF		7	10	1.0	12	ns
t_{PHL}		C_L = 50pF		8.5	12	1.0	14	ns

Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C_{IN}	Input Capacitance	V_{CC} = 5V, V_I = 0V or V_{CC}	5	pF
C_{PD}	Power Dissipation Capacitance (5)	10MHz, V_{CC} = 5V, V_I = 0V or V_{CC}	13	pF

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

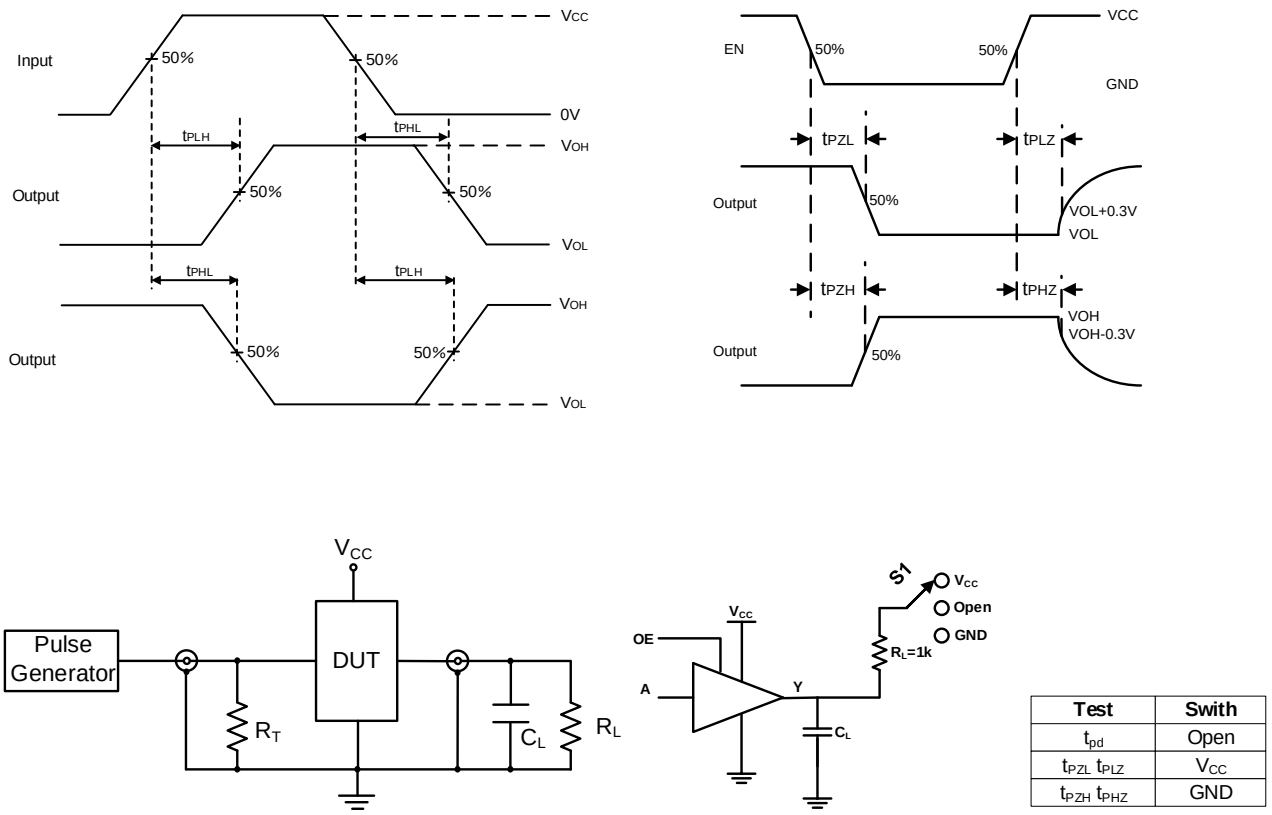
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

AC Test Circuit



Test	Swith
t_{pd}	Open
t_{PZL} t_{PLZ}	V_{CC}
t_{PZH} t_{PHZ}	GND

C_L includes probe and jig capacitance

All input pulses are supplied by generators having the following characteristics:

PRR ≤ 1MHz, Z_O = 50Ω, t_r ≤ 3ns, t_f ≤ 3ns.

The outputs are measured one at a time with one input transition per measurement.

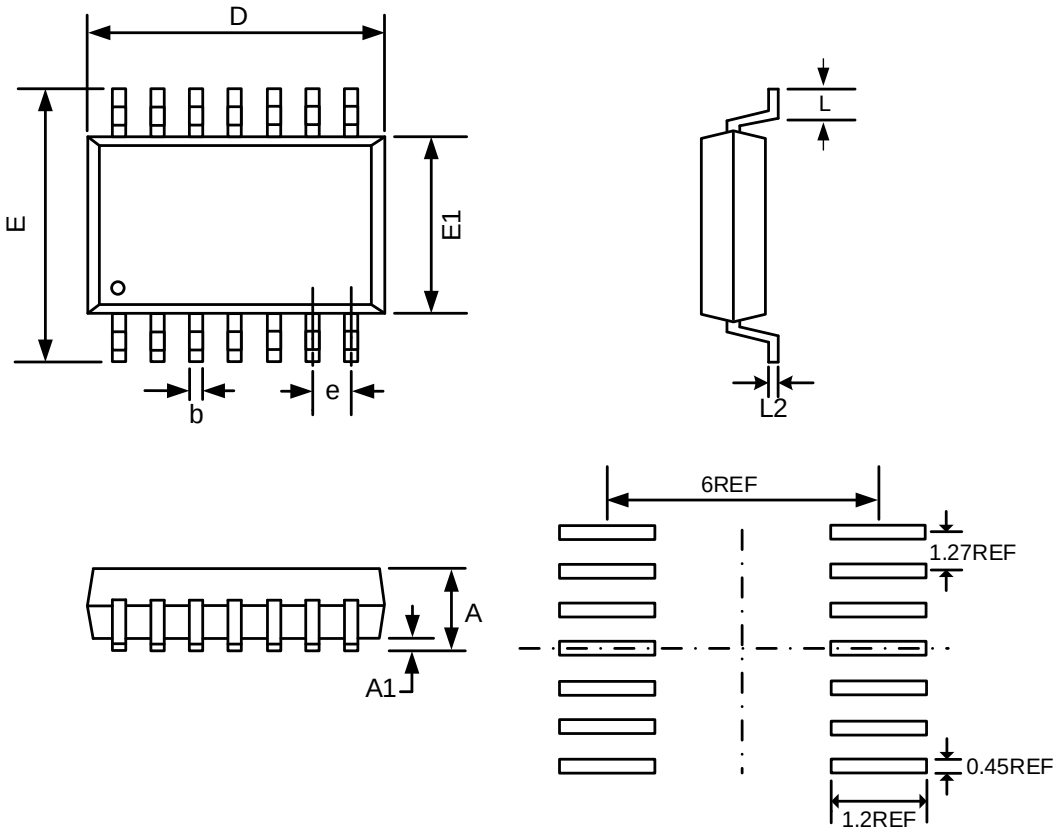
All parameters and waveforms are not applicable to all devices.

Figure3. Load Circuit and Voltage Waveforms

Note6: This electric circuit only supplies for reference. It is recommended to ground the unused I/O ports and ensure they are **not left floating**.

Package Dimension

SOP14 (3.9mm × 8.65mm)

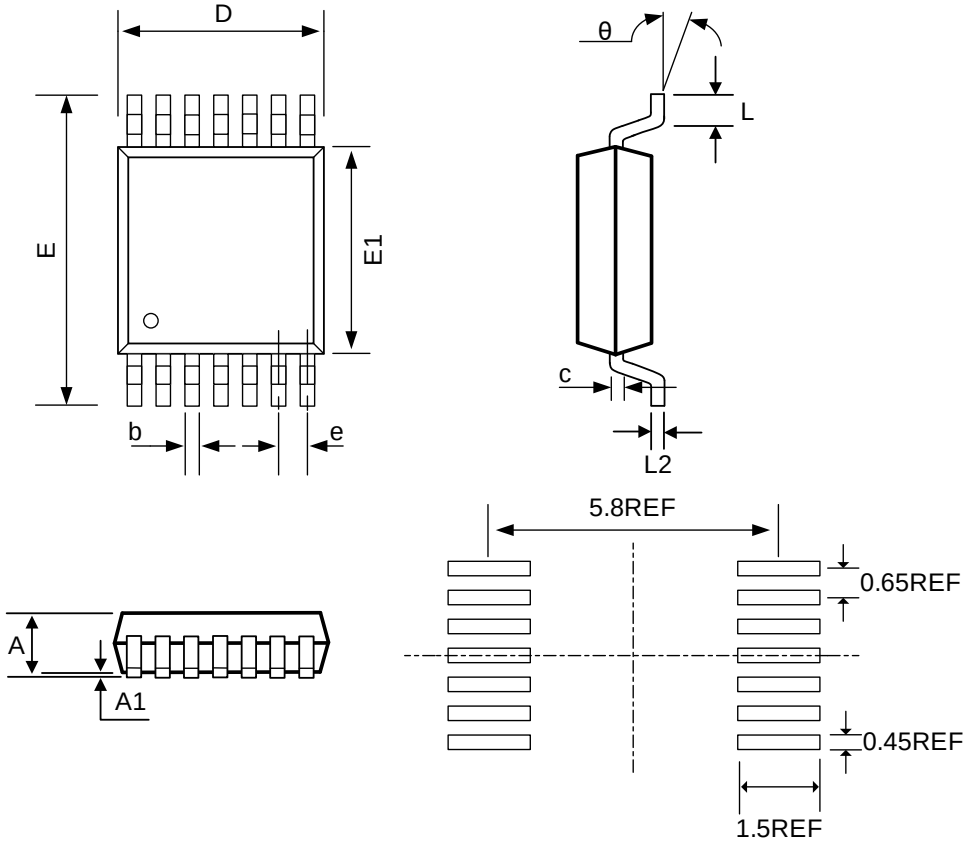


COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	MAX
A	--	1.75
A1	0.10	0.25
b	0.36	0.51
D	8.55	8.75
E	5.80	6.20
E1	3.80	4.00
e	1.22	1.32
L	0.45	0.75
L2	0.25 BSC	

TSSOP14 (4.4mm × 5.0mm)



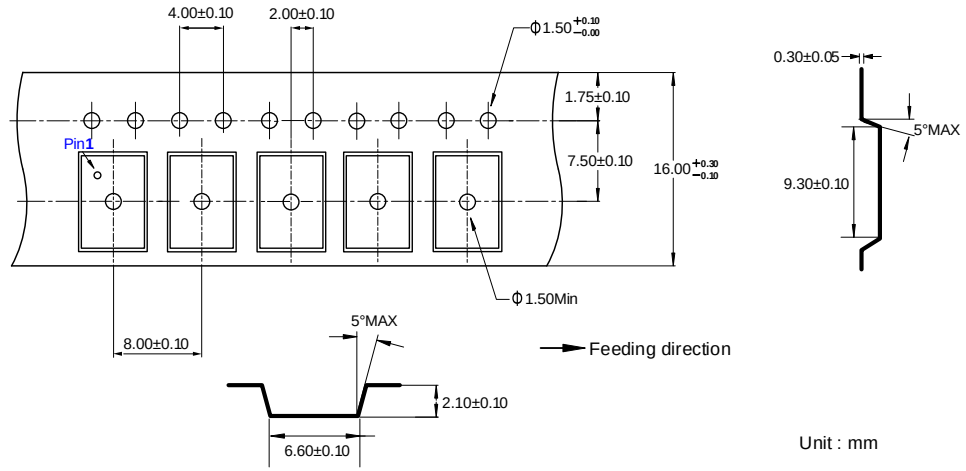
COMMON DIMENSIONS

(Unit: mm)

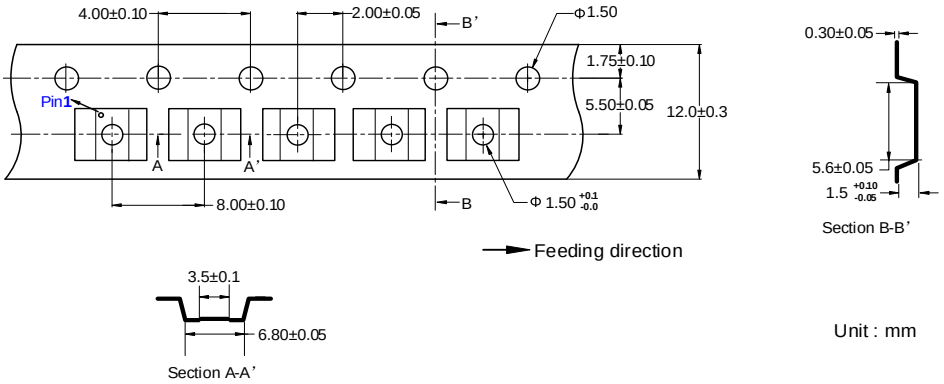
SYMBOL	MIN	MAX
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.15 REF	
D	4.86	5.10
E	6.20	6.60
E1	4.30	4.50
e	0.65BSC	
L	0.45	0.75
L2	0.25 REF	
θ	0°	8°

Tape Information

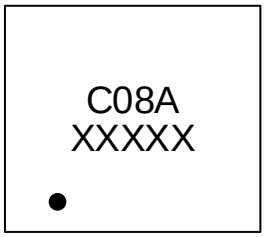
SOP14 (3.9mm × 8.65mm)



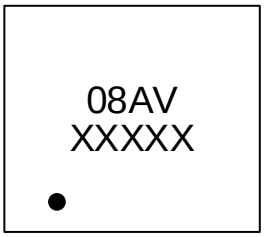
TSSOP14 (4.4mm × 5.0mm)



Marking Information



ET74AHCT08M
C08A = Part Number
XXXXX = Tracking Number



ET74AHCT08V
08AV = Part Number
XXXXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2026-03-29	Official Version	Wang anran	Yang xiaoxu	Liu jiaying