Octal Buffers/Drivers With 3-State Outputs

General Description

The ET74HC541 octal buffers/drivers is ideal for driving bus lines or buffer memory address registers. The device feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable($\overline{OE}$1 or $\overline{OE}$2) input is high, all corresponding outputs are in the high-impedance state. The outputs provide non-inverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to VCC through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Features

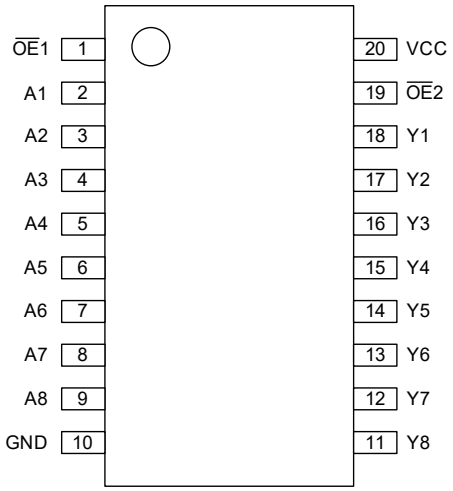
- Designed for 2V to 6V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 6V
- ±5.2mA Balanced Output Sink and Source Capability
- Inputs are TTL Voltage Compatible
- ESD Protection Complies with JESD22 Standard
  -- HBM: ±2000V Pass (JEDEC JS-001)
  -- CDM: ±1500V Pass (JEDEC JS-002)
- Latch-up Performance Exceeds ±200mA per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	MSL
ET74HC541V	TSSOP20 (6.5mm × 4.4mm)	3
ET74HC541M	SOP20 (12.75mm × 7.5mm)	3

Applications

- Fully Compliant with Standards for Automotive Applications
- Combine Normal Power Signals from Multiple Power Rails

Pin Configuration



TSSOP20/SOP20

Figure1. Pin Configuration

Pin Function

TSSOP20/SOP20

Pin No.	Pin Name	Function
1	$\overline{OE}$ 1	Output Enable 1
2	A1	Input A1
3	A2	Input A2
4	A3	Input A3
5	A4	Input A4
6	A5	Input A5
7	A6	Input A6
8	A7	Input A7
9	A8	Input A8
10	GND	Ground
11	Y8	Output Y8
12	Y7	Output Y7
13	Y6	Output Y6
14	Y5	Output Y5
15	Y4	Output Y4
16	Y3	Output Y3
17	Y2	Output Y2
18	Y1	Output Y1
19	$\overline{OE}$ 2	Output Enable 2
20	VCC	Supply Voltage

Block Diagram

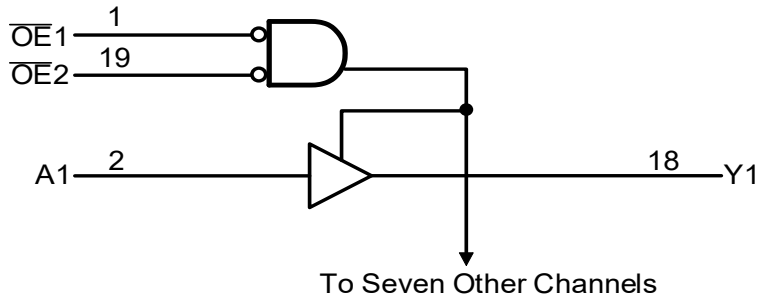


Figure2. Logic Symbol

Functional Table

Inputs			Output
$\overline{OE}$ 1	$\overline{OE}$ 2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

H = High voltage level ,

L = Low voltage level ,

X = Don't care ,

Z = High-impedance OFF-state.

Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage (VCC Pin)		-0.5 to 6.5	V
V_I	DC Input Voltage (1)		-0.5 to 6.5	V
V_O	DC Output Voltage		-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current, V_I < GND		-20	mA
I_{OK}	DC Output Diode Current, V_O < GND		-50	mA
I_O	DC Output Sink Current, V_O = 0V to V_{CC}		±35	mA
I_{CC}	DC Supply Current per Supply Pin		70	mA
I_{GND}	DC Ground Current per Supply Pin		-70	mA
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-65 to 150	°C
V_{ESD}	ESD Classification	Human Body Model (2)	±2000	V
		Charged Device Model (3)	±1500	
I_{LU}	Max Latch Up Current Above V_{CC} and GND (4)		±200	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch up Current Maximum Rating tested per JEDEC JESD78F.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage Operating		2.0	6	V
V_I	DC Input Voltage		0	6	V
V_O	DC Output Voltage		0	6	V
T_A	Operating Temperature Range		-40	125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.3V to 2.7V		200	ns/V
		V_{CC} = 3V to 3.6V		100	
		V_{CC} = 4.5V to 5.5V		20	

Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Condition	V_{CC}(V)	T_A = 25°C			-40°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High-Level Input Voltage		2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-Level Input Voltage		2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-Level Output Voltage	I_{OH} = -20μA	2	1.9	1.998		1.9		V
			4.5	4.4	4.499		4.4		
			6	5.9	5.999		5.9		
		I_{OH} = -4mA	4.5	3.98	4.3		3.84		
		I_{OH} = -5.2mA	6	5.48	5.8		5.34		
V_{OL}	Low-Level Output Voltage	I_{OL} = 20μA	2		0.002	0.1		0.1	V
			4.5		0.001	0.1		0.1	
			6		0.001	0.1		0.1	
		I_{OL} = 4mA	4.5		0.17	0.26		0.33	
		I_{OL} = 5.2mA	6		0.15	0.26		0.33	
I_I	Input Leakage Current	V_I = 6V or GND	6		±0.1	±100		±1000	nA
I_{CC}	Quiescent Supply Current	V_I = 6V or GND	6			2		20	μA

AC Electrical Characteristics

Symbol	Parameter	Condition	V_{CC}(V)	T_A = 25°C			-40°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
t_{pd}	Propagation Delay (Figure3 and 4)	C_L = 15pF	2.5		6.7	11.3	1.0	13.5	ns
			3.3		4.8	7.0	1.0	8.5	
			5		3.5	5	1.0	6	
		C_L = 50pF	2.5		8.7	15.9	1.0	18.5	
			3.3		6.1	10.5	1.0	12	
			5		4.3	7.0	1.0	8.0	
t_{en}	Enable Times (Figure3 and 4)	C_L = 15pF	2.5		8.5	16.6	1.0	19.5	
			3.3		6.1	10.5	1.0	12.5	
			5		4.3	7.2	1.0	8.5	
		C_L = 50pF	2.5		10.5	20.7	1.0	24	
			3.3		7.4	14	1.0	16	
			5		5.3	9.2	1.0	10.5	
t_{dis}	Disable Times (Figure3 and 4)	C_L = 15pF	2.5		8.4	13.1	1.0	15	
			3.3		5.8	11	1.0	12	
			5		3.9	7.5	1.0	8	
		C_L = 50pF	2.5		12.3	17.9	1.0	20	
			3.3		8.8	15.4	1.0	17.5	
			5		5.6	8.8	1.0	10	

Capacitance Characteristics

Symbol	Parameter	Conditions	Typ	Unit
C_I	Input Capacitance	V_{CC} = 6V, V_I = 0V or V_{CC}	2	pF
C_{PD}	Power Dissipation Capacitance[(5)]	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	16.3	
		10MHz, V_{CC} = 5V, V_I = 0V or V_{CC}	17.8	

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

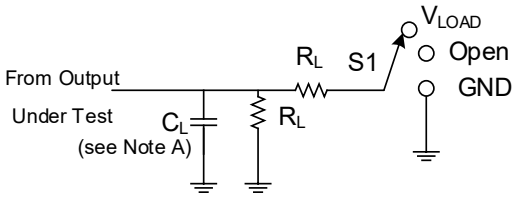
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

AC Test Circuit



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

Figure3. Test Circuit for Measuring Switching Times

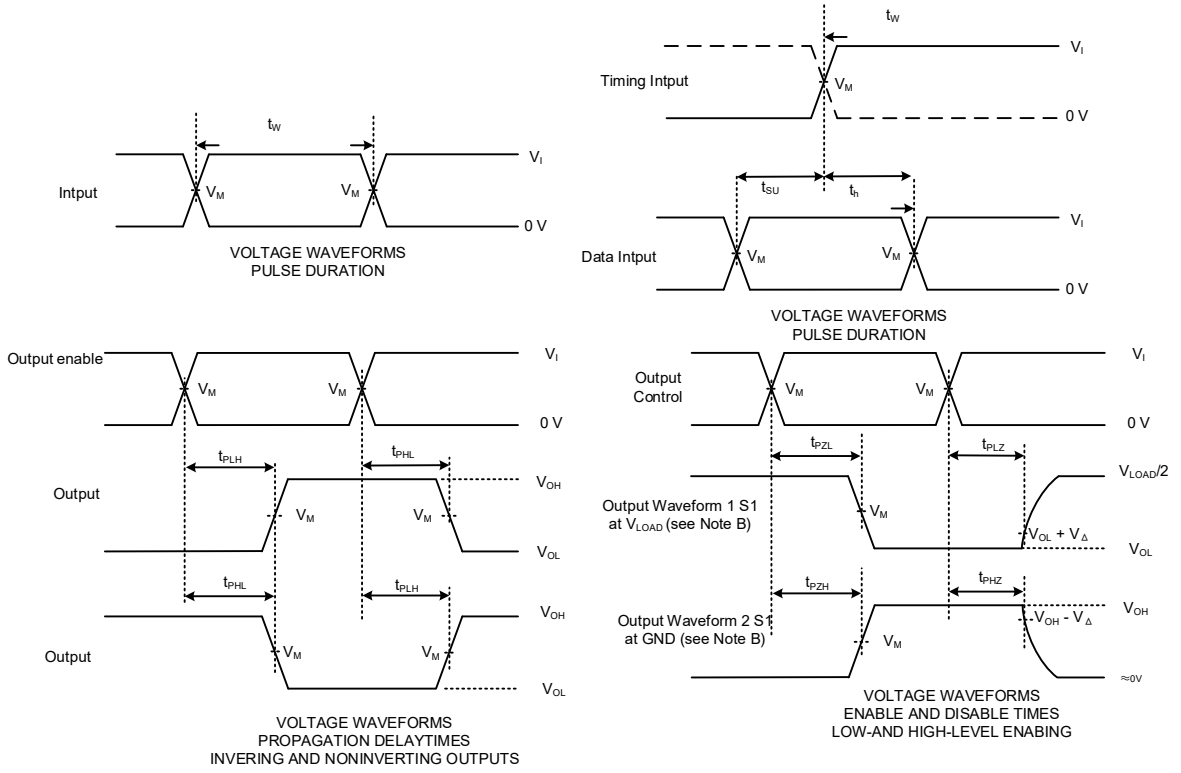


Figure4. Input to Output Propagation Delay Times

NoteA: C_L includes probe and jig capacitance.

NoteB: Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.

NoteC: Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

NoteD: All input pulses are supplied by generators having the following characteristics:

PRR ≤ 10MHz, Z_O = 50Ω

NoteE: The outputs are measured one at a time, with one transition per measurement.

NoteF: t_{PLZ} and t_{PHZ} are the same as t_{dis}.

NoteG: t_{PZL} and t_{PZH} are the same as t_{en}.

NoteH: t_{PLH} and t_{PHL} are the same as t_{pd}.

NoteI: All parameters and waveforms are not applicable to all devices.

Test Data

V_{CC}	Input		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
2.5V ± 0.2V	V_{CC}	≤ 3ns	V_{CC} / 2	2 × V_{CC}	15pF/50pF	500Ω	0.15V
3.3V ± 0.3V	V_{CC}	≤ 3ns	V_{CC} / 2	2 × V_{CC}	15pF/50pF	500Ω	0.3V
5V ± 0.5V	V_{CC}	≤ 3ns	V_{CC} / 2	2 × V_{CC}	15pF/50pF	500Ω	0.3V

Typical Application

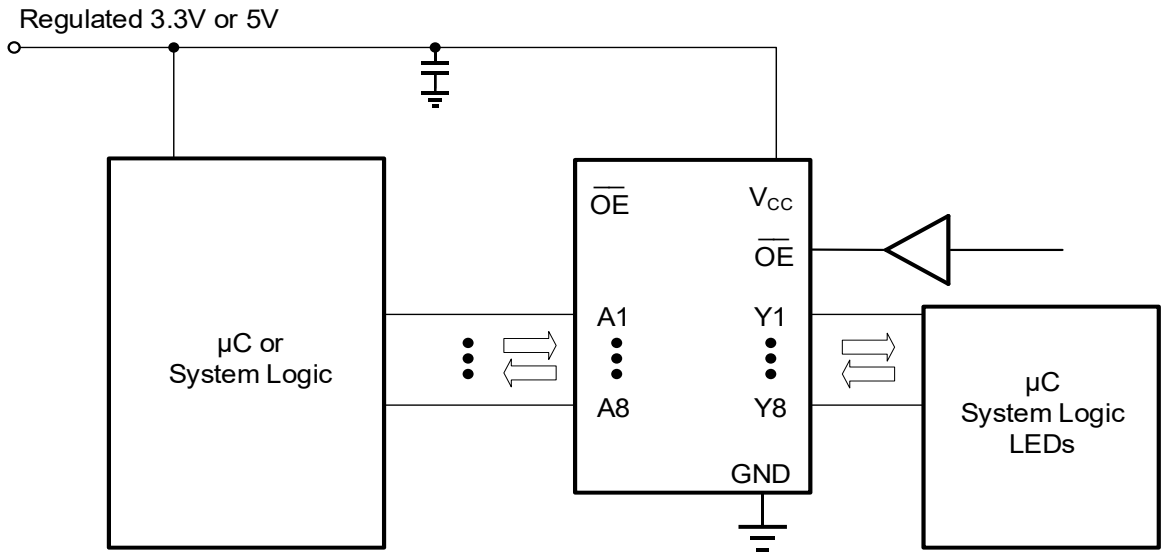
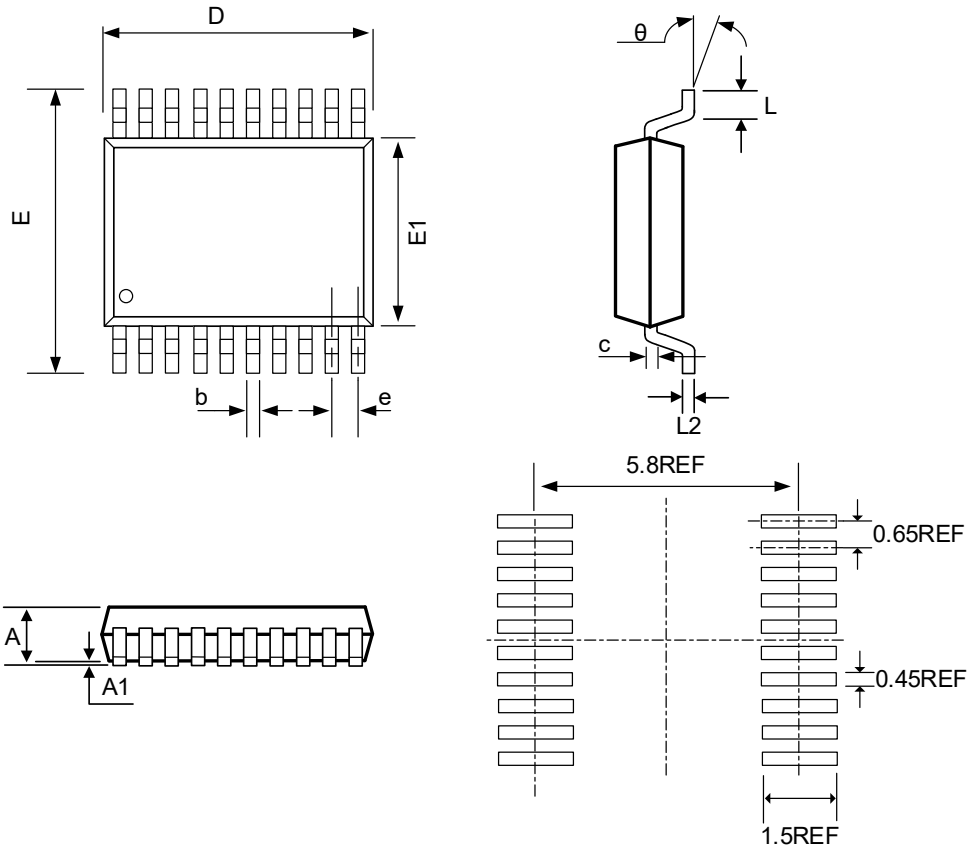


Figure5. Typical Application Schematic

Package Dimension

TSSOP20 (6.5mm × 4.4mm)

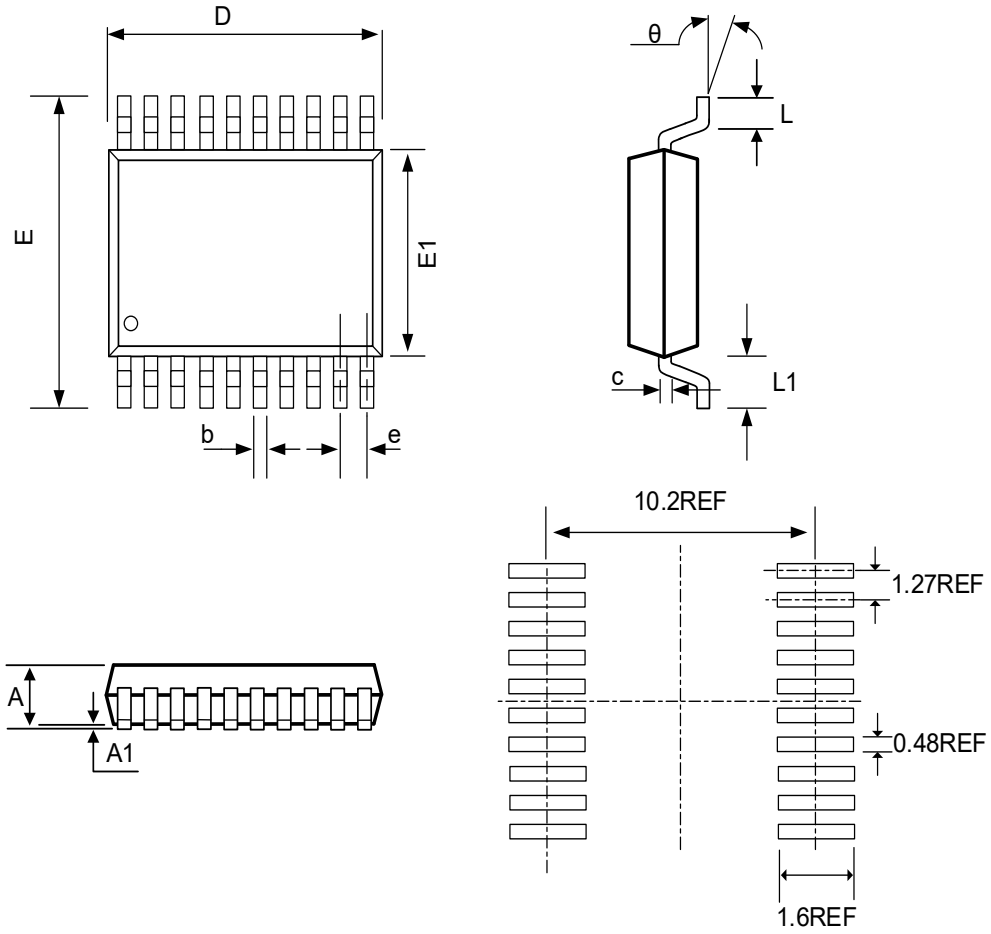


COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	MAX
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.15 REF	
D	6.40	6.60
E	6.20	6.60
E1	4.30	4.50
e	0.65BSC	
L	0.50	0.72
L2	0.25 REF	
θ	0°	8°

SOP20 (12.75mm × 7.5mm)



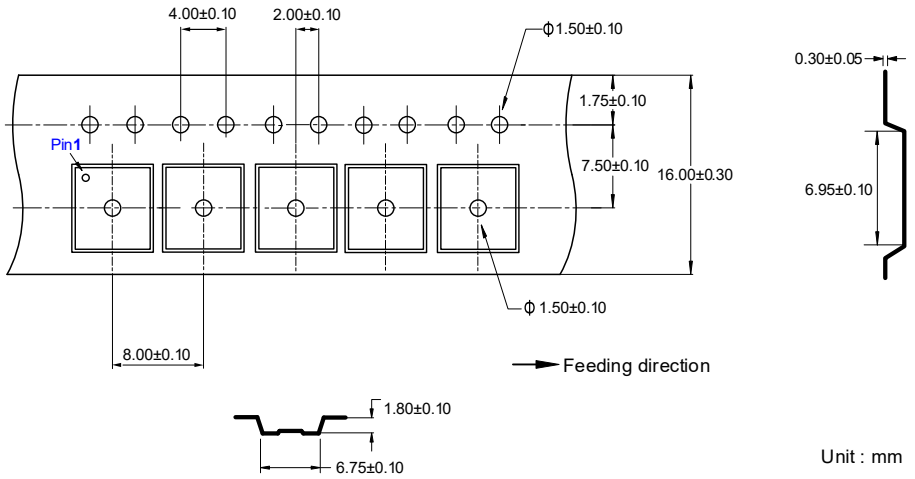
COMMON DIMENSIONS

(Unit: mm)

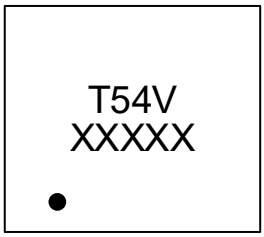
SYMBOL	MIN	MAX
A	--	2.65
A1	0.1	0.3
b	0.38	0.48
c	0.24	0.3
D	12.6	12.9
E	10.1	10.5
E1	7.4	7.6
e	1.27BSC	
L	0.6	1
L1	1.4REF	
θ	0°	8°

Tape Information

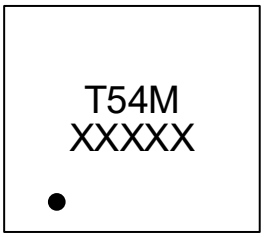
TSSOP20 (4.4mm × 6.5mm)



Marking Information



ET74HC541V
V54V = Part Number
XXXXX = Tracking Number



ET74HC541M
T54M = Part Number
XXXXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2026-03-30	Official Version	Wang anran	Yang xiaoxu	Liu jiaying