ET5HAADJ - 20V, 1A High Speed LDO

General Description

The ET5HAADJ is a high voltage ADJ type LDO with enable function, the output operates from 0.8V to 5.5V. The characteristics are low noise and good PSRR and low dropout voltage, make this device ideal for portable consumer applications.

The ET5HAADJ can operate with up to 20V input.

The Devices are available in ESOP8, DFN6 packages

Features

- Operating Input Voltage Range:2.7V~20V
- Max Output Current: 1A
- Output Voltage Accuracy: ±2%
- Adjustable Output Voltage 0.8V~5.5V with V_{FB} = 0.6V
- Standby Current: 160uA (Typ.)
- High Ripple Rejection: 80dB at 1kHz
- Low Dropout: 480mV (Typ.) at 1A @ V_{OUT} = 3.3V

Applications

- Consumer and Industrial Equipment Point of Regulation.
- Switching Power Supply Post Regulation
- Battery Chargers
- Hard Drive Controllers

Device Information

Part No.	Package	Packing Option	MSL
ET5HAADJYB	DFN6 (2.0mm × 2.0mm)	Tape and Reel, 3K/Reel	1
ET5HAADJEB	ESOP8 (4.9mm × 6.0mm)	Tape and Reel, 4K/Reel	3

Pin Configuration

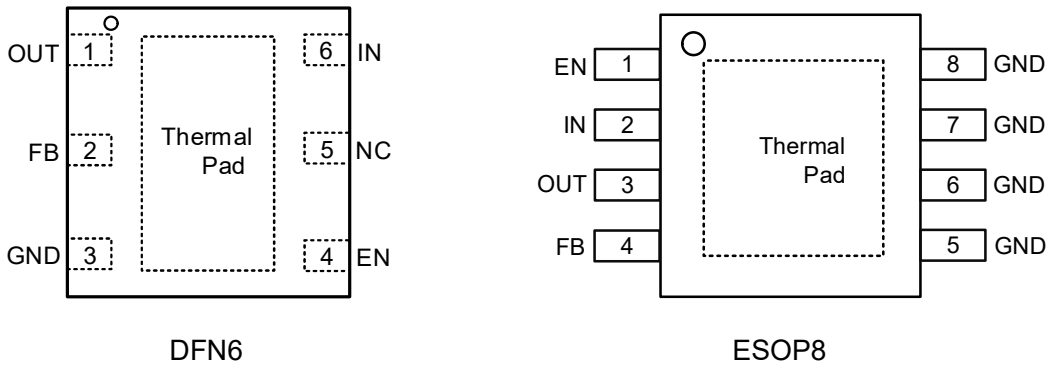


Figure1. Pin Configuration

Pin Function

DFN6

Pin Number	Pin Name	Functions
1	OUT	Output
2	FB	Set the output voltage of the LDO.
3	GND	Ground
4	EN	Enable Pin
5	NC	Not Connect
6	IN	Power Supply Input

ESOP8

Pin Number	Pin Name	Functions
1	EN	Enable Pin.
2	IN	Power Supply Input.
3	OUT	Output.
4	FB	Set the Output Voltage of the LDO.
5	GND	Ground.
6	GND	Ground.
7	GND	Ground.
8	GND	Ground.

Block Diagram

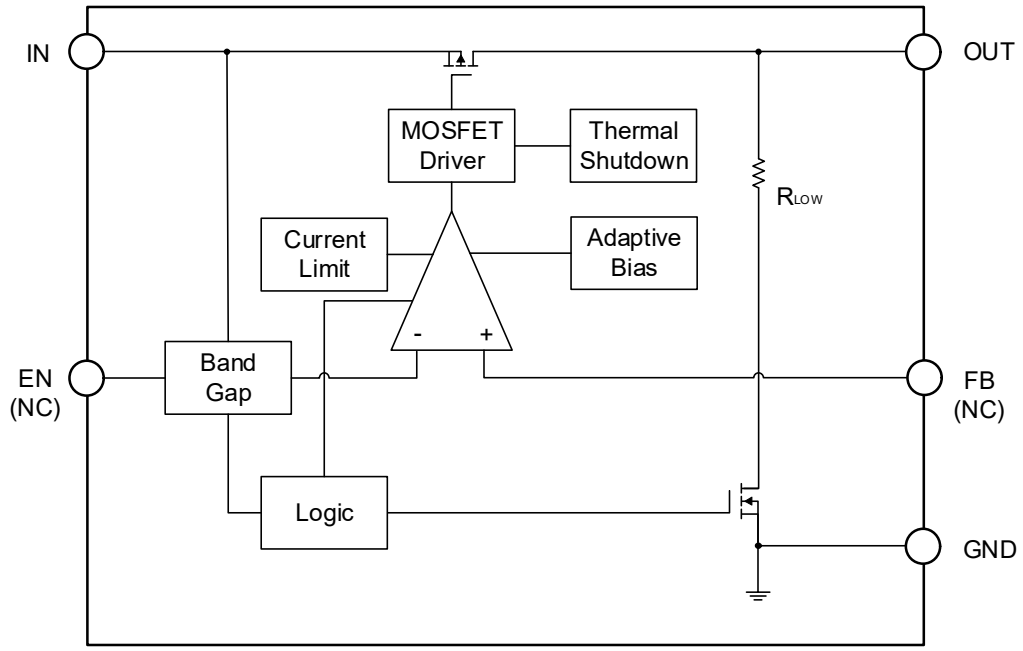


Figure2. Block Diagram

Functional Description

Input and Output Capacitor Selection

The ET5HAADJ requires an output capacitance of 4.7μF or larger for stability. Use X5R and X7R type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. When choosing a capacitor for a specific application, pay attention to the dc bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range off frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

Application of Electrolytic Capacitor

If the electrolytic capacitor should be used as input and output capacitor, the capacitance of the capacitor must be greater. The capacity value must be greater than 22uF.

Enable

The ET5HAADJ delivers the output power when it is set to enable state. When it works in disable state, there is no output power and the operation quiescent current is almost zero. The enable pin (EN) is active high.

Shutdown

Turn off the device by forcing the EN pin to drop below $V_{EN(LO)}$. If shutdown capability is not required, connect EN to IN. The ET5HAADJ has an internal pull down MOSFET that connects an $R_{PULLDOWN}$ resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the pull-down resistor (R_{PD}).

Formula 1 calculates the time constant:

$$\mathbf{t = (R_{PD} \times R_L) / (R_{PD} + R_L)} \quad (1)$$

Setting the Output Voltage

The ET5HAADJ develops a 0.6V reference voltage, V_{REF}, between the output and the adjust terminal. This voltage is applied across resistor R1 to generate a constant current. The current I_{ADJ} from the ADJ terminal could introduce DC offset to the output. Because, this offset is very small (about 0.1uA), it can be ignored.

The constant current then flows through the output set resistor R2 and sets the output voltage to the desired level. Formula 2 is used for calculating V_{OUT}:

$$\mathbf{V_{OUT} = 0.6V \times (1 + R1 / R2)} \quad (2)$$

Although I_{ADJ} is very small, R1 + R2 should be limited to less than 100KΩ for optimum performance.

Dropout Voltage

The ET5HAADJ uses a PMOS pass transistor to achieve low dropout. When (V_{IN} - V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} - V_{OUT}) approaches dropout operation.

Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 150°C.Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 125°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycle limits regulator dissipation, protecting the LDO from damage as a result of overheating. Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} - V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to 150°C maximum.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by Formula 3:

$$\mathbf{PD_{(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}} \quad (3)$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating specifications the maximum junction temperature is 150°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For DFN6 package, the thermal resistance, θ_{JA}, is 100°C/W on the test board. The maximum power dissipation at T_A = 25°C can be calculated by Formula 4:

$$\mathbf{PD_{(MAX)} = (150°C - 25°C) / (100°C/W) = 1.25W} \quad (4)$$

Layout Guide

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections in order to optimize thermal performance.
- Place thermal vias around the device to distribute heat.
- Do not place a thermal via directly beneath the thermal pad of the DRV package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input Voltage (1)	0~24	V
V_{OUT}	Output Voltage	0.8~6	V
V_{CE}	Chip Enable Input	-0.3~22	V
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65~150	°C
V_{ESD}	Human Body Model Capability (2)	±2000	V
	Charged Device Model Capability (2)	±1500	V
I_{LU}	Latch up Current Maximum Rating (2)	±200	mA

Stresses exceeding those listed in this table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: Refer to Electrical Characteristics and Application Information for Safe Operating Area.

Note2: This device series incorporates ESD protection and is tested by the following methods ESD:

HBM tested per JEDEC JS-001;

CDM tested per JEDEC JS-002;

Latch Up Current Maximum Rating tested per JEDEC JESD78F.

Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
$R_{\theta JA}$	ESOP8	Thermal Characteristics, Thermal Resistance, Junction-to-Air	150	°C/W
	DFN6		100	°C/W

Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_{IN}	Input Voltage	2.7 to 22	V
I_{OUT}	Output Current	0 to 1.0	A
T_J	Operating Junction Temperature	-40 to 125	°C
C_{IN}	Effective Input Ceramic Capacitor Value (3)	1 to 10	uF
C_{OUT}	Effective Output Ceramic Capacitor Value (3)	1 to 10	uF
ESR	Input and Output Capacitor Equivalent Series Resistance (ESR)	5 to 100	mΩ

Note3: The capacitor refers to a chip capacitor, and larger capacitance value is required if electrolytic capacitor is used.

Electrical Characteristics

V_{IN} = V_{OUT} + 1V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 10μF, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
V_{IN}	Operating Input Voltage (4)		2.7		20	V
V_{OUT}	Output Voltage	I_{OUT} = 1mA, 25°C	-2%		+2%	V
		I_{OUT} = 1mA, -40~125°C	-3%		+3%	
V_{REF}	Reference Voltage	T_A = 25°C	0.588	0.60	0.612	V
$Line_{Reg}$	Line Regulation (7)	2.8V ≤ V_{IN} ≤ 20V, I_{OUT} = 10mA		0.05	0.20	%/V
$Load_{Reg}$	Load Regulation (7)	1mA ≤ I_{OUT} ≤ 800mA, V_{IN} = V_{OUT} + 1V			40	mV
V_{DROP}	Dropout Voltage I_{OUT} = 1A, V_{IN} ≥ 2.7V (5) (7)	V_{OUT} = 1.8V		750	800	mV
		V_{OUT} = 3.3V		480	600	
		V_{OUT} = 5.0V		450	550	
	Dropout Voltage I_{OUT}=500mA, V_{IN} ≥2.7V (5) (7)	V_{OUT} = 1.8V		650	900	mV
		V_{OUT} = 3.3V		210	450	
		V_{OUT} = 5.0V		200	400	
I_{LMT}	Current Limit	V_{IN} = V_{OUT} + 1V	1.04	1.3		A
I_{SHORT}	Short Circuit Current Limit	V_{OUT} = 0V		330		mA
I_Q	Quiescent Current	I_{OUT} = 0mA, 25°C		160	190	μA
I_{Q_OFF}	Standby Current	V_{EN} = 0V, 25°C		0.1	1	μA
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage “H”	1.4			V
V_{ENL}	EN Pin Threshold Voltage	EN Input Voltage “L”			0.4	V
I_{EN}	EN Pin Current	V_{EN} ≤ V_{IN} ≤ 20V		1		uA
PSRR	Power Supply Rejection Ratio V_{IN} = V_{OUT} + 2V I_{OUT} = 50mA	f = 1kHz		80		dB
		f = 100kHz		70		
		f = 1MHz		65		
e_N	Output Noise Voltage (4) (5)	V_{IN} = V_{OUT} + 1V, I_{OUT} = 1mA, f = 10Hz to 100KHz, V_{OUT} = 3V, C_{OUT} = 1μF		30* V_{OUT}		μVrms
R_{LOW}	Active Output Discharge Resistance	V_{IN} = 4V, V_{EN} = 0V		300		Ω
T_{SD}	Thermal Shut down Temperature (6)	Temperature Increasing from T_A = 25°C		150		°C
T_{SDH}	Thermal Shutdown Hysteresis (6)	Temperature Falling from T_{SD}		25		°C

Note4: V_{IN} range guarantees internal circuit can work normal.

If $V_{IN} < V_{OUTSET}$, V_{OUT} follows V_{IN}(I_{OUT} = 1mA), circuit is safe still.

Note5: The minimum operating voltage is 2.7V. $V_{DROP} = V_{IN(min)} - V_{OUT}$.

V_{DROP} FT test method: Test the V_{OUT} voltage at $V_{OUTSET} + V_{DROP-MAX}$ with 1A output current.

Note6: Guaranteed by design, not an FT item.

Note7: At high temperatures, the maximum load current can be calculated according to the following formula:

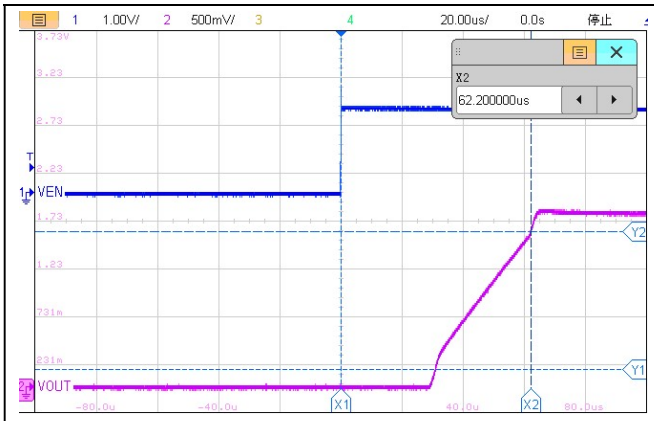
$$\mathbf{I_{OUT_MAX} = (T_J - T_A) / R_{\theta JA} / (V_{IN} - V_{OUT})}$$

Typical Characteristics

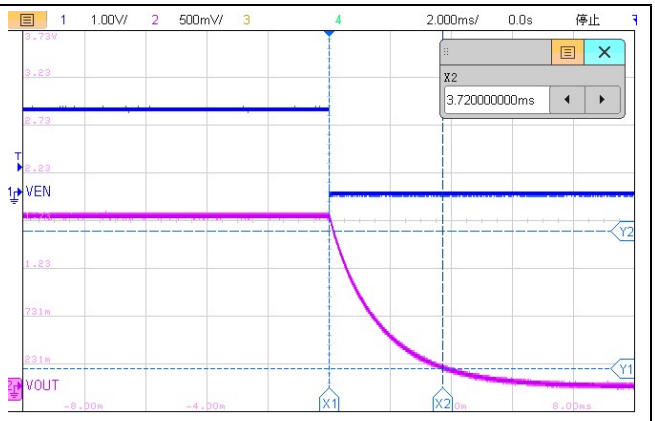
Typical Characteristics only for reference, thus they are not guaranteed.in practical use.

V_{IN} = V_{OUT} + 1V, I_{OUT} = 1mA, C_{IN} = C_{OUT} = 10μF (Ceramic Cap), unless otherwise noted.

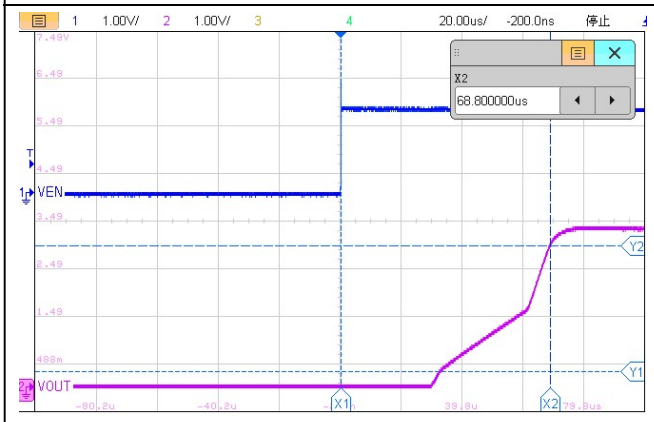
t_{ON} and t_{OFF}



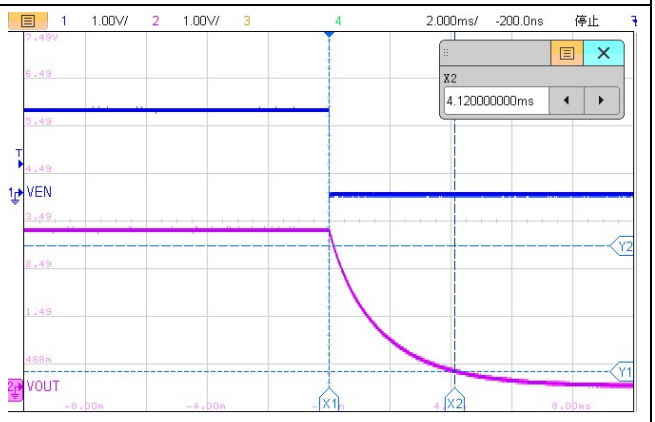
t_{ON} (V_{OUT} = 1.8V, I_{OUT} = 0mA)



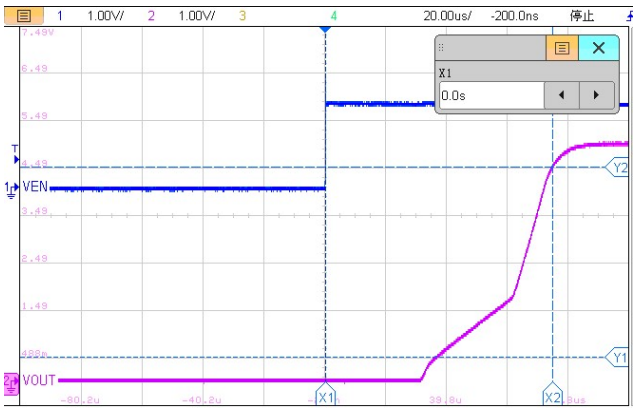
t_{OFF} (V_{OUT} = 1.8V, I_{OUT} = 0mA)



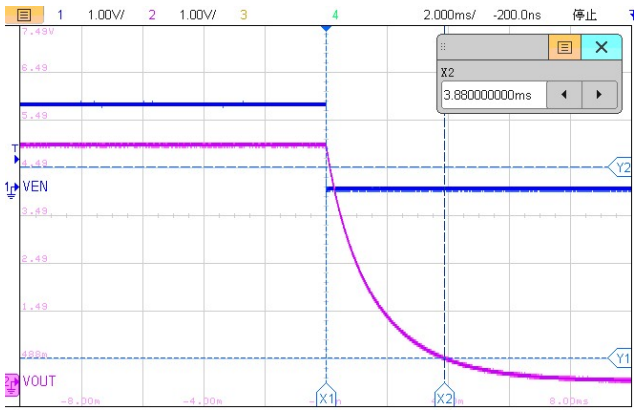
t_{ON} (V_{OUT} = 3.3V, I_{OUT} = 0mA)



t_{OFF} (V_{OUT} = 3.3V, I_{OUT} = 0mA)

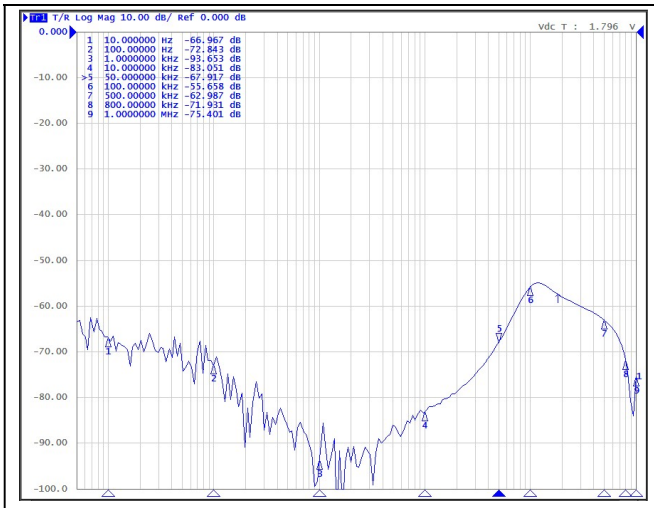


t_{ON} (V_{OUT} = 5.0V, I_{OUT} = 0mA)

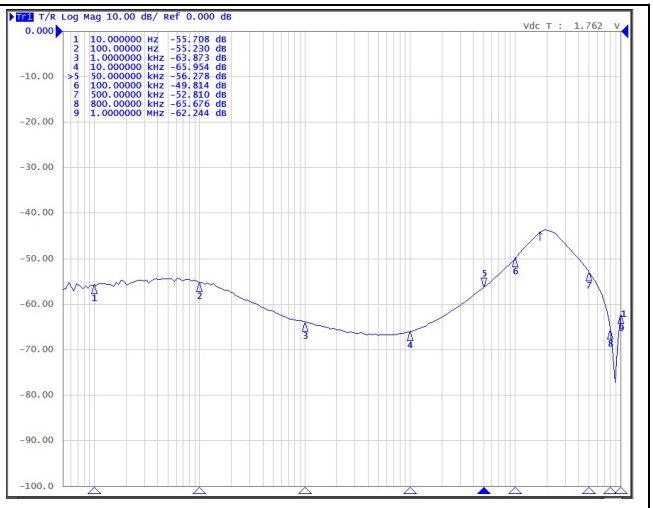


t_{OFF} (V_{OUT} = 5.0V, I_{OUT} = 0mA)

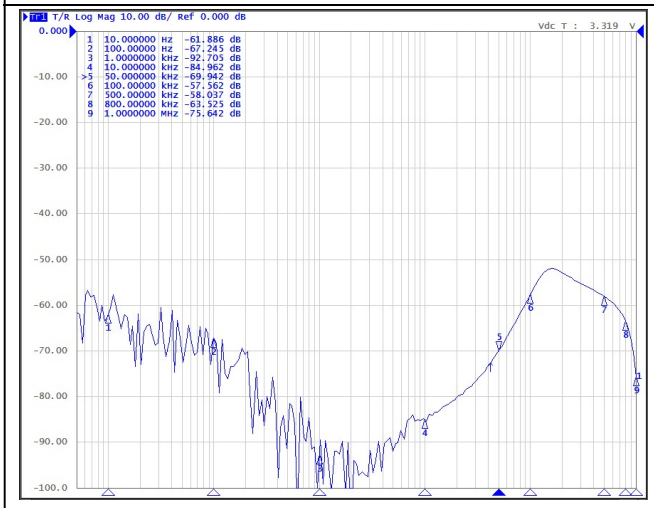
PSRR



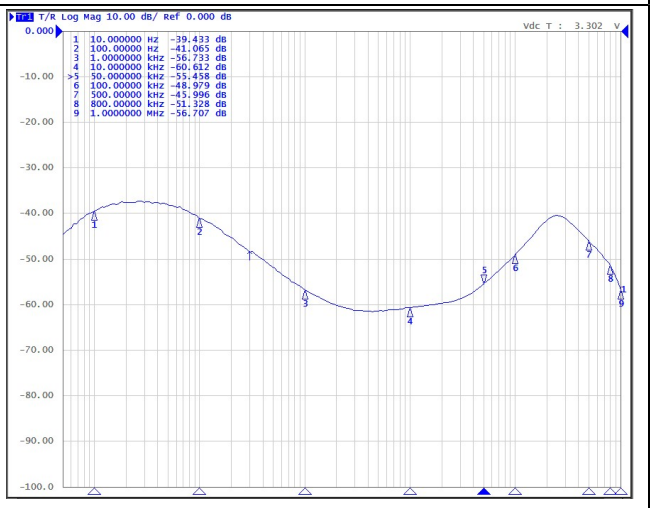
PSRR (V_{OUT} = 1.8V, I_{OUT} = 50mA)



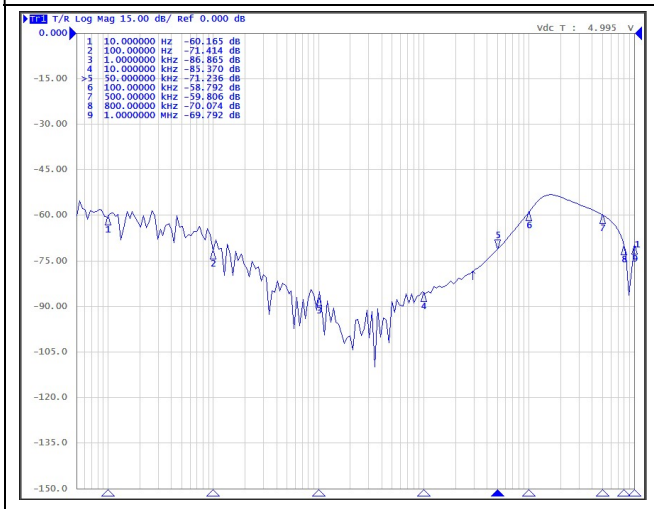
PSRR (V_{OUT} = 1.8V, I_{OUT} = 500mA)



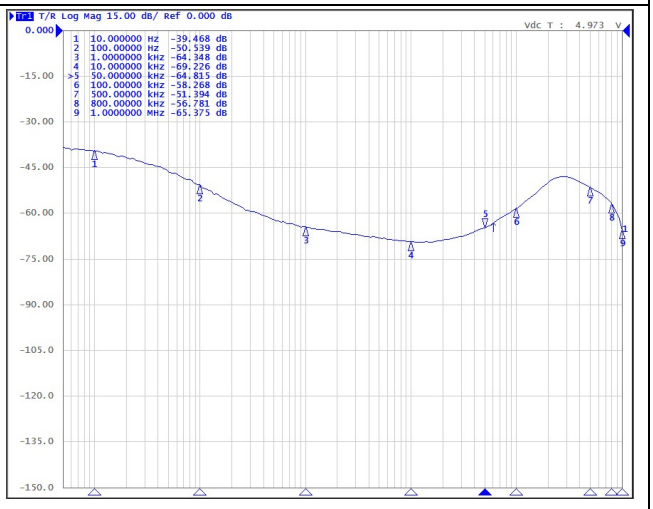
PSRR (V_{OUT} = 3.3V, I_{OUT} = 50mA)



PSRR (V_{OUT} = 3.3V, I_{OUT} = 500mA)



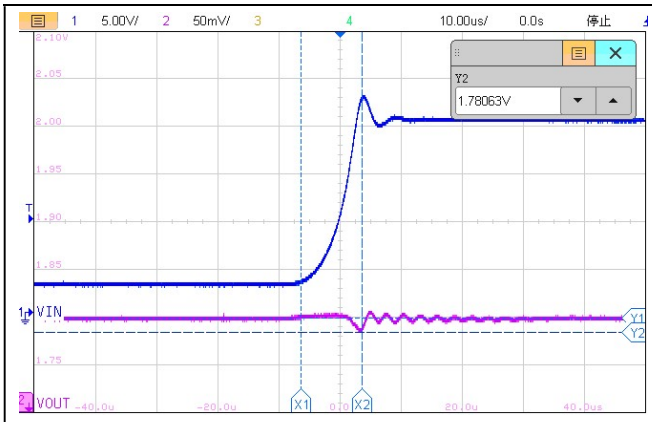
PSRR (V_{OUT} = 5.0V, I_{OUT} = 50mA)



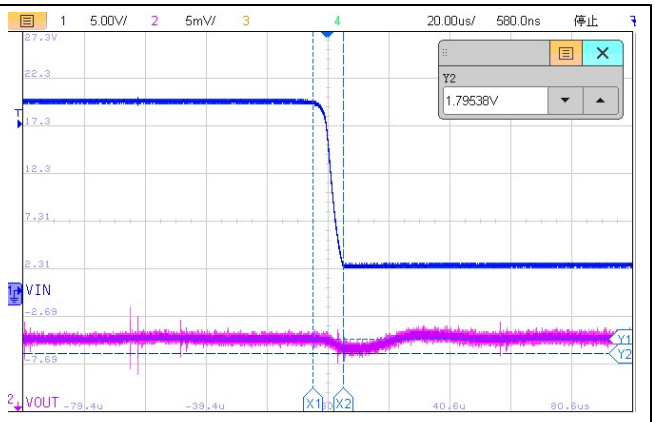
PSRR (V_{OUT} = 5.0V, I_{OUT} = 500mA)

Line Transient Response

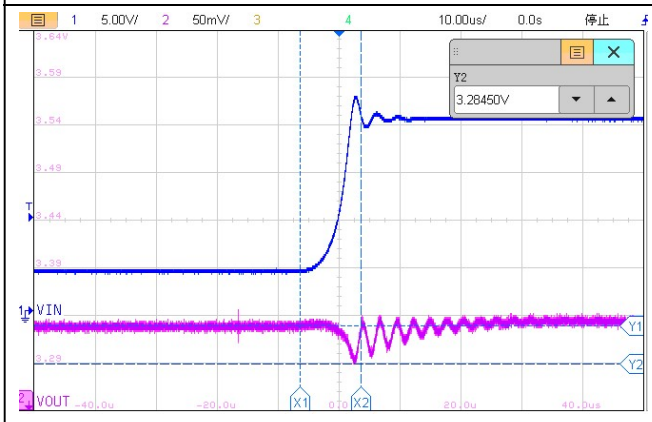
Test Condition: V_{IN} = V_{OUT} + 1V, C_{OUT} = 10μF, t_R = T_F = 10us, I_{OUT} = 1mA, V_{IN} step between 6V~18V.



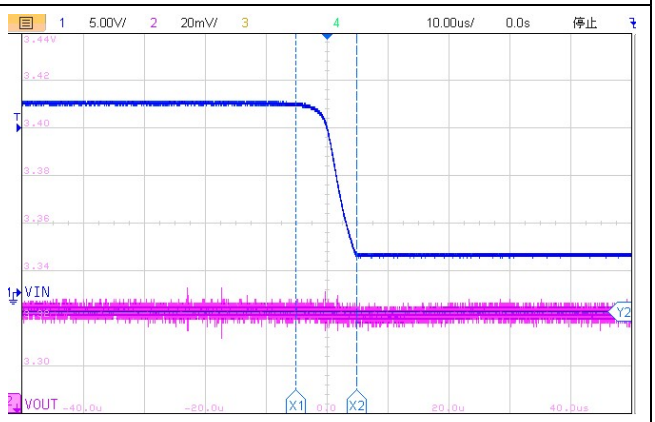
Line Transient Response
(V_{OUT} = 1.8V, I_{OUT} = 1mA)



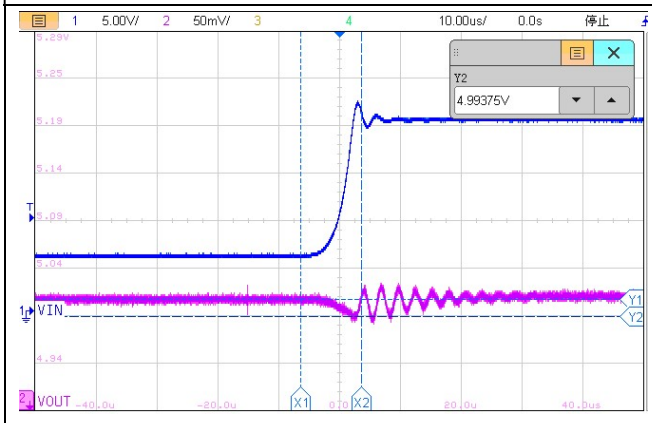
Line Transient Response
(V_{OUT} = 1.8V, I_{OUT} = 1mA)



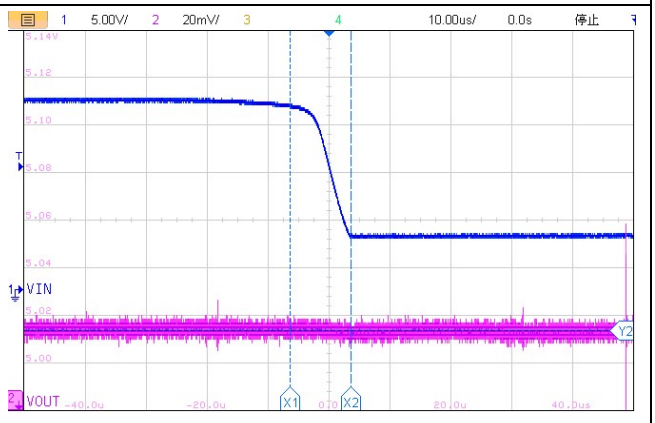
Line Transient Response
(V_{OUT} = 3.3V, I_{OUT} = 1mA)



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(V_{OUT} = 3.3V, I_{OUT} = 1mA)



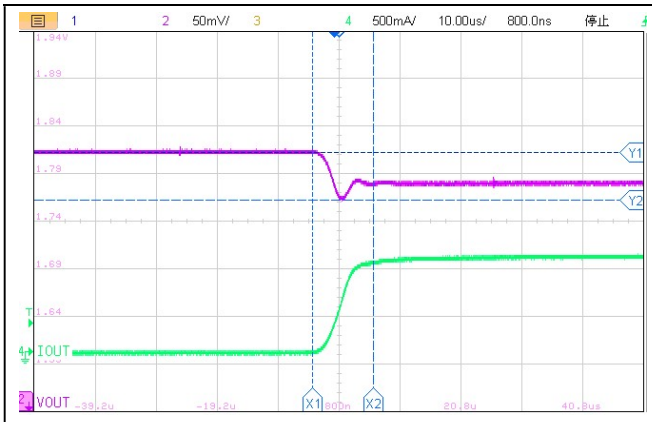
Line Transient Response
(V_{OUT} = 5.0V, I_{OUT} = 1mA)



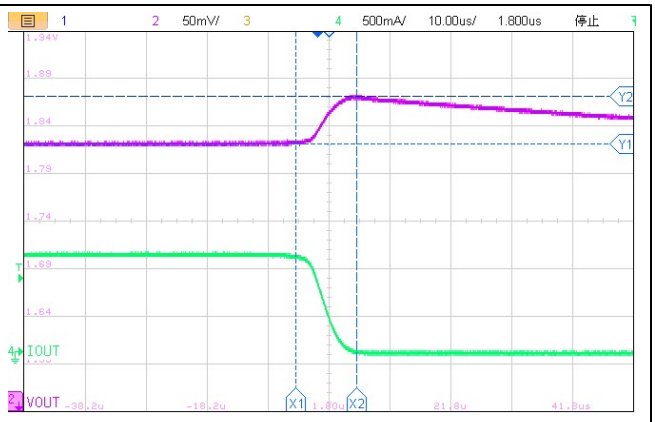
Line Transient Response
(V_{OUT} = 5.0V, I_{OUT} = 1mA)

Load Transient Response

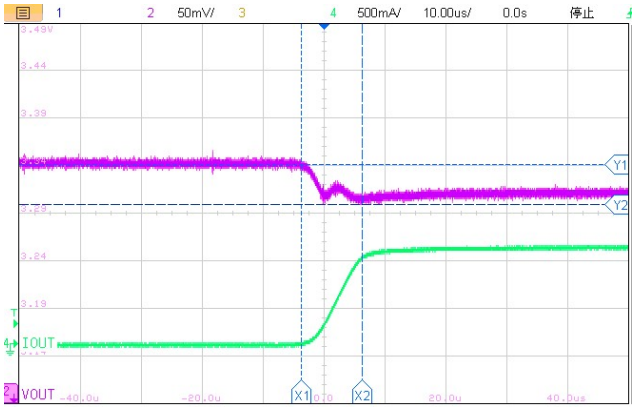
Test Condition: V_{IN} = V_{OUT} + 1V, t_R = T_F = 10us, I_{OUT} step between 1mA~1000mA.



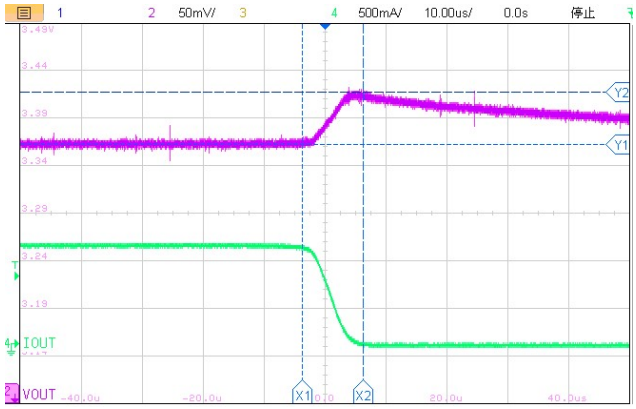
Load Transient Response
(V_{OUT} = 1.8V, I_{OUT} = 1~1000mA)



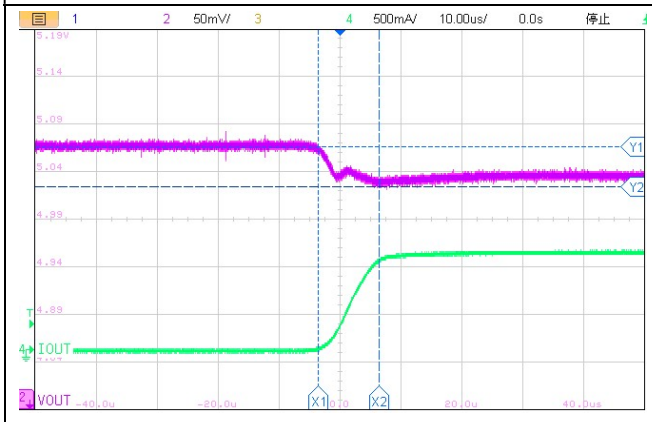
Load Transient Response
(V_{OUT} = 1.8V, I_{OUT} = 1~1000mA)



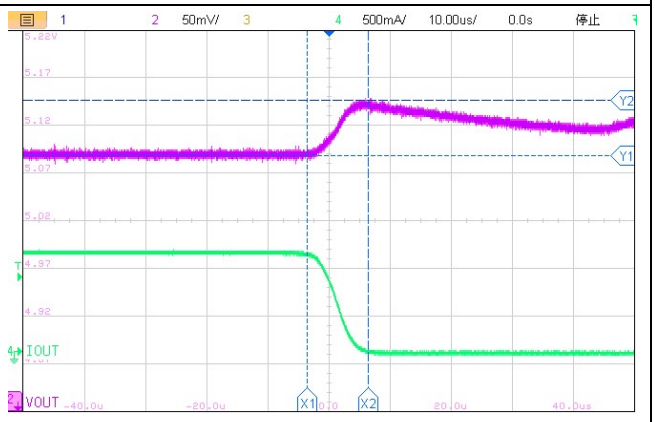
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(V_{OUT} = 3.3V,I_{OUT} = 1~1000mA)



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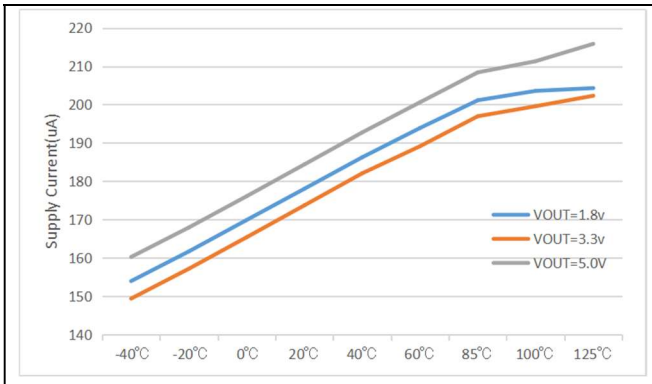


Load Transient Response
(V_{OUT} = 5.0V, I_{OUT} = 1~1000mA)

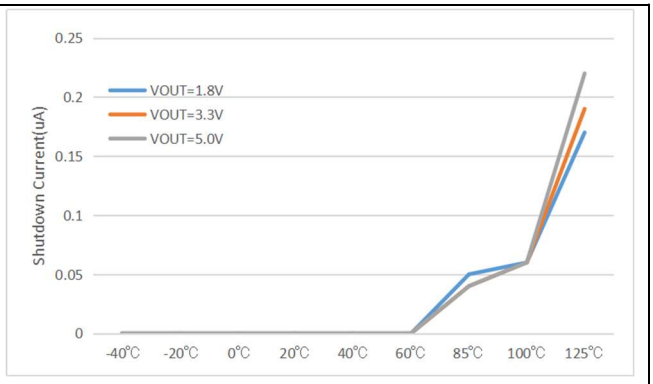


Load Transient Response
(V_{OUT} = 5.0V, I_{OUT} = 1~1000mA)

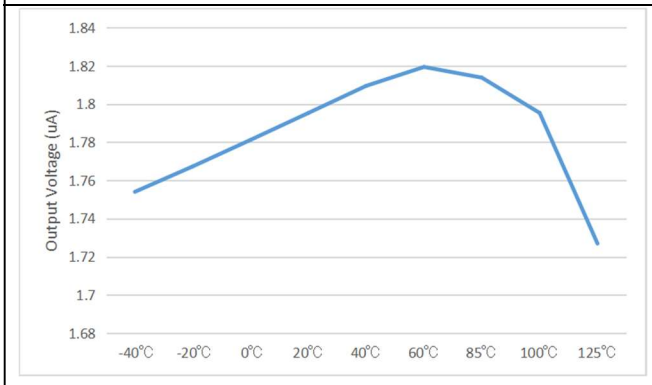
Temperature Characteristics



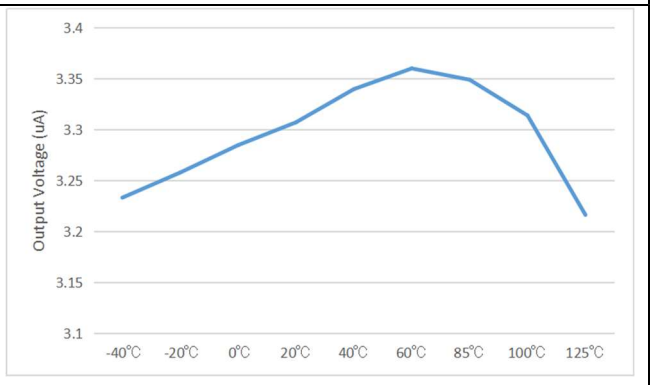
Supply Current vs. Temperature



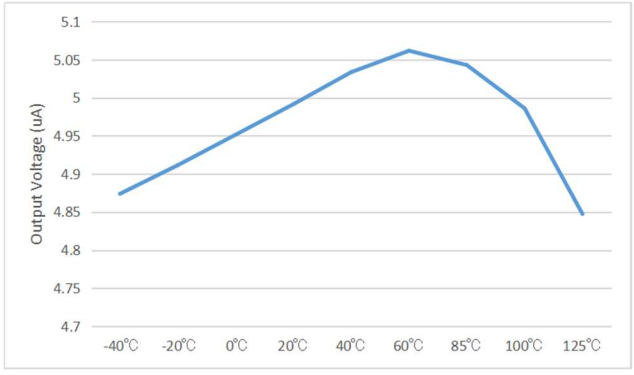
Shutdown Current vs. Temperature



Output Voltage vs. Temperature (V_{OUT}=1.8V)

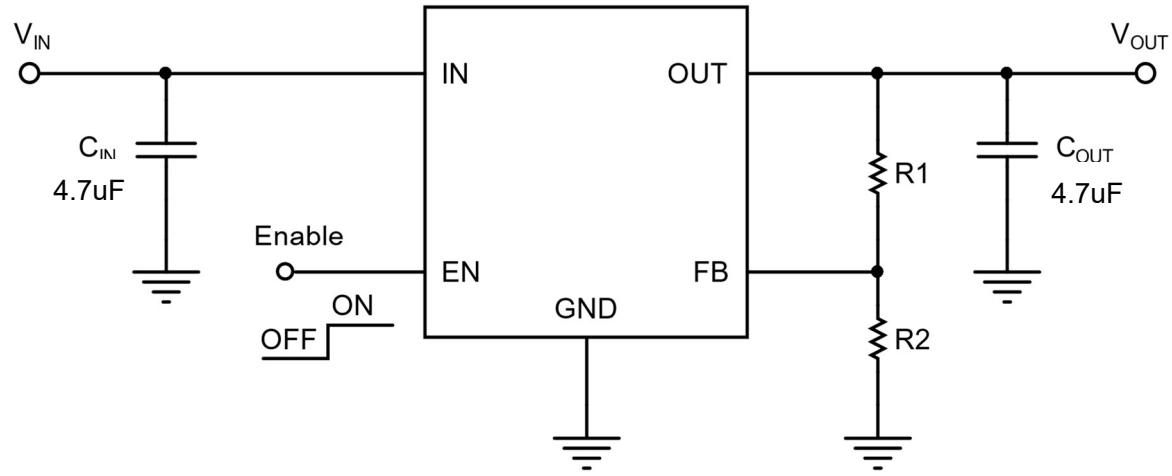


Output Voltage vs. Temperature (V_{OUT} = 3.3V)



Output Voltage vs. Temperature (V_{OUT} = 5.0V)

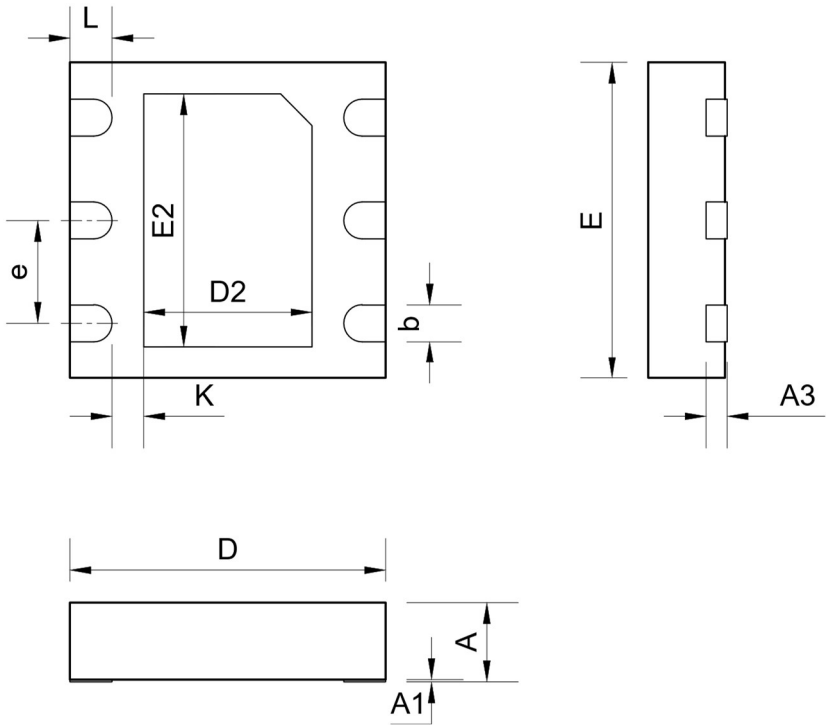
Application Circuits



V_{OUT} = 0.6V × (1 + R1 / R2)

Package Dimension

DFN6 (2.0mm × 2.0mm)



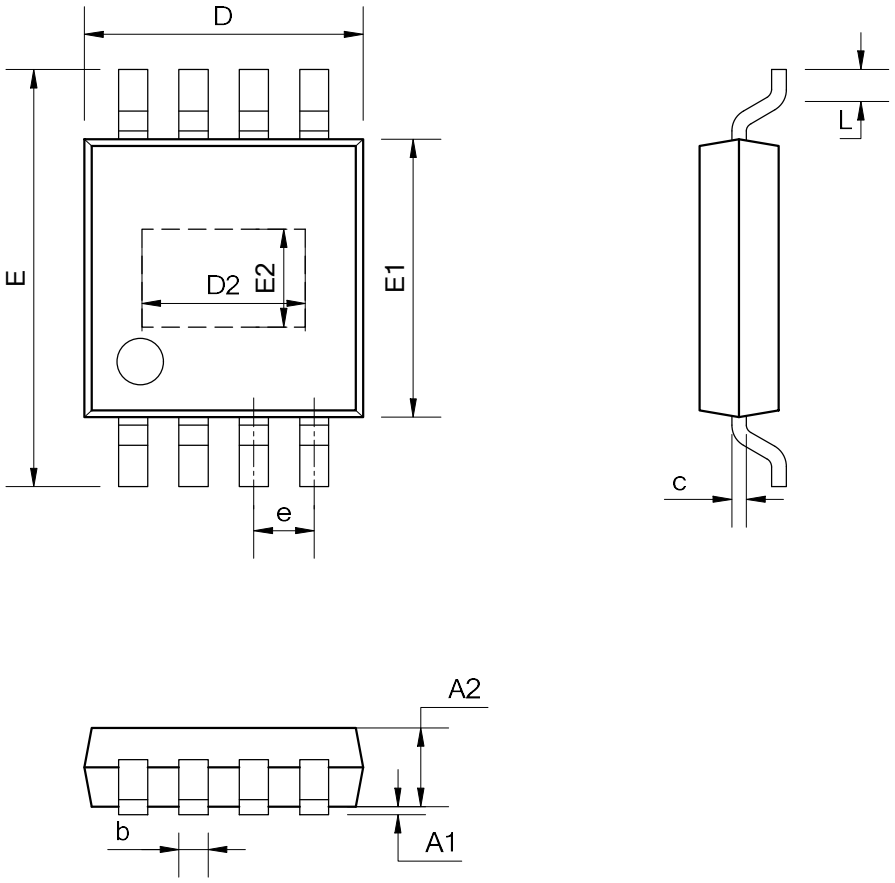
COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.25	0.35	0.45
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.65	0.80	0.90
E2	1.35	1.50	1.60
e		0.65BSC	
L	0.30	0.35	0.40
k	0.20	--	--

Package Dimension (Continued)

ESOP8 (4.9mm × 6.0mm)



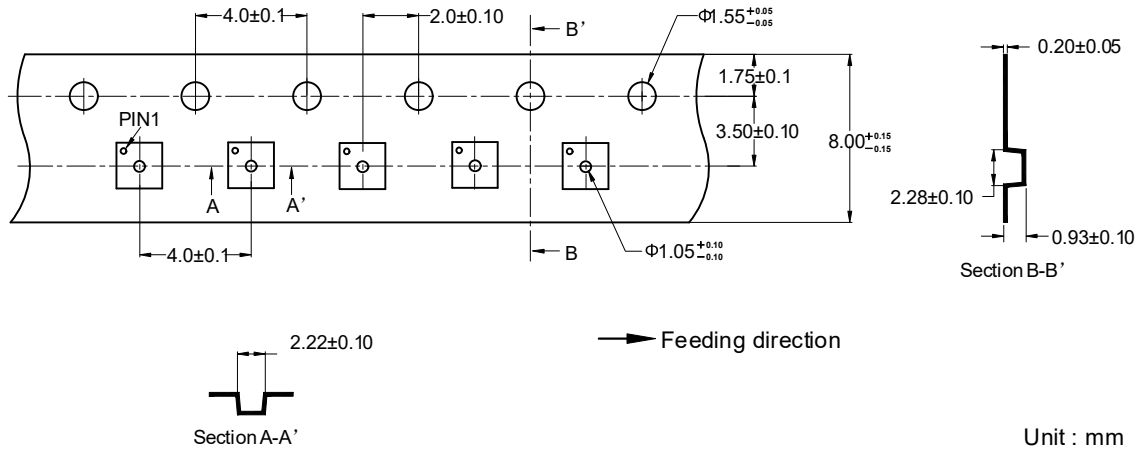
COMMON DIMENSIONS

(Unit: mm)

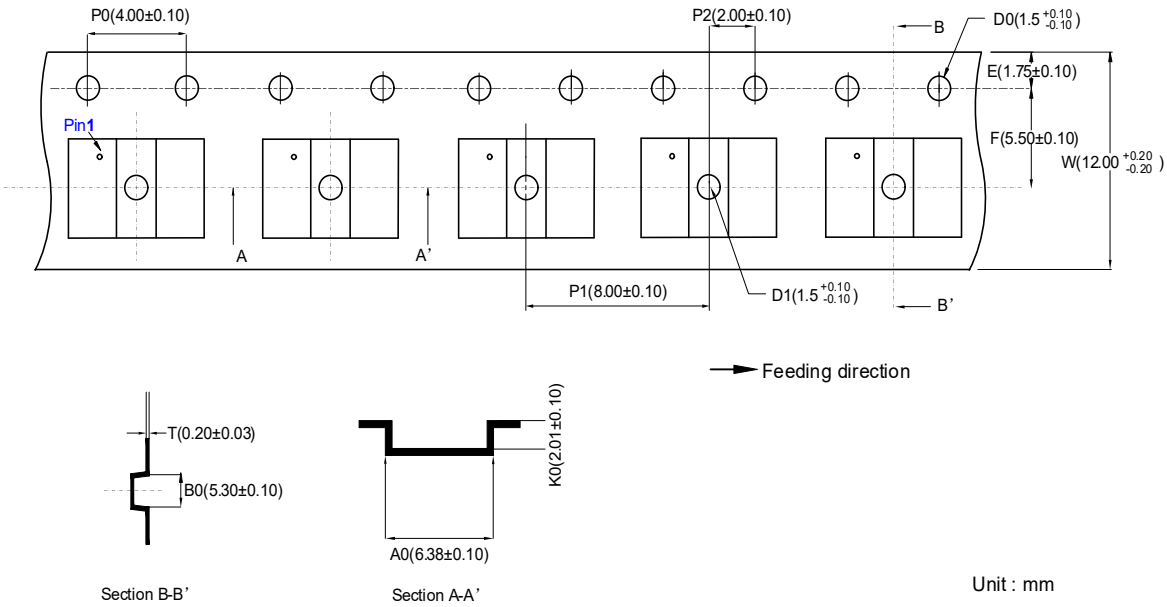
SYMBOL	MIN	NOM	MAX
A1	0.00	-	0.30
A2	1.20	1.40	1.60
b	0.35	-	0.47
c	0.15	-	0.27
D	4.70	4.90	5.10
E	5.80	6.00	6.20
D2	3.00	3.25	3.50
E1	3.70	3.90	4.10
E2	2.10	2.30	2.50
e	1.27 TYP		
L	0.35	0.60	0.85

Tape Information

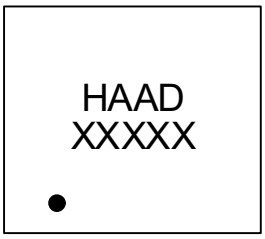
DFN6 (2.0mm × 2.0mm)



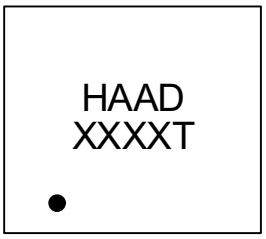
ESOP8 (4.9mm × 6.0mm)



Marking Information



ET5HAADJYB
HAAD = Part Number
XXXXX = Tracking Number



ET5HAADJEB
HAAD = Part Number
XXXXT = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2021-9-28	Preliminary Version	Shibo	Liuxiaomin	Liujy
1.0	2021-11-21	Initial Version	Shibo	Yuangr	Zhujl
1.1	2023-3-28	Update Typeset	Shibo	Yuangr	Zhujl
1.2	2024-8-20	Ton Toff to ton toff	Shibo	Liu xiaomin	Liujy
1.2.a	2025-9-23	Update package	Yang xiaoxu	Yang xiaoxu	Liujy
1.2.b	2026-07-21	Update Recommended Operating Conditions	Yang xiaoxu	Yang xiaoxu	Liujy
1.2.c	2026-08-18	Add Tape and Marking	Xu tao	Yang xiaoxu	Liujy
1.3	2026-08-27	Update MSL Level	Yang xiaoxu	Yang xiaoxu	Liujy