ET61L128 - Constant Current Matrix LED Controller

General Description

ET61L128 is a constant current LED matrix drive control dedicated circuit, the maximum support 16×8 array display; The communication mode is the standard I²C communication interface, and also supports continuous read and write function. Internal integration of a number of registers can set a variety of display effects, single point support 256-level brightness adjustment, mainly used in home appliances display drivers. Available in QFN32 or LQFP32 package form.

Features

- Supply voltage 2.7V to 5.5V
- The maximum application matrix is 16×8，maximum drive 128 leds
- 16 constant current driver channels, max output current 49.2mA
- With an external resistor, the current output can be adjusted
- The overall current supports 32 adjustment
- Each constant channel supports 4 adjustment
- Each circuit has 256 order PWM current adjustment function
- I²C interface, four chip-address can be set
- Open and short circuit detection function
- Soft shutdown function/external hardware off function
- Spread spectrum function
- Blanking function

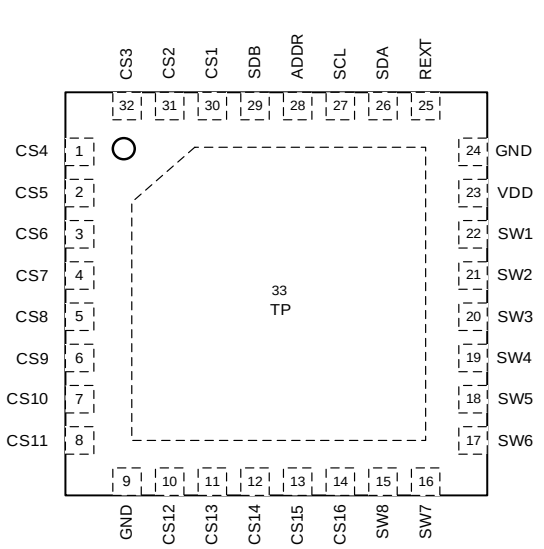
Device Information

Part No.	Package	Size
ET61L128Y1	QFN32	4mm × 4mm
ET61L128Q	LQFP32	7mm × 7mm

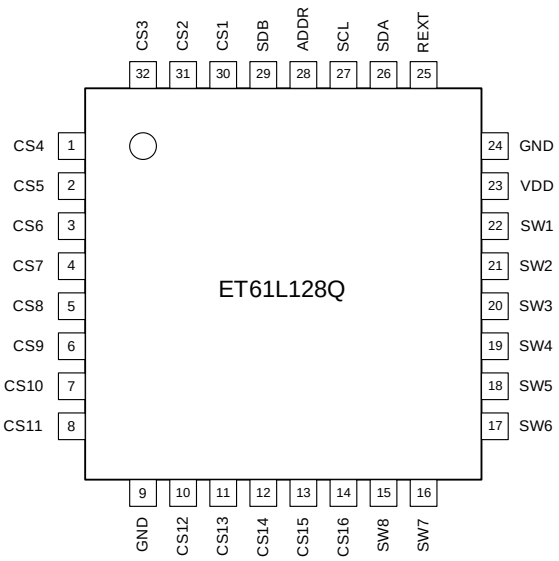
Application

- Household appliances, Toy display
- Smart portable devices, Smart audio

Pin Assignments



ET61L128Y1(QFN32)



ET61L128Q(LQFP32)

Figure 1. Pin Assignments (Top View)

Pin. Function

Pin No. QFN32/LQFP32	Name	Function
1~8,10~14	CS4~CS16	Constant current input port, connected to LED cathode
9,24	GND	GND
15~22	SW8~SW1	Current output port, connected to the LED anode
23	VDD	Supply voltage
25	REXT	Connect the input end of the external resistor; 10KΩ recommended,the resistor can set the output current of all output channels.
26	SDA	I^2C data serial input/output port
27	SCL	I^2C clock serial input port
28	ADDR	Chip-address select
29	SDB	Shutdown the chip when pulled low
30~32	CS1~CS3	Constant current input port, connected to LED cathode
33(QFN32)	TP	Thermal Pad, Connect to GND or floating

Block Diagram

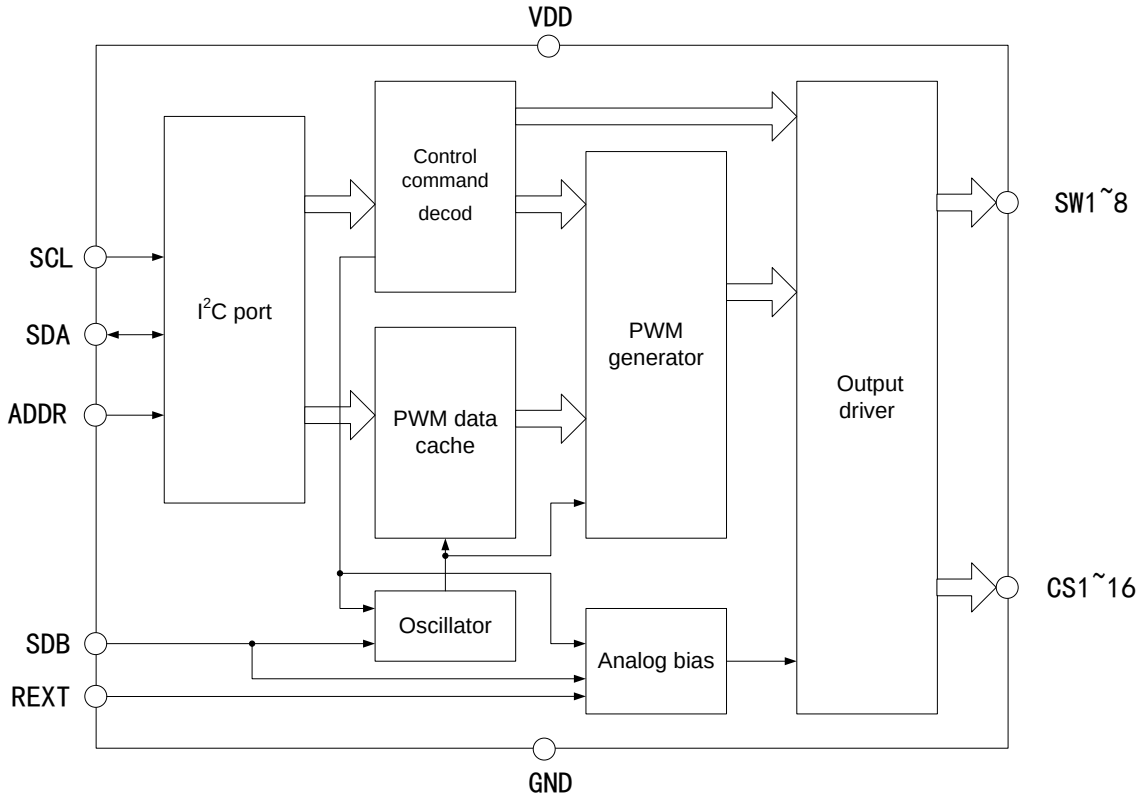


Figure 2. Block Diagram

Functions Description

Serial Port Interface

MCU can transmit data with ET61L128 each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected.

Data Validity

When the SCL signal is HIGH, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

Start (Re-start) and Stop Working Conditions

When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

Byte format

Each byte of data line contains 8 bits, which contains an acknowledge bit. The first data is transmitted MSB.

Acknowledge

During the writing mode, ET61L128 will send a low level response signal with one period width to the SDA port. During the reading mode, ET61L128 will not send response signal and the host will send a high response signal one period width to the SDA.

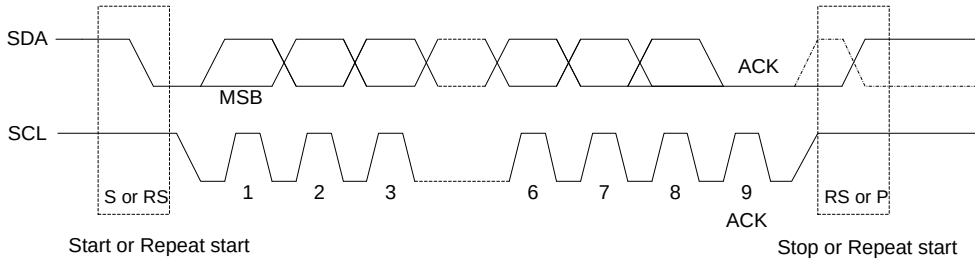


Figure 3. I²C write mode

- ACK=Acknowledge
- MSB=Most Significant Bit
- S=Start Conditions RS=Restart Conditions P=Stop Conditions
- Fastest Transmission Speed =400KBITS/S
- Restart: SDA-level turnover as expressed by the dashed line waveform

Chip-Address

ET61L128 has 4 chip-address:

ADDR pin connect signal	7bit Chip-Address	8bit Chip-Address
VDD	0101011b(2BH)	56H/57H(W/R)
GND	0101010b(2AH)	54H/55H(W/R)
SCL	0101000b(28H)	50H/51H(W/R)
SDA	0101001b(29H)	52H/53H(W/R)

I²C Writing Command Register Interface Protocol (continuous)：

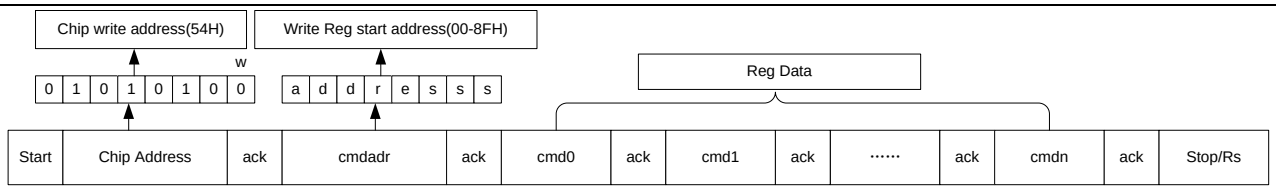


Figure 4. I²C Writing Command Register Protocol (continuous)

- Start = Start Conditions
- Chip Address = Write register address = 0101010+0(w)b
- ack = Acknowledge from ET61L128
- Write Reg start address byte = cmdadr (REG's 8bit address)
- ack = Acknowledge from ET61L128
- Command Reg data 1=cmd1(Command data)
- ack = Acknowledge from ET61L128
- ……
- Command Reg data n=cmdn(Command data)
- ack = Acknowledge from ET61L128

- Stop/Rs=Stop Condition/Restart Condition

I²C Reading Command Register Interface Protocol(continuous)

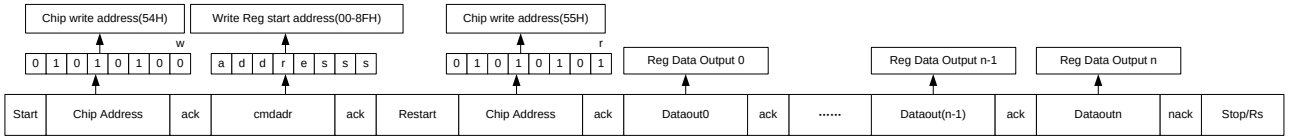


Figure 5. I²C Reading Command Register Interface Protocol(continuous)

- Start =Start Conditions
- Chip Address = Write register address = 0101010+0(w)b
- ack = Acknowledge from ET61L128
- Write Reg start address byte = cmdadr(REG's 8bit address)
- ack = Acknowledge from ET61L128
- Restart = Restart condition
- Chip address = Read register address= 0110010+1(w)b
- ack = Acknowledge from ET61L128
- Dataout0=Register data output 0
- ack=Acknowledge from Host
- ……
- Dataoutn=Register data output n
- nack=No Acknowledge from Host
- Stop/Rs=Stop Condition/Restart Condition

Register Definition

Table 1. Registers Definition

Addr	Name	Description							
00H	CONTROL1	soft_reset=11011b effective					osc_clk_sel[1:0]		chip_en
01H	CONTROL2	000b			scan_line_sel[1:0]			chg_line_time[1:0]	
02H	CONTROL3	chipid=1110				shadow_sw[1:0]		shadow_cs[1:0]	
03H	CONTROL4	00b		glb_max_cur_sel[4:0]					dis_en
04H	CONTROL5	otp_en	vds_sel	rext_sel	000b			sspt_sel	ssp_en
05H	CS_CUR_SEL1	cs4_cur[1:0]		cs3_cur[1:0]		cs2_cur[1:0]		cs1_cur[1:0]	
06H	CS_CUR_SEL2	cs8_cur[1:0]		cs7_cur[1:0]		cs6_cur[1:0]		cs5_cur[1:0]	
07H	CS_CUR_SEL3	cs12_cur[1:0]		cs11_cur[1:0]		cs10_cur[1:0]		cs9_cur[1:0]	
08H	CS_CUR_SEL4	cs16_cur[1:0]		cs15_cur[1:0]		cs14_cur[1:0]		cs13_cur[1:0]	
09H	STA_DET_CTR1	00b		open_vset[1:0]		short_vset[1:0]		sta_det_en	open_ short_sel
0AH	STA_DET_CTR2	cs_port_ en	0000b				sw_port_en		
0BH	LED_N8_STA1	cs8_led_ n8_sta	cs7_led_ n8_sta	cs6_led_ n8_sta	cs5_led_ n8_sta	cs4_led_ n8_sta	cs3_led_ n8_sta	cs2_led_ n8_sta	cs1_led_ n8_sta
0CH	LED_N8_STA2	cs16_led _n8_sta	cs15_led _n8_sta	cs14_led _n8_sta	cs13_led_ n8_sta	cs12_led _n8_sta	cs11_led_n 8_sta	cs10_led_n 8_sta	cs9_led_n 8_sta
10~8FH	LEDnPWM	ledn_pwm[7:0]							

Table 2. CONTROL1 Register

Addr: 00h			CONTROL1 Register			
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
00H	7:3	sw_reset	00000b	R/W	Software Reset Command	
					11011b	Reset reg00~8Fh
					Other	-
	2:1	osc_clk_sel	00b	R/W	Oscillator frequency Selection	
					00	1M
					01	2M
					10	4M
					11	8M
	0	chip_en	0b	R/W	Chip Enable Signal	
					0	Disable the IC
					1	Enable the IC

Note: chip_en=0, all the analog circuit will be shutdown, the current consumption will be lowest.

Table 3. CONTROL2 Register

Control Register 2						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
01H	7:5	-	000	-	Reserved	
	4:2	scan_line_sel	111	W/R	Scan lines for the SW port	
					111	8 SWs(default)
					……	……
					100	5 SWs
					……	……
					001	2 SWs
					000	1 SW
	1:0	chg_line_time	00	W/R	00	4 PWM clock cycles
					01	8 PWM clock cycles
					10	12 PWM clock cycles
					11	16 PWM clock cycles

Table 4. CONTROL3 Register

Control Register 3						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
02H	7:4	chipid	1110	R	IC ID	
	3:2	shadow_cs	01	W/R	CS Blanking	
					00	Disable blanking
					01	Weak level blanking
					10	Middle level blanking
					11	High level blanking
	1:0	shadow_sw	00	W/R	SW Blanking	
					00/01	Disable blanking
					10	Weak blanking
					11	High level blanking

Table 5. CONTROL4 Register

Control Register 4						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
03H	7：6	-	00	-	Reserved	
	5:1	glb_max_cur_sel	01111	W/R	CSnport output constant current Ics(n=1~16)	
					11111	49.2mA
					11110	48mA
					……	……
					01111	30mA(default)
					……	……
					00000	12mA

	0	dis_en	0	W/R	0	Display off
					1	Display on

Note: The current data in the table3, the condition is that the external resistance between REXT port and gnd is 10K ohm.

Table 6. CONTROL5 Register

Control Register 5						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
04h	7	otp_en	0	R/W	Chip over-temperature protection(OTP)	
					0	Disable Chip OTP function
					1	Enable Chip OTP function
	6	vds_sel	0	R/W	CSn VDS selection	
					0	Normal
					1	100mv upper
	5	rext_sel	0	R/W	Reference Resistor Selection	
					0	Select External Resistor
					1	Select Internal Resistor(fixed 10K)
	4:2	-	-	-	Reserved	
	1	sspt_sel	0b	R/W	Spread Spectrum Cycle Time Selection	
					0b	2000us
					1b	1000us
	0	ssp_en	0b	R/W	Spread Spectrum Function Enable	
					0b	Disable
					1b	Enable

Note: Spread Spectrum Function will modulate the OSC frequency in a range of Fosc+-10% with setting spread spectrum cycle time.

Table 7. CS_CUR_SEL1 Register

CS1~CS4 Channel Current Selection Registers						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
05H	7:6	cs4_cur[1:0]	11b	R/W	CS4 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	5:4	cs3_cur[1:0]	11b	R/W	CS3 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	3:2	cs2_cur[1:0]	11b	R/W	CS2 Channel Current Selection	
					11b	4/4 of Max Channel Current

					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	1:0	cs1_cur[1:0]	11b	R/W	CS1 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current

Table 8. CS_CUR_SEL2 Register

CS8~CS5 Channel Current Selection Registers						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
06H	7:6	cs8_cur[1:0]	11b	R/W	CS8 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	5:4	cs7_cur[1:0]	11b	R/W	CS7 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	3:2	cs6_cur[1:0]	11b	R/W	CS6 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	1:0	cs5_cur[1:0]	11b	R/W	CS5 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current

Table 9. CS_CUR_SEL3 Register

CS12~CS9 Channel Current Selection Registers						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
07H	7:6	cs12_cur[1:0]	11b	R/W	CS12 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	5:4	cs11_cur[1:0]	11b	R/W	CS11 Channel Current Selection	

					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	3:2	cs10_cur[1:0]	11b	R/W	CS10 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	1:0	cs9_cur[1:0]	11b	R/W	CS9 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current

Table 10. CS_CUR_SEL4 Register

CS16~CS13 Channel Current Selection Registers						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
08H	7:6	cs16_cur[1:0]	11b	R/W	CS16 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	5:4	cs15_cur[1:0]	11b	R/W	CS15 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	3:2	cs14_cur[1:0]	11b	R/W	CS14 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current
	1:0	cs13_cur[1:0]	11b	R/W	CS13 Channel Current Selection	
					11b	4/4 of Max Channel Current
					10b	3/4 of Max Channel Current
					01b	2/4 of Max Channel Current
					00b	1/4 of Max Channel Current

Table 11. STA_DET_CTR1 Register

Output Status Detection Control Register						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
09h	7:6	-	-	-	Reserved	
	5:4	open_vset[1:0]	00b	R/W	Open Detection Voltage Setting	
					00b	0.1V
					01b	0.2V
					10b	0.3V
					11b	0.4V
	3:2	short_vset[1:0]	00b	R/W	Short Detection Voltage Setting	
					00b	VDD-0.2V
					01b	VDD-0.4V
					10b	VDD-0.6V
					11b	VDD-0.8V
	1	sta_det_en	0b	R/W	Channel OPEN or SHORT Detection Enable	
					0b	Detection Disable
					1b	Detection Enable
	0	open_short_sel	0b	R/W	Channel OPEN or SHORT Detection Selection	
					0b	OPEN Detection
					1b	SHORT Detection

Table 12. STA_DET_CTR2 Register

Output Status Detection Control Register						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
0Ah	7	cs_port_en	0	R/W	CSn port enable signal(n=1~16)	
					0	Disable
					1	Enable
	6:3	--	0000b	-	Reserved	
	2:0	sw_port_en	000b	R/W	SWn Port Enable Select(n=1~8)	
					000b	SW1 port enable
					001b	SW2 port enable
					010b	SW3 port enable
					011b	SW4 port enable
					100b	SW5 port enable
					101b	SW6 port enable
					110b	SW7 port enable
					111b	SW8 port enable

Table 13. LED_N8_STA1 Registers

CS1~CS8 Channel Connected LED Open-short Status Register when any of SW1~SW8 enable						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
0BH	7	cs8_led_n8_sta	0b	R	CS8 Channel Connected LED Open/Short Status Error	
					0b	Normal
					1b	Error
	6	cs7_led_n8_sta	0b	R	CS7 Channel Connected LED Open/Short Status Error	
					0h	Normal
					1b	Error
	5	cs6_led_n8_sta	0b	R	CS6 Channel Connected LED Open/Short Status Error	
					0h	Normal
					1b	Error
	4	cs5_led_n8_sta	0b	R	CS5 Channel Connected LED Open/Short Status Error	
					0h	Normal
					1b	Error
	3	cs4_led_n8_sta	0b	R	CS4 Channel Connected LED Open/Short Status Error	
					0h	Normal
					1b	Error
	2	cs3_led_n8_sta	0b	R	CS3 Channel Connected LED Open/Short Status Error	
					0h	Normal
					1b	Error
	1	cs2_led_n8_sta	0b	R	CS2 Channel Connected LED Open/Short Status Error	
					0h	Normal
					1b	Error
	0	cs1_led_n8_sta	0b	R	CS1 Channel Connected LED Open/Short Status Error	
					0h	Normal
					1b	Error

Table 14. LED_N8_STA2 Registers

CS9~CS16 Channel Connected LED Open-short Status Register when any of SW1~SW8 enable						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
0CH	7	cs16_led_n8_sta	0b	R	CS16 Channel Connected LED Open/Short Status Error	
					0h	Normal
					1b	Error
	6	cs15_led_n8_sta	0b	R	CS15 Channel Connected LED Open/Short Status Error	
					0h	Normal
					1b	Error
	5	cs14_led_n8_sta	0b	R	CS14 Channel Connected LED Open/Short Status Error	
					0h	Normal
					1b	Error
	4	cs13_led_n8_sta	0b	R	CS13 Channel Connected LED Open/Short Status Error	
					0h	Normal
					1b	Error
	3	cs12_led_n8_sta	0b	R	CS12 Channel Connected LED Open/Short Status Error	
					0h	Normal
					1b	Error
	2	cs11_led_n8_sta	0b	R	CS11 Channel Connected LED Open/Short Status Error	
					0h	Normal
					1b	Error
	1	cs10_led_n8_sta	0b	R	CS10 Channel Connected LED Open/Short Status Error	
					0h	Normal
					1b	Error
	0	cs9_led_ n8_sta	0b	R	CS9 Channel Connected LED Open/Short Status Error	
					0h	Normal
					1b	Error

Note: Output Error status need to cooperate with Reg09 [1:0] sta_det_en and open_short_sel status, while the data is “0”, the output port is the normal status, while the data is “1”, the output port is OPEN or SHORT status.

Also, it need to cooperate with Reg0A[7][2:0] cs_port_en and sw_port_en[2:0] to detect all the LEDs OPEN or SHORT status in each SWn(n=1~8) enable condition.

Table 15. LEDnPWM Register

LEDnPWM Registers(n=1~128)						
Addr	**Bit**	**Bit Name**	**Default**	**Access**	**Description**	
10H → 8FH	7:0	ledn_pwm	00000000b	R/W	LEDn PWM Current Setting(n=1~144)	
					00000000b	0/255 duty cycle
					00000001b	1/255 duty cycle
					……	……
					11111110b	254/255 duty cycle
					11111111b	255/255 duty cycle

Note： Other registers can be configured only after the 00 register is enabled. When the chip is in the off state, other registers cannot be written. The soft reset instruction is recommended to be written after the chip is enabled off, after which all control registers and PWM data registers are reset to default values.

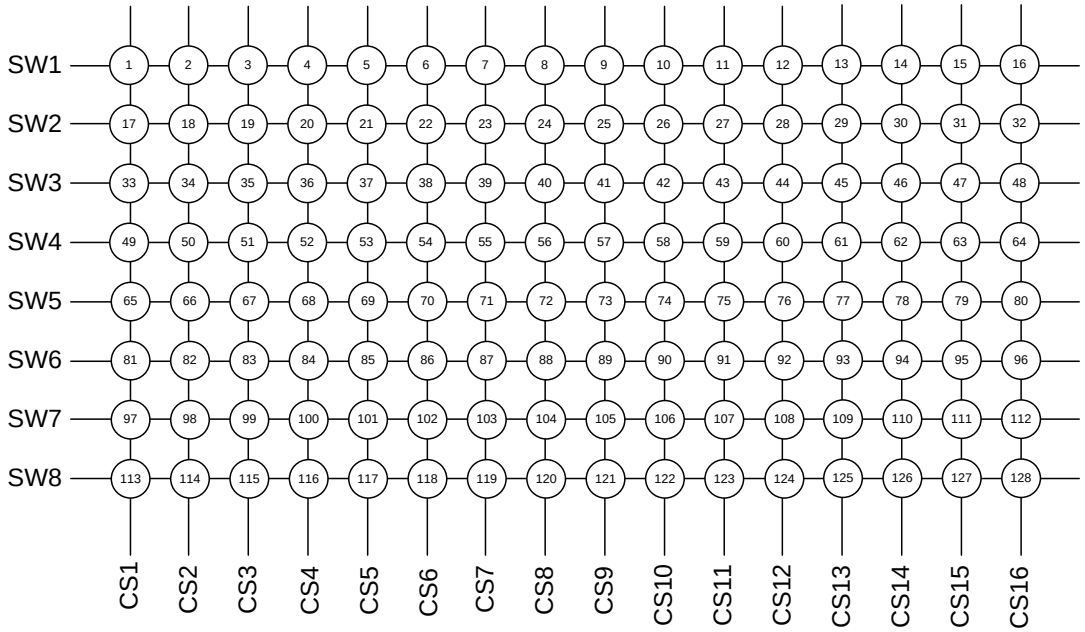


Figure 6. LED dot matrix diagram

Note： The PWM data corresponding to 1 point in the figure is LED1PWM in the following table, and the PWM data corresponding to 128 points in the figure is LED128PWM in the following table, and so on for other points.

Table 16. PWM register and LED lattice mapping table

地址	描述	地址	描述	地址	描述	地址	描述
10H	LED1PWM	11H	LED2PWM	12H	LED3PWM	13H	LED4PWM
14H	LED5PWM	15H	LED6PWM	16H	LED7PWM	17H	LED8PWM
18H	LED9PWM	19H	LED10PWM	1AH	LED11PWM	1BH	LED12PWM
1CH	LED13PWM	1DH	LED14PWM	1EH	LED15PWM	1FH	LED16PWM
20H	LED17PWM	21H	LED18PWM	22H	LED19PWM	23H	LED20PWM
24H	LED21PWM	25H	LED22PWM	26H	LED23PWM	27H	LED24PWM
28H	LED25PWM	29H	LED26PWM	2AH	LED27PWM	2BH	LED28PWM
2CH	LED29PWM	2DH	LED30PWM	2EH	LED31PWM	2FH	LED32PWM
30H	LED33PWM	31H	LED34PWM	32H	LED35PWM	33H	LED36PWM
34H	LED37PWM	35H	LED38PWM	36H	LED39PWM	37H	LED40PWM
38H	LED41PWM	39H	LED42PWM	3AH	LED43PWM	3BH	LED44PWM
3CH	LED45PWM	3DH	LED46PWM	3EH	LED47PWM	3FH	LED48PWM
40H	LED49PWM	41H	LED50PWM	42H	LED51PWM	43H	LED52PWM
44H	LED53PWM	45H	LED54PWM	46H	LED55PWM	47H	LED56PWM
48H	LED57PWM	49H	LED58PWM	4AH	LED59PWM	4BH	LED60PWM
4CH	LED61PWM	4DH	LED62PWM	4EH	LED63PWM	4FH	LED64PWM
50H	LED65PWM	51H	LED66PWM	52H	LED67PWM	53H	LED68PWM
54H	LED69PWM	55H	LED70PWM	56H	LED71PWM	57H	LED72PWM
58H	LED73PWM	59H	LED74PWM	5AH	LED75PWM	5BH	LED76PWM
5CH	LED77PWM	5DH	LED78PWM	5EH	LED79PWM	5FH	LED80PWM
60H	LED81PWM	61H	LED82PWM	62H	LED83PWM	63H	LED84PWM
64H	LED85PWM	65H	LED86PWM	66H	LED87PWM	67H	LED88PWM
68H	LED89PWM	69H	LED90PWM	6AH	LED91PWM	6BH	LED92PWM
6CH	LED93PWM	6DH	LED94PWM	6EH	LED95PWM	6FH	LED96PWM
70H	LED97PWM	71H	LED98PWM	72H	LED99PWM	73H	LED100PWM
74H	LED101PWM	75H	LED102PWM	76H	LED103PWM	77H	LED104PWM
78H	LED105PWM	79H	LED106PWM	7AH	LED107PWM	7BH	LED108PWM
7CH	LED109PWM	7DH	LED110PWM	7EH	LED111PWM	7FH	LED112PWM
80H	LED113PWM	81H	LED114PWM	82H	LED115PWM	83H	LED116PWM
84H	LED117PWM	85H	LED118PWM	86H	LED119PWM	87H	LED120PWM
88H	LED121PWM	89H	LED122PWM	8AH	LED123PWM	8BH	LED124PWM
8CH	LED125PWM	8DH	LED126PWM	8EH	LED127PWM	8FH	LED128PWM

Note： Each address has 8bits of data corresponding to the number of PWM steps at that point (256 steps). The default value for each set of registers is FFH.

Display cycle

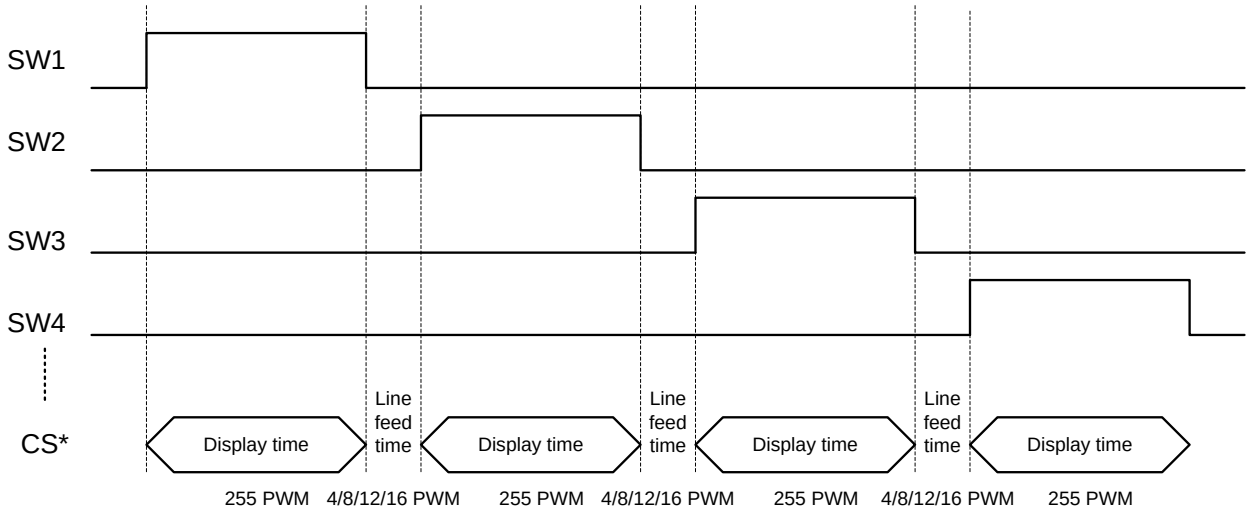


Figure 7. Display Cycle: Scan line× (4/8/12/16 Line feed time+255 steps PWM time)

Absolute Maximum Ratings

(Unless otherwise noted ,T_A=25°C)

Symbol	Characteristic	Rating	Unit
V_{DD}	Supply Voltage	-0.3~6.0	V
V_I	Input Voltage	-0.3~V_{DD}+0.3	V
P_D	Power Dissipation（QFN32）	1400	mW
	Power Dissipation（LQFP32）	700	
θ_{JA}	Thermal Resistance（QFN32）	41	°C/W
	Thermal Resistance（LQFP32）	89	
T_{JMAX}	Junction Temperature	150	°C
T_{STG}	Storing Temperature	-65～150	°C
V_{ESD}	HBM	±2.0	KV
	CDM	±1.0	KV

Recommended Operating Conditions

Symbol	Characteristic	Min	Typ	Max	Unit
V_{DD}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	Logic high level	1.4		V_{DD}	V
V_{IL}	Logic low level	0		0.4	*V*
T_A	Operating Temperature	-40		+85	°C

Electrical Characteristics

(Unless otherwise noted, V_{DD}=5V ,T_A=25°C)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage		2.7	5.0	5.5	V
I_{CS_MAX}	Maximum constant current output	CSn；V_{CSn}=0.5V，R_{EXT}=10KΩ lednpwm=FFH(n=1~128) csn_cur [1:0]=11b(1~16) glb_max_cur_sel [4:0]=11111b		49.2		mA
I_{CS_MIN}	Minimum constant current output	CSn；V_{CSn}=0.5V，R_{EXT}=10KΩ lednpwm=FFH(n=1~128) csn_cur [1:0]=11b(1~16) glb_max_cur_sel [4:0]=00000b		12		mA
$I_{CS_default}$	Default constant current output	CSn；V_{CSn}=0.5V，R_{EXT}=10KΩ lednpwm=FFH(n=1~128) csn_cur [1:0]=11b(1~16) glb_max_cur_sel [4:0]=01111b		30		mA
I_{SW}	Switch tube drive capability	SWn；V_{SWn}=4.5V		800		mA
V_{IH}	Logic high level	SDA，SCL，ADDR，SDB	1.4			V
V_{IL}	Logic low level	SDA，SCL，ADDR，SDB			0.4	V
I_{IN}	IO input current	V_I=V_{DD}， SDA，SCL，ADDR，SDB	-1		1	uA
I_{IN_SW}	SW input current	SWn=0V(n=1~8)，SDB=0V	-1		1	uA
I_{IN_CS}	CS input current	CSn(n=1~16)=5V，SDB=0V	-1		1	uA
V_{OL_SDA}	SDA Output Low Level	I_{OUT}=3mA			0.4	V
I_{DD}	Static current	无负载，关显示，芯片使能		3	6	mA
I_{SD}	Shutdown current	V_{SDB} = 0V， V_{SDA} = V_{SCL} = V_{ADDR} = V_{DD}/0V		3	5	uA
		V_{SDB} = V_{DD}，chip_en=0， V_{SDA} = V_{SCL} = V_{ADDR} = V_{DD}/0V		3	5	uA

Switching Characteristics

(Unless otherwise noted, V_{DD}=5V ,T_A=25°C)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
T_{PWM}	Display time	LEDPWM=0xFF, osc_clk_sel=00		255		us
T_{CHG_LINE}	Line feed time	scan_chg_line=00, osc_clk_sel=00		4.0		us

I²C Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCL}	SCL Clock Frequency	0	-	400	KHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	1.3	-	-	μs
$t_{HD:STA}$	Hold Time(Repeated) START Condition	0.6	-	-	μs
t_{LOW}	Low Period of SCL Clock	1.3	-	-	μs
t_{HIGH}	HIGH Period of SCL Clock	0.6	-	-	μs
$t_{SU:STA}$	Setup Time for a Repeated START Condition	0.6	-	-	μs
$t_{HD:DAT}$	Data Hold Time	0.1	-	-	μs
$t_{SU:DAT}$	Data Setup Time	100	-	-	ns
t_R	Data Hold Time2	-	20+0.1Cb(1)	300	ns
t_F	Data Hold Time2	-	20+0.1Cb(1)	300	ns
$t_{SU:STO}$	Setup Time for STOP Condition	0.6	-	-	μs

Note1: Cb=total capacitance of one bus line in PF unit.

I²C Timing Waveform

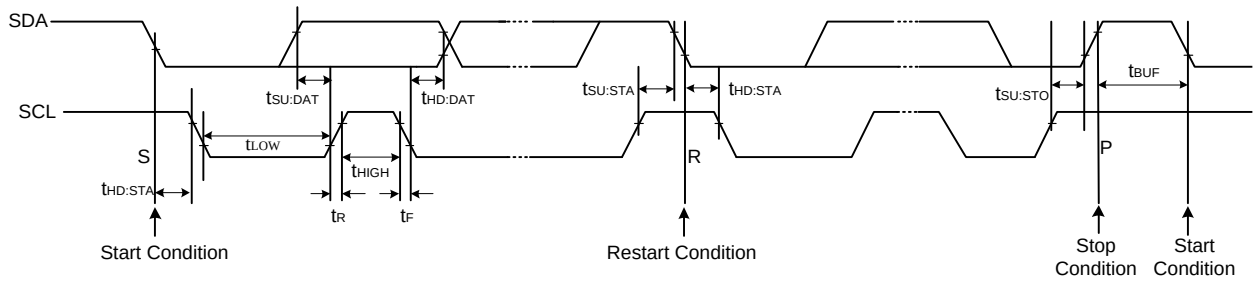


Figure 8. Definition of Timing for I²C Bus

Application circuit

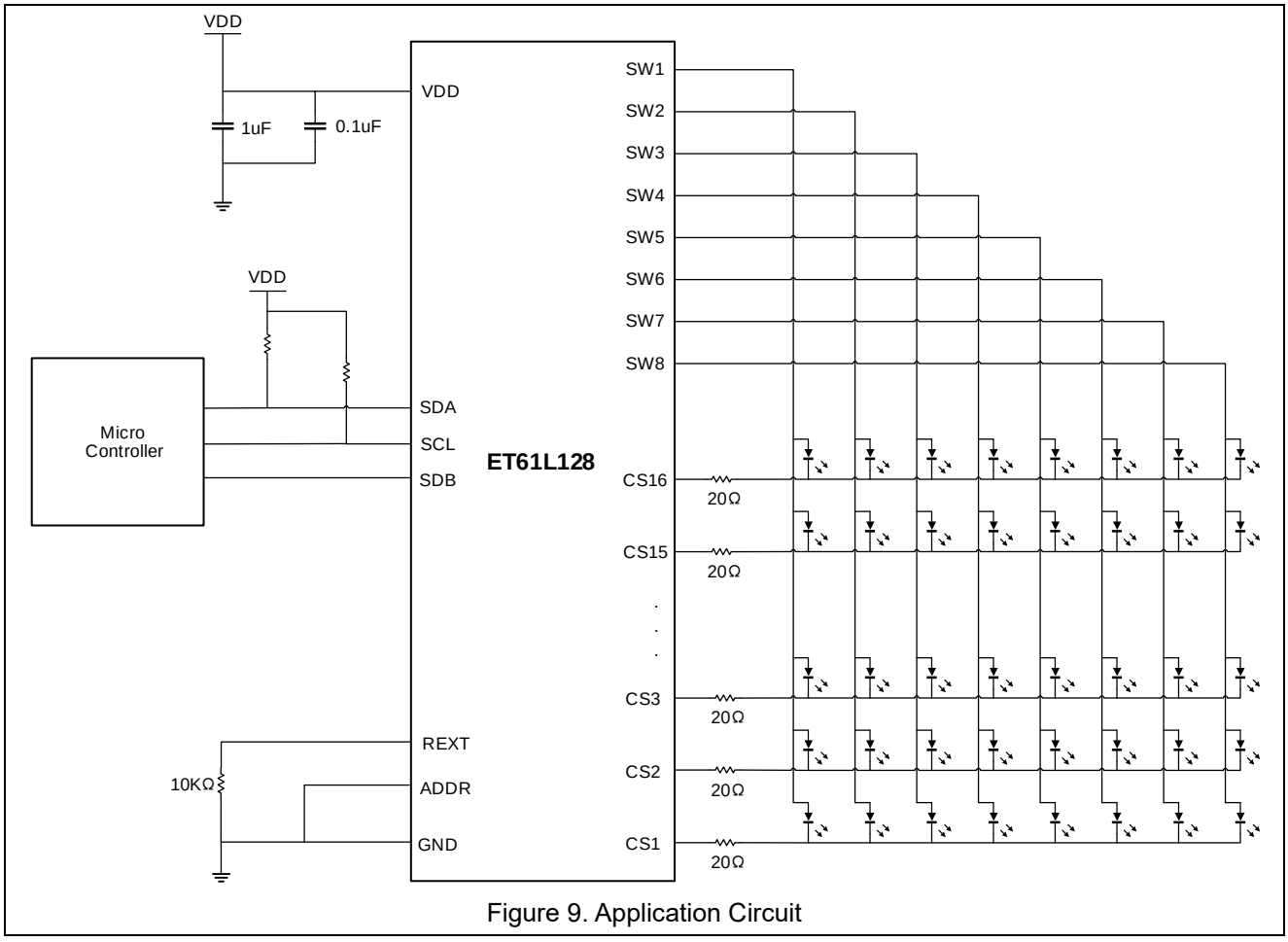
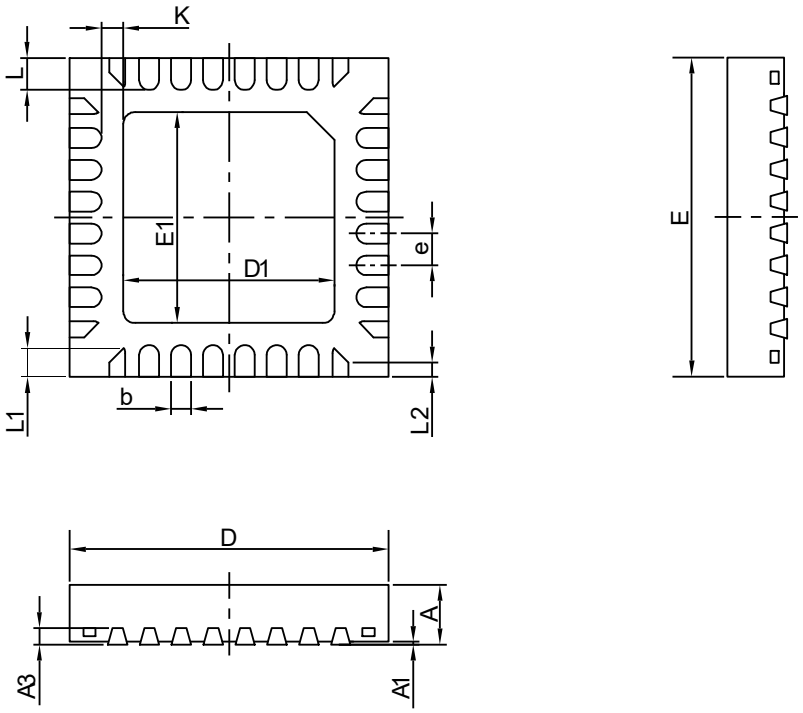


Figure 9. Application Circuit

Note：This application circuit is only for reference.

Package

QFN32

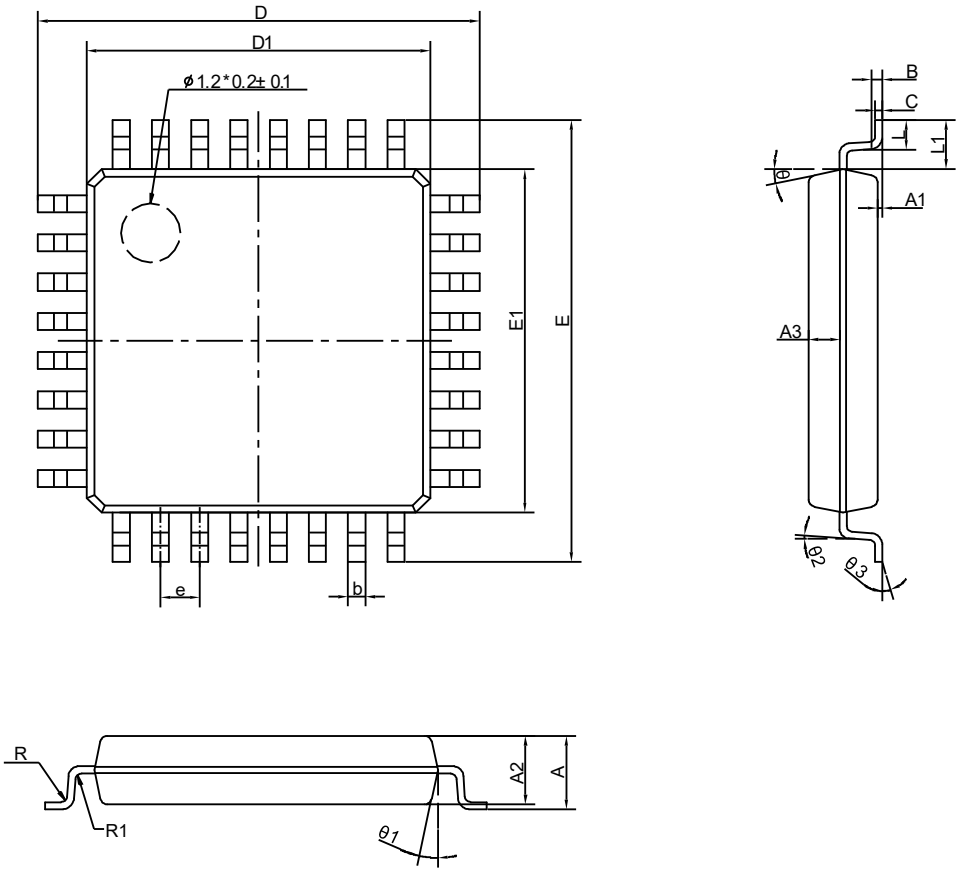


COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	--	0.05
A3		0.203REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D1	2.55	2.65	2.75
E1	2.55	2.65	2.75
e		0.40TYP	
K	0.20	--	--
L	0.30	0.40	0.50
L1	0.31	0.36	0.41
L2	0.13	0.18	0.23

LQFP32



COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A	--	1.60	E1	6.90	7.10
A1	0.05	0.15	e	0.80TYP	
A2	1.35	1.45	L	0.50	0.80
A3	0.64TYP		L1	1.00BSC	
B	0.25TYP		θ	12° TYP	
b	0.32	0.43	θ1	12° TYP	
C	0.127	0.16	θ2	4° TYP	
D	8.80	9.20	θ3	0° ~ 8°	
D1	6.90	7.10	R	0.15TYP	
E	8.80	9.20	R1	0.12TYP	

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2026-03-12	Original Version	Wangli	Li Chen Xuan	Liu Jia Ying
1.0.a	2026-08-24	Correcting a typing error	Tianqihe	Li Chen Xuan	Liu Jia Ying