Logic Detection IC

General Description

The ET9821L is a micro-power logic IC for TWS case status detection. It monitors VBUS, hall detect signal and reset optional signal continuously and generate related reset signal for microprocessor or logic system. It has internal oscillator for time delay generation. It has one open drain output port for reset signal.

Features

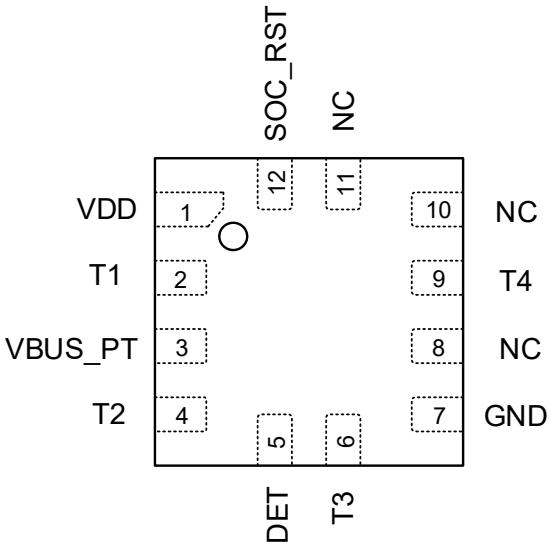
- Supply Voltage Range: 2.4 ~ 5.5V
- Low Standby Current: 1.2μA (Max)
- One N-Channel Open-Drain Output for Reset Signal
- Internally Generated Delay Time
- 3 Optional Reset Trigger mode
- Operation Temperature Range: -40 ~ 85°C
- Package information:

Part No.	Package	Reel	MSL
ET9821L	UTQFN12 (1.6*1.6 mm)	3k/Reel	Level 1

Application

- TWS Case
- Portable/Battery-Powered Equipment

Pin Configuration

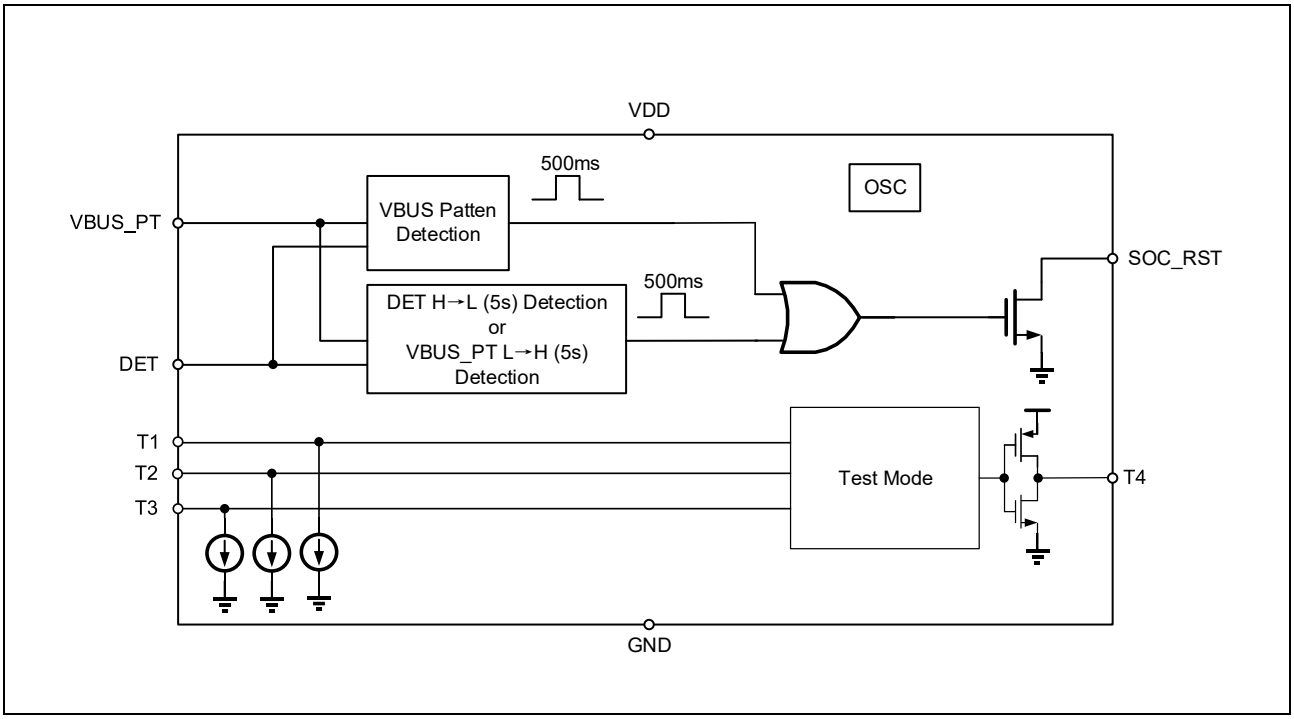


Top View

Pin Function

Pin No	Pin Name	Description
1	VDD	Power Supply
2	T1	Test Pin 1 (This pin is only for ATE function test and could keep floating when using)
3	VBUS_PT	VBUS Power Detecting Input
4	T2	Test Pin 2 (This pin is only for ATE function test and could keep floating when using)
5	DET	Hall Detecting Input
6	T3	Test Pin 3 (This pin is only for ATE function test and could keep floating when using)
7	GND	Ground
8	NC	No Connection Pin
9	T4	Test Pin 4 (This pin is only for ATE function test and must keep floating when using)
10	NC	No Connection Pin
11	NC	No Connection Pin
12	SOC_RST	SOC Reset Control Open Drain Output

Block Diagram



Function Description

ET9821L is a logic detecting circuit. It has 2 input and 1 output ports, SOC_RST is according to several input and have delay time control.

SOC_RST is for system SOC reset. If DET is high, SOC_RST send 500ms (T_{D2}) low pulse when detect VBUS power on pattern. If VBUS_PT is high, SOC_RST send 500ms (T_{D2}) low pulse when detect DET input H -> L and keep L for more than 5 second (T_{D1b}). If DET is low, SOC_RST send 500ms (T_{D2}) low pulse when detect VBUS_PT input L -> H and keep H for more than 5 second (T_{D1b}). Otherwise SOC_RST keep high in normal. SOC_RST has NMOS open drain output. VBUS_PT sequence must be in 1 second (T_{D1a}). Both of VBUS_PT and DET input have 100ms (T_{DB1}) debounce time.

VBUS_PT and DET input have 10us (T_{DG1}) de-glitch time.

T1, T2, T3 and T4 are only for ATE function test. T1, T2 and T3 could keep floating when using. T1, T2 and T3 highly recommend to connect to ground when using. T4 must keep floating when using.

Truth Table - SOC_RST

VBUS_PT (Input)	DET (Input)	SOC_RST (Output)
0	x	1
1	x	1
5V Reset Pattern	1	After Reset Pattern (within 1s), output 500ms ‘0’ pulse
x	1	1
1	1- > 0(t(0) < 5s)	Keep 1
1	1- > 0(t(0) > 5s)	After 5s, output 500ms ‘0’ pulse
0- > 1(t(1) > 5s)	0	After 5s, output 500ms ‘0’ pulse
0- > 1(t(1)< 5s)	0	Keep 1

Notes: 1=High, 0=Low, x=Don't Care;

For open drain output, 1=Floating, 0=Low;

For VBUS_PT, "1" means V>V_{TH_BUS}, "0" means V< (V_{TH_BUS} - V_{HYS_BUS}).

Timing Diagram

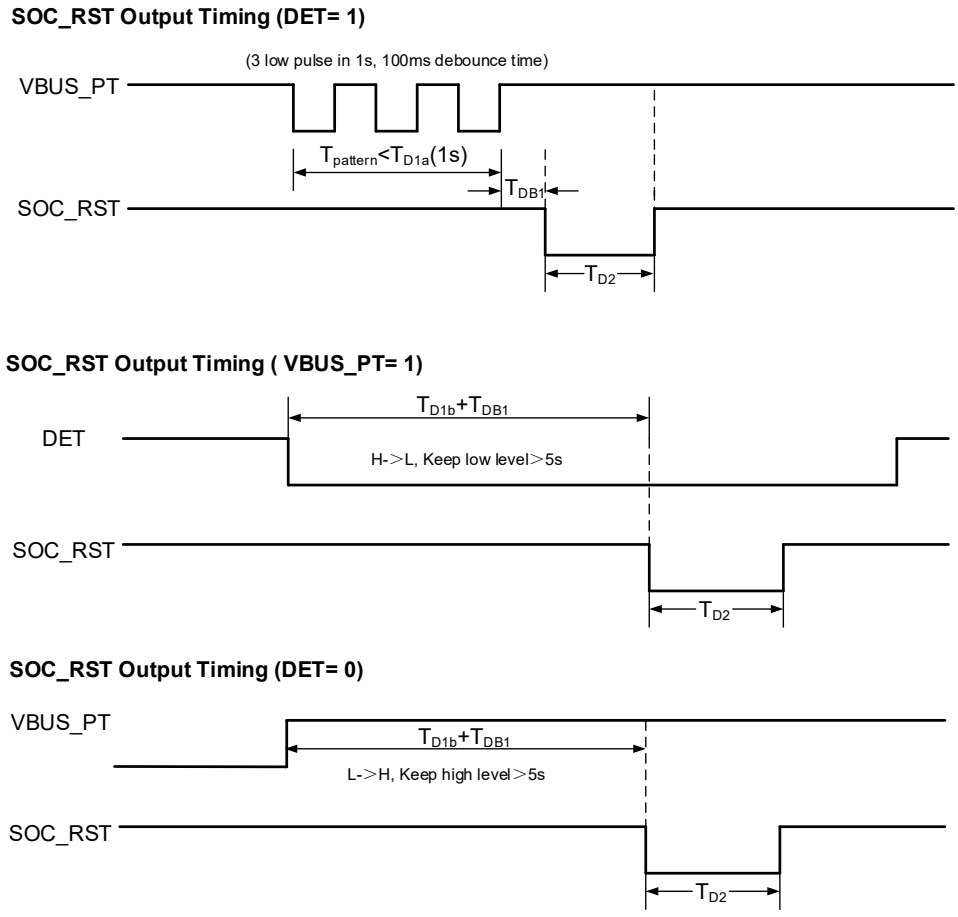


Figure 1. SOC_RST Timing

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristic	Symbol	Value	Unit
VDD Pin Voltage	V_{DD}	-0.3~6.0	V
VBUS_PT, DET, T1, T2, T3, SOC_RST Pin Voltage	V_{BUS_PT}, V_{DET}, V_{T1}, V_{T2}, V_{T3}, V_{SOC_RST}	-0.3~6.0	V
T4 Pin Voltage	V_{T4}	-0.3~ V_{DD}+0.3	V
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	300	°C/W
ESD Susceptibility (Human Body Mode) (1)	V_{ESD}	±2.0	kV
Operating Junction Temperature	T_J	-40~150	°C
Operating Ambient Temperature	T_A	-40~85	°C
Storage Temperature	T_{STG}	-65~150	°C

Note1: ESD Human Body Model tested per EIA/JESD22-A114 .

Electrical Characteristics

(Unless otherwise specified T_A= 25°C, V_{DD}= 5V)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply Voltage Range		2.4		5.5	V
I_{DD1}	Standby Current	VBUS_PT=L/DET= L and keep stable more than 100ms or VBUS_PT=L/DET= H and keep stable more than 100ms		0.8	1.2	μA
I_{DD2}	Supply Current In Active State	Internal oscillator active (In delay control state)		10	20	μA
V_{TH_BUS}	VBUS_PT Input Threshold Voltage	V_{DD} >2.7V	2.35	2.5	2.65	V
		2.4< V_{DD} <2.7V		V_{DD}-0.1		
V_{HYS_BUS}	VBUS_PT Input Hysteresis Voltage			40		mV
V_{IH_DET}	DET Input High Voltage		1.2			V
V_{IL_DET}	DET Input Low Voltage				0.3	V
I_B	T1, T2, T3 Terminal Current Sink			6	15	μA
V_{OD}	Open Drain Output Low Voltage (SOC_RST)	I-sink= 1mA			0.2	V
V_{OH}	T4 Output High Voltage	I-source= 1mA	V_{DD}-0.2			V
V_{OL}	T4 Output Low Voltage	I-sink= 1mA			0.2	V
T_{D1a}	VBUS_PT Maximum Detect Time	T_A = +25°C	0.96	1	1.04	s
		-40°C ≤ T_A ≤ 85°C	0.9	1	1.2	
T_{D1b} (2)	DET Low Level or VBUS_PT High Level Detect Time	T_A = +25°C	4.8	5	5.2	s
		-40°C ≤ T_A ≤ 85°C	4.5	5	6	
T_{D2}	SOC_RST Holding Time	T_A = +25°C	480	500	520	ms
		-40°C ≤ T_A ≤ 85°C	450	500	600	
T_{DB1}	VBUS_PT, DET Debounce time	T_A = +25°C	96	100	104	ms
		-40°C ≤ T_A ≤ 85°C	90	100	120	
T_{DG1} (3)	VBUS_PT, DET De-glitch time			10		μs
T_{SU}	Startup Time	V_{DD} rising past 1.9V		0.5		ms

Note2: T_{D1b} is factory programmable to 0s, 2.5s, 5s, 7.5s, 10s, 12.5s, 15s, 20s, default is 5s.

Note3: T_{DG1} is guaranteed by design, not test item.

Application Circuit

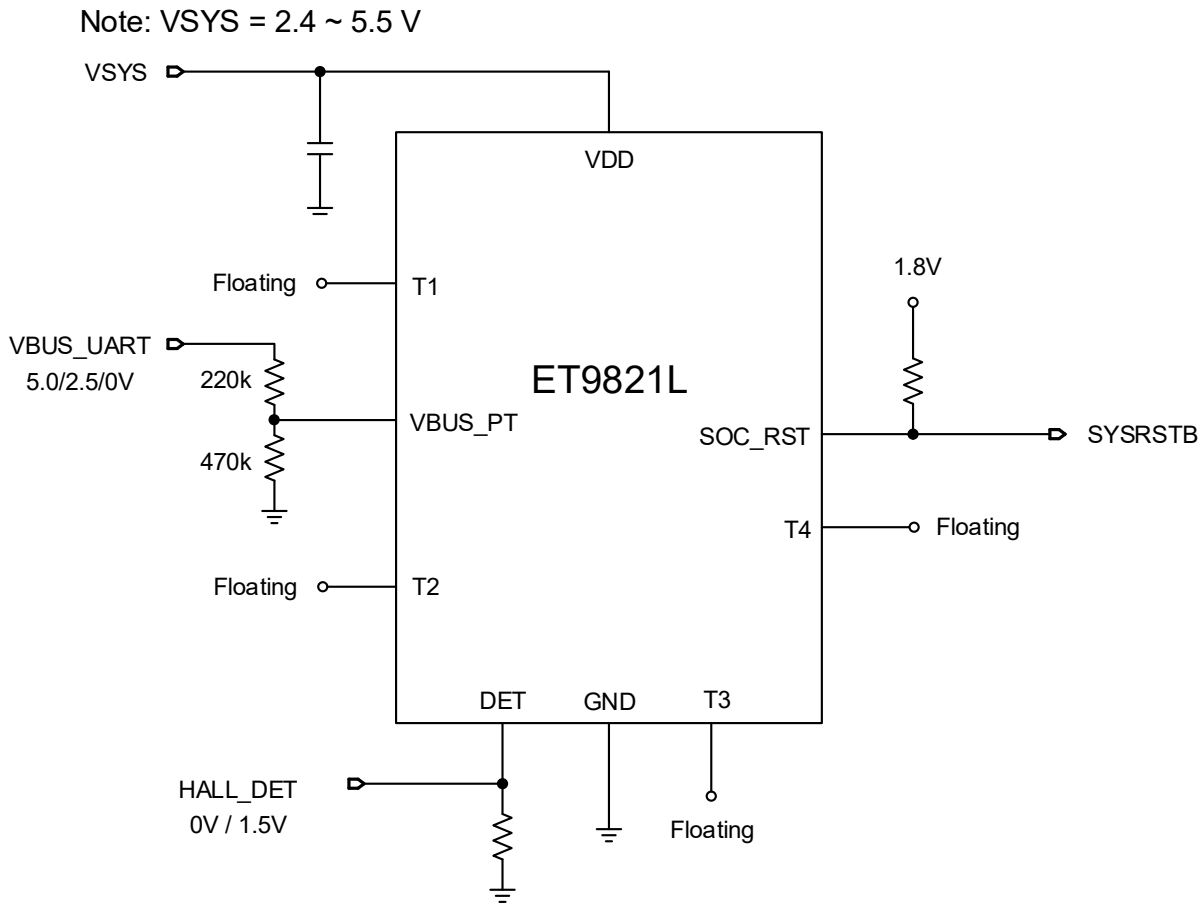
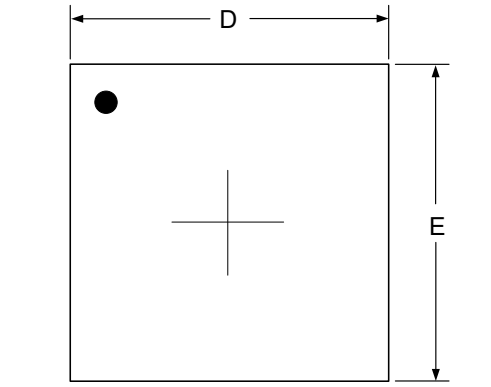


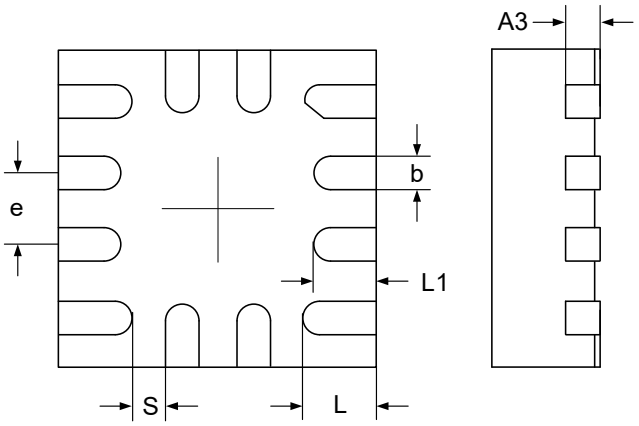
Figure 2. Reference Circuit Diagram

Package Dimension

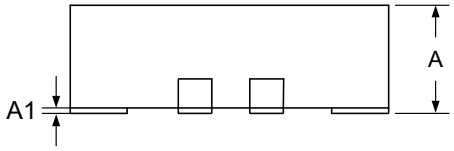
UTQFN12(1.6*1.6 mm)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

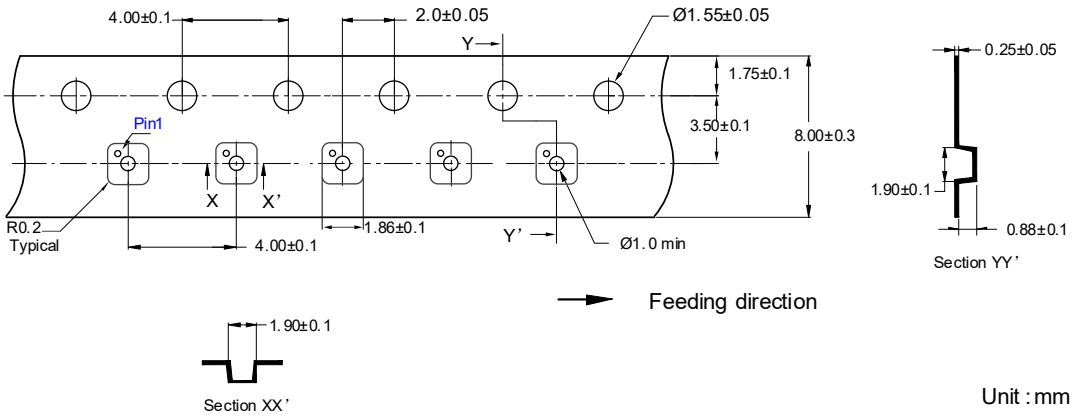
SYMBOL	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	--	0.05
A3		0.15 REF	
D	1.55	1.60	1.65
E	1.55	1.60	1.65
b	0.13	0.18	0.23
L	0.26	0.31	0.36
L1	0.175	0.225	0.275
S		0.20 REF	
e		0.40 REF	

Marking



XXXX - Tracking Number (year and week)

Tape Information



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025-10-09	Offical Version	Chenzx	Chenh	Liujy