800mA Dual-rail Very Low Dropout LDO

General Description

The ET55111YB is a CMOS-based low-dropout, low-power linear regulators, offering 800mA with NMOS pass transistor and a separate bias supply voltage (VBIAS). The device provides very stable, accurate output voltage with low noise, high ripple rejection and low supply current suitable for space constrained, noise sensitive application. The ET55111YB consist of an accurate voltage-reference block, an error amplifier, a thermal-shutdown circuit, and a current limit circuit.

The ET55111YB is offered in the small DFN4(1.2mm×1.2mm) package.

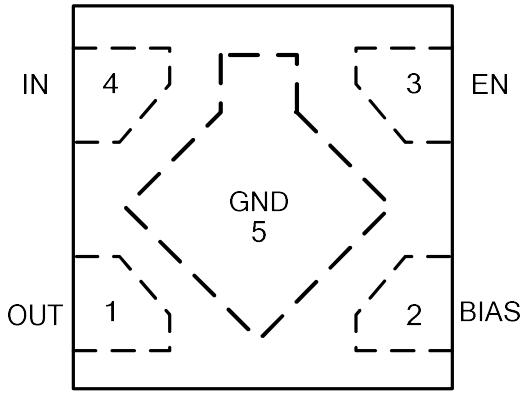
Features

- Wide VIN Input Voltage Range: 1.1V to 5.5V
- Wide VBIAS Voltage Range: 2.7V to 5.5V
- Output Voltage: 1.1V fixed
- Very Low VBIAS Input Current of Typ. 80μA
- Ultra-Low Dropout: Typ. 200mV at 800mA, 1.1V Output, 3.3V Bias
- Built-in Over Current Protection and Thermal Shutdown Circuit
- Built-in Auto-discharging Circuit
- Built-in Under Voltage Lock-out
- Stable with a 2.2μF Ceramic Capacitor
- Package: DFN4 (1.2mm × 1.2mm × 0.4mm)
- MSL1

Applications

- Constant-voltage power supply for battery-powered device
- Constant-voltage power supply for smartphones, tablets
- Constant-voltage power supply for cameras, DVRs, STB and camcorders

Pin Configuration

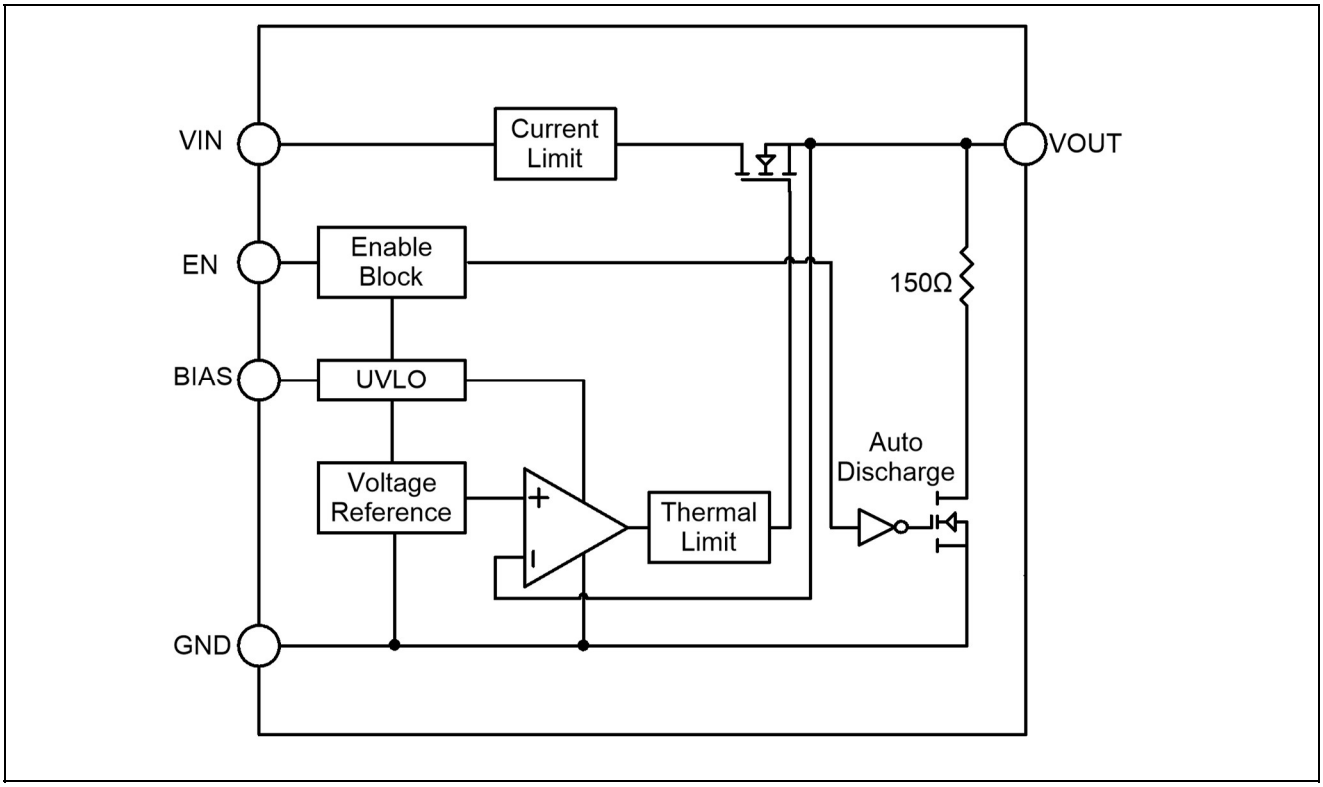


DFN4 (Top View)

Pin Function

Pin No.	Symbol	Pin Description
1	OUT	The Power Output of the Device.
2	BIAS	Input Voltage for Controlling Circuit.
3	EN	Enable Input.
4	IN	Input Voltage Pin. Large bulk capacitance should be placed closely to this pin. A 1μF ceramic capacitor is recommended at this pin.
5	GND	Ground Pin. Thermal PAD.

Block Diagram



Functional Description

The ET55111YB dual−rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from V_{IN} voltage. All the low current internal control circuitry is powered from the V_{BIAS} voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike PMOS topology devices, the output capacitor has reduced impact on loop stability. V_{IN} to V_{OUT} operating voltage difference can be very low compared with standard PMOS regulators in very low V_{IN} applications.

The ET55111YB offers smooth monotonic start-up.

Input and output Capacitor

The device is designed to be stable for ceramic output capacitors with Effective capacitance in the range from 1μF to 10μF. The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range. In applications where no low input supplies impedance available (PCB inductance in VIN and/or VBIAS inputs as example), the recommended C_{IN} = 1uF and C_{BIAS}= 0.1uF or greater.

Enable Pin Operation

The ET55111YB is turned on by setting the EN pin to “H”. The threshold limits are covered in the electrical characteristics table in this datasheet. When the EN pin is not used, connect the EN pin with VBIAS to keep the LDO in operating mode.

Current Limit Protection

When output current of VOUT pin is higher than current limit threshold or the VOUT pin is direct short to GND, the current limit protection will be triggered and clamp the output current at a predesigned level to prevent over-current and thermal damage.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool down. When the junction temperature reduces to approximately +145°C the output circuit is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Auto Discharging

When the EN pin set to “L”, the output circuit will be disable immediately, and the Auto-Discharging circuit will be turned on to discharge the electric charge on output capacitor, and decrease the voltage of V_{OUT} in very short time.

Absolute Maximum Ratings

Item	Rating	Unit
Input Voltage (IN Pin)	-0.3 to 6.0	V
Input Voltage (BIAS Pin)	-0.3 to 6.0	V
Input Voltage (EN Pin)	-0.3 to 6.0	V
Output Voltage (OUT Pin)	-0.3 to 6.0	V
Maximum Load Current	800	mA
Maximum Power Consumption	640	mW
Storage Temperature Range	-65 to +150	ºC
Operating Junction Temperature	-40 to +150	ºC
ESD HBM (JEDEC JS-001)	±4000	V
ESD CDM (JEDEC JS-002)	±1500	V

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{IN}	IN Input Voltage	1.1V + V_{DROP} to 5.5	V
V_{BIAS}	BIAS Input Voltage	2.7 to 5.5	V
I_{OUT}	Output Current	0 to 800	mA
T_A	Operating Ambient Temperature	-40 to 85	ºC
C_{IN}	Effective Input Ceramic Capacitor Value	0.47 to 10	µF
C_{BIAS}	Effective Input Ceramic Capacitor Value	0.047 to 4.7	µF
C_{OUT}	Effective Output Ceramic Capacitor Value	1 to 10	µF
ESR	Input and Output Capacitor Equivalent Series Resistance	5 to 100	mΩ

Electrical Characteristics

(Unless otherwise noted, V_{IN} = 1.4V, V_{BIAS} = 3.3V, I_{OUT} = 1mA, C_{IN} = 1μF, C_{OUT} = 2.2μF, C_{BIAS} = 0.1uF, T_A = -40ºC~85ºC.Typical values are at. T_A = 25ºC)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN} (1)	$V_{IN} > V_{OUT}$	1.1+ V_{DROP}		5.5	V
V_{BIAS} Voltage Range	V_{BIAS}	$V_{BIAS} \geq V_{OUT}$ + 1.6V	2.7		5.5	V
Under-voltage lock-out	V_{UVLO}	V_{BIAS} Rising / Hysteresis		1.6/0.2		V
V_{BIAS} Current	I_{Q_ON} (4)	Active Mode: V_{EN} = H		80	110	μA
	I_{Q_OFF}	V_{EN} = L		0.5	1.0	μA
Output Voltage	V_{OUT}	I_{OUT} = 1mA~800mA, T_A = 25 ºC	1.078		1.122	V
Dropout Voltage	V_{DROP} (2)	I_{OUT} = 500mA		125	187	mV
		I_{OUT} = 800mA		200	300	
Current Limit	I_{LIM}	V_{OUT} = 90%V_{OUT}	800	1150	1550	mA
Load Regulation	Reg_{LOAD}	1Ma ≤ I_{OUT} ≤ 800mA		2	20	mV
V_{IN} Line Regulation	Reg_{LINE}	1.4V ≤ V_{IN} ≤ 5V (V_{BIAS} = 3.3V, I_{OUT} = 1mA)		0.01	0.1	%/V
V_{BIAS} Line Regulation		2.7V < V_{BIAS} < 5.5V (V_{IN} = 1.4V, I_{OUT} = 1mA)		0.01	0.1	%/V
Ripple Rejection	PSRR (3)	V_{IN} to V_{OUT}, f = 1kHz, Ripple 0.2Vp-p, I_{OUT} = 30mA		80		dB
		V_{BIAS} to V_{OUT}, f = 1kHz, Ripple 0.2Vp-p, I_{OUT} = 30mA		80		
Output Noise	e_N (3)	V_{IN} = 1.6V f = 10Hz to 100kHz		40		μV_{RMS}
EN Pull-down Current	I_{EN}	V_{EN} = 5.5V		0.5	1	μA
EN Input Voltage High	V_{ENH}		0.9			V
EN Input Voltage Low	V_{ENL}				0.4	V
Output resistance of auto discharge at off state	R_{DIS}	V_{EN} = 0V, V_{OUT} = 0.5V		150		Ω
Line transient	V_{TRLN} (3)	V_{IN} = 1.4V to 5.5V in 10us, I_{OUT} = 1mA, T_A = 25ºC		18	30	mV
		V_{IN} = 5.5V to 1.4V in 10us, I_{OUT} = 1mA, T_A = 25ºC		18	30	mV
Load transient	V_{TRLD} (3)	I_{OUT} = 1mA to 800mA in 10us V_{IN} = 1.6V, T_A = 25ºC		120	180	mV
		I_{OUT} = 800mA to 1mA in 10us V_{IN} = 1.6V, T_A = 25ºC		80	120	mV

Electrical Characteristics (Continued)

(Unless otherwise noted, V_{IN} = 1.4V, V_{BIAS} = 3.3V, I_{OUT} = 1mA, C_{IN} = 1μF, C_{OUT} = 2.2μF, C_{BIAS} = 0.1uF, T_A = -40ºC~85ºC.Typical values are at. T_A = 25ºC)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Turn-On Time	t_{ON}	From Assertion of V_{EN} to V_{OUT} = 98%$V_{OUT(NOM)}$		120		μs
Thermal Shutdown Temperature	T_{SD}(3)	Temperature Increasing		165		℃
Thermal Shutdown Released Temperature	T_{SR}(3)	Temperature Decreasing		145		℃

Notes:

1: The maximum input voltage should take into account the maximum power consumption ($P_{D(MAX)}$).The calculation formula is as follows:

$$\mathbf{P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT}}$$

The maximum power consumption of the circuit is 640mW.

$$\mathbf{V_{IN(MAX)} = 640mW / I_{OUT} + V_{OUT}}$$

For example:

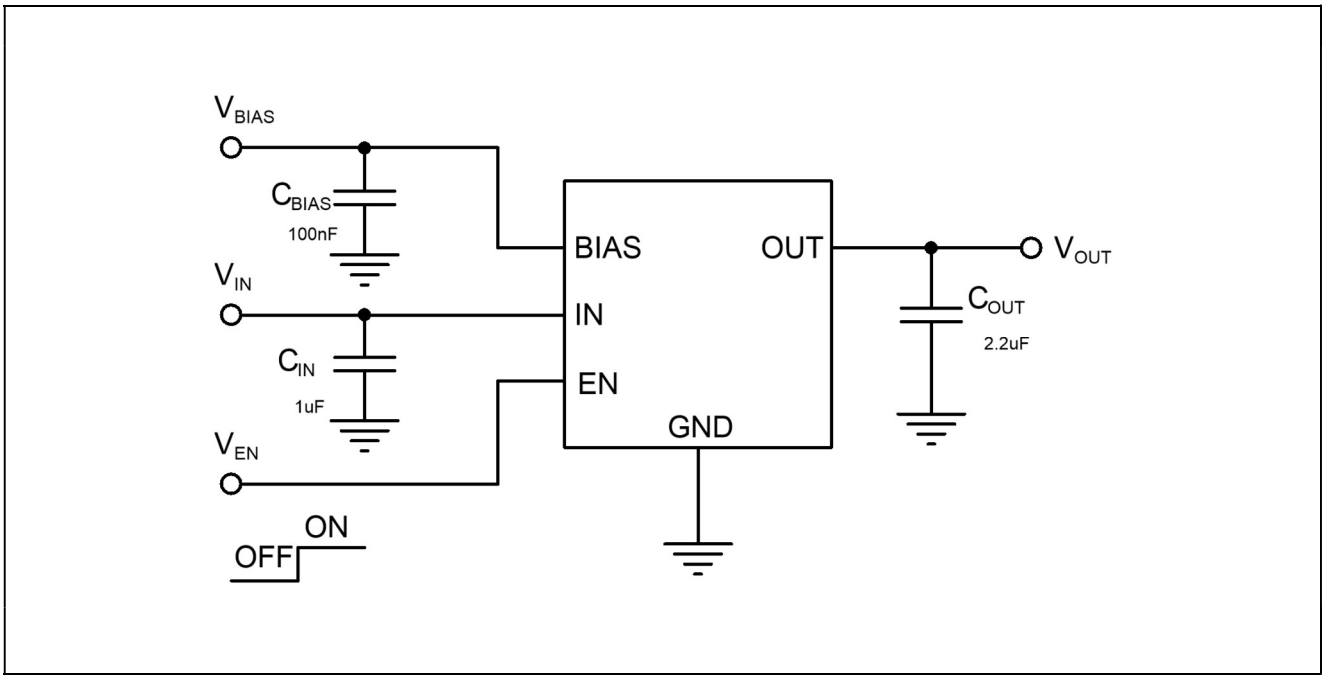
If V_{OUT} = 1.1V, I_{OUT}=800mA, the maximum input voltage is $V_{IN(MAX)}$ = 640mW / 800Ma + 1.1 = 1.9V

2: V_{DROP} FT test method: test the V_{OUT} voltage at V_{SET} + $V_{DROPMAX}$ with output current.

3: Guaranteed by design and characterization. not a FT item.

4: Since the power on process of BIAS needs a large current, the BIAS input voltage should have a current driving capacity of more than 100mA.

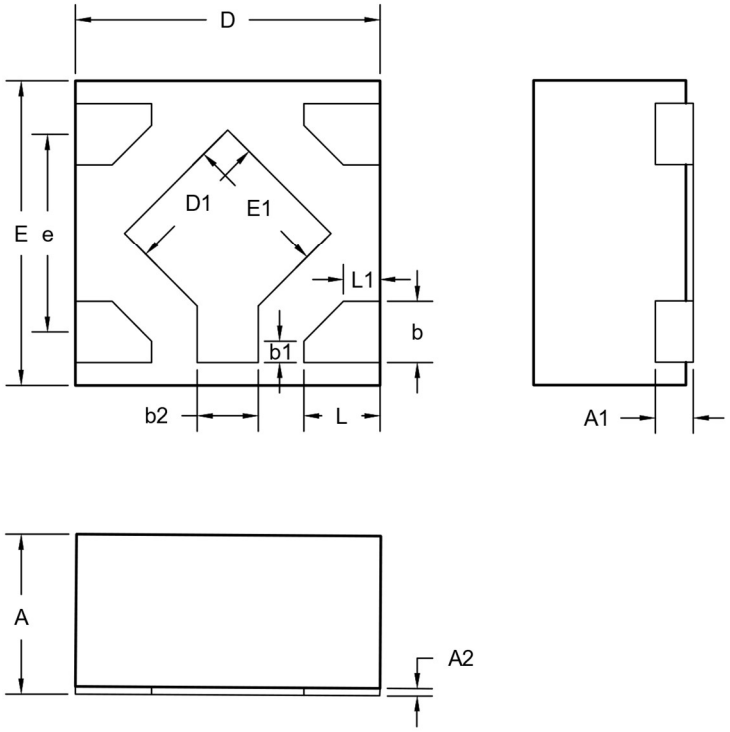
Application Circuits



Note*: If BIAS input series resistor is used, it is recommended no greater than 20Ω.

Package Dimension

DFN4 (1.2mm x 1.2mm)

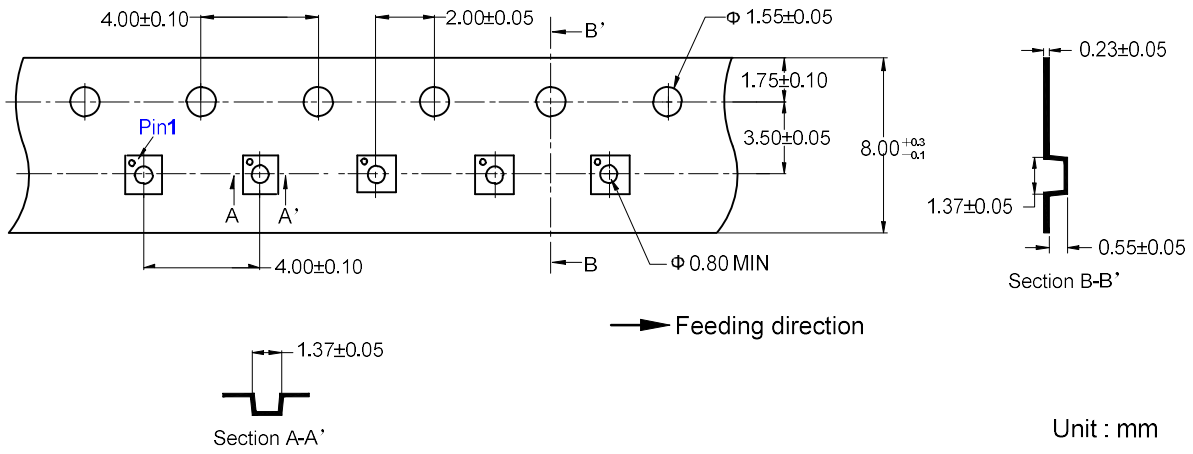


COMMON DIMENSIONS

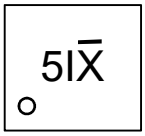
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.35	0.40	0.45
A1		0.13REF	
A2	0.00	0.02	0.05
b	0.25	0.30	0.35
b1		0.12REF	
b2	0.15	0.20	0.25
D	1.15	1.20	1.25
D1	0.58	0.63	0.68
E	1.15	1.20	1.25
E1	0.58	0.63	0.68
e		0.8BSC	
L	0.25	0.30	0.35
L1		0.12REF	

Reel



Marking



5I=Part Version

X=Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2019-1-24	Preliminary Version	Liuyg	Liuyg	Zhujl
1.1	2019-02-27	Add T_{TSD}&T_{TSR} in EC Table, Revise Test Condition of I_{LIM}, Revise the Functional Description	Liuyg	Liuyg	Liujy
1.2	2019-03-27	Update V_{DROP}	Liuyg	Liuyg	Liujy
1.3	2020-03-17	Add MSL Level	Liuyg	Liuyg	Liujy
1.4	2021-06-02	Add Note 4 for I_{Q_ON}	Liuyg	Liuyg	Liujy
1.5	2024-03-03	Update Typeset	Shibo	Liuyg	Liujy
1.5.a	2026-09-01	Update C_{OUT} Value	Yangxx	Liuyg	Liujy