5V to 100V Input, 200mA Synchronous Step-Down Regulator

General Description

The ET81181 is a highly integrated, wide input voltage, 200mA output synchronous buck convertor. The device is optimized to operate with minimum external component counts.

This convertor adopts adaptive constant-on-time (ACOT) structure, and provides a fast transient response. It also supports both low-equivalent series resistance (ESR) output capacitors and ultra-low ESR ceramic capacitors with no external compensation components.

During light load operation, ET81181 operates in pulse frequency modulation (PFM) mode, which maintains high efficiency.

ET81181 is available in a SOT23-6 package.

Features

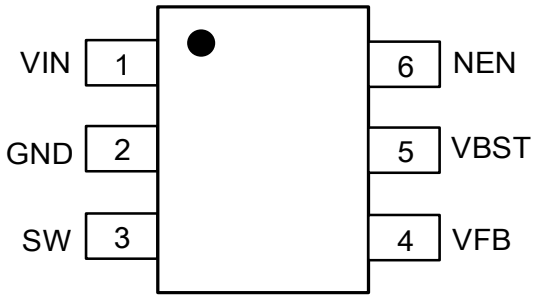
- 200mA Converters Integrated 3.5Ω and 1.5Ω FET
- ACOT Mode Control with Fast Transient Response
- Wide Input Voltage Range: 5V to 100V
- FB Voltage Fixed Voltage 1V Typical
- PFM Mode During Light Load Operation
- 250KHz Switching Frequency
- Start-up from Pre-Biased Output Voltage
- Cycle-by-Cycle Over-current Limit
- Hiccup-mode Over-current Protection
- Non-Latch UVP and TSD Protections
- Fixed Soft Start Time: 0.7ms
- Part No. and Package

Part No.	Package	Packing Option	MSL
ET81181	SOT23-6	3K / Reel	3

Applications

- LED Lighting
- Portable Device
- Motor Driver Power Supply

Pin Configuration

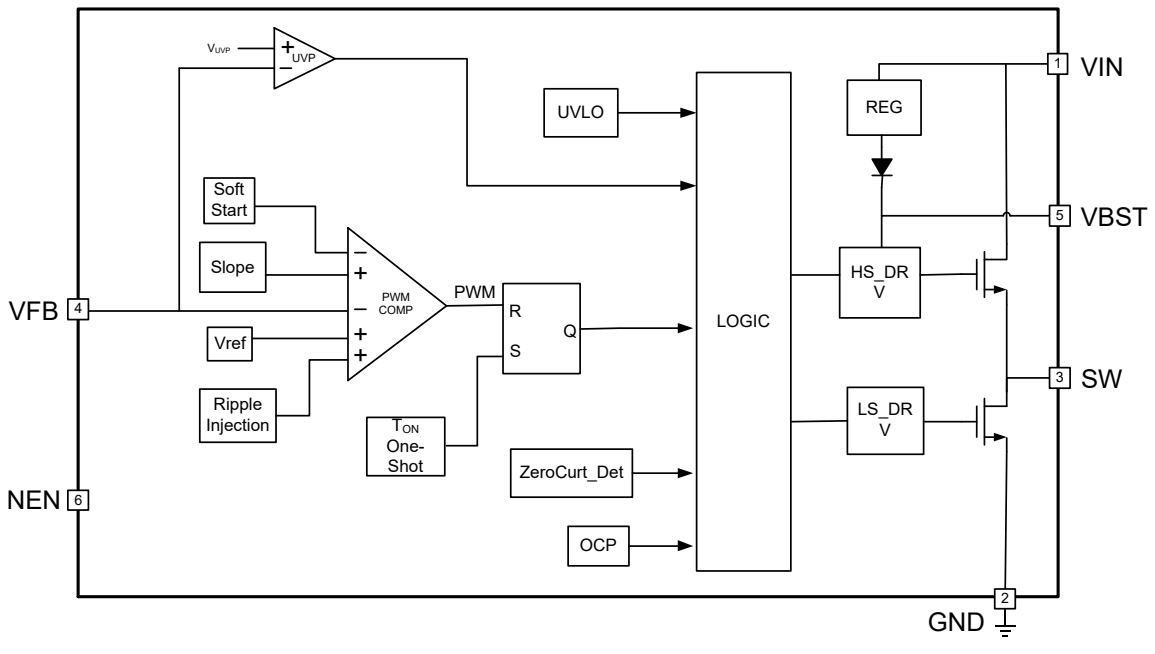


Top View

Pin Function

Pin Name	Pin No.	I/O	Description
VIN	1	I	Input voltage supply pin, also the drain terminal of high-side power NFET.
GND	2	Ground	Ground pin of controller circuit, as well as source terminal of low-side power NFET. Connect sensitive VFB to this GND at a single point.
SW	3	O	Switch node connection between low-side NFET and high-side NFET.
VFB	4	I	Output voltage feedback pin. Connect to output voltage with feedback resistor divider.
VBST	5	O	Power supply of high-side NFET control circuit. Connect 0.1μF capacitor between VBST and SW pins.
NEN	6	I	Connect to GND or floating.

Block Diagram



Functional Description

Overview

The ET81181 is highly integrated, 200mA synchronous Buck convertor. It employs adaptive constant on time (ACOT) mode, and supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of this device can reduce the output capacitance.

Adaptive On-Time Control and PWM Operation

The main control mode of ET81181 is pulse width modulation (PWM) with ACOT structure. This control mode control can achieve pseudo-fixed frequency and stable operation with both low-ESR and ceramic output capacitors.

The high-side MOSFET is turned on at the beginning of each cycle. When one shot timer expires, the high-side power FET is turned off. This one shot duration is set proportional to input voltage, VIN, and inversely proportional to the output voltage, VO, to achieve pseudo-fixed frequency over the input voltage range, hence it is called adaptive constant on-time control. The one-shot timer is reset and the high-side power FET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is generated to emulate output ripple, eliminating the need for ESR of output capacitor.

Pulse Frequency modulation

The ET81181 is designed with pulse frequency modulation mode to achieve high efficiency during light load condition. As the output current decreases from heavy load condition, the inductor current also deceases and eventually comes to zero, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side power FET is turned off when the zero inductor current is detected. As the load current further decreases the convertor enters into discontinuous conduction mode. The on-time is almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps efficiency high in light load condition. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{sw}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

In PFM mode, each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the VFB voltage falls below the threshold voltage. As the output current decreases, the sleep time between switching pulses increases.

Soft Start and Pre-Biased Soft Start

The ET81181 is designed with an internal 1ms soft-start. When the VIN is plugged in, the reference voltage of PWM comparator begins to rise from zero.

If the output capacitor is pre-biased at start-up, the device begins to switch and start ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the convertors ramp up smoothly into regulation point.

Current Protection

The over-current limit (OCL) is implemented by using cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET drain to source voltage during its on-state. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-state of high-side FET, the switch current increases at a linear rate determined by V_{IN}, V_{OUT}, and the inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the monitored current is above the OCL level, the convertor keeps low-side FET on and prevents the creation of a new set pulse, even the voltage feedback loop requires one, until the current level decreases to OCL level or lower. In next switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the load current is higher than the current available from the convertor. This may cause the output voltage to fall. When the V_{FB} voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device will shut down after the UVP delay time and re-start after the hiccup time (typically 6ms).When the over current condition is removed, the output voltage returns to the regulated value.

Under-voltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When input voltage increases up to the upper threshold of UVLO, it begins to switch.

Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 170°C), the device is shut off. When the temperature falls to about 140°C or below, the convertor begins to switch.

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

Parameters		Min	Max	Unit
Input Voltage	VIN	-0.3	110	V
	VIN(10us transient)	-0.3	115	V
	NEN	-0.3	6.5	V
	BST	-0.3	114	V
	BST(10ns transient)	-0.3	119	V
	BST(VS SW)	-0.3	6.5	V
	FB	-0.3	6.5	V
	SW	-2	110	V
	SW(10ns transient)	-3.5	117	V
V_{ESD}	Human Body Model (JEDEC JS-001)		±2000	V
	Charged Device Model(JESD22-C101)		±1000	V
T_J	Junction Temperature	-40	+150	°C
T_{STG}	Storage Temperature	-65	+150	°C
T_L	Lead Temperature (Soldering 10 sec)		+260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameters		Min	Typ	Max	Unit
V_{IN}	Supply Input Voltage Range		5		100	V
V_I	Input Voltage Range	BST	-0.1		104	
		BST(10ns transient)	-0.1		107	
		BST (VS SW)	-0.1		6	
		NEN	-0.1		6	
		FB	-0.1		5.5	
		SW	-1.8		100	
		SW(10ns transient)	-3.5		105	
I_{OUT}	Output current Range			200		mA
T_J	Operating Junction Temperature		-40		150	°C
T_A	Ambient Temperature		-40		125	°C

Electrical Characteristics

V_{IN} = 48V, T_A = –40°C to 125°C, (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Current						
I_{VIN}	Operating–non-switching Supply Current	V_{IN} current, V_{FB} = 2V		350		μA
V_{FB} Voltage and Discharge Resistance						
V_{FBTH}	V_{FB} Threshold Voltage	V_O = 12V, I_O = 10mA, PFM operation		1.005		V
	V_{FB} Threshold Voltage	V_O = 12V, Continuous mode operation	0.99	1	1.01	V
I_{VFB}	V_{FB} Input Current	V_{FB} = 1V			0.1	μA
MOSFET						
$R_{DS(ON)H}$	High-side Switch Resistance	T_A = 25°C, V_{BST} – SW = 5V		3.5	9	Ω
$R_{DS(ON)L}$	Low-side Switch Resistance	T_A = 25°C		1.5	3.4	Ω
Current Limit						
I_{OCL}	Current Limit	Valley current, V_{OUT} = 12V, L_1 =150μH		280		mA
Thermal Shutdown						
T_{SHDN}	Thermal Shutdown Threshold(1)	Shutdown temperature		170		°C
		Hysteresis		30		
ON-Time Timer Control						
$t_{OFF(MIN)}$	Minimum off Time	V_{FB} = 0.5V		120		ns
Soft Start						
t_{SS}	Soft Start Time	Internal soft-start time		0.7		ms
Frequency						
F_{SW}	Switching Frequency	V_{IN} = 48V, V_O = 12V, CCM mode		250		kHz
Output Under-voltage and Over-voltage Protection						
V_{UVP}	Output UVP Threshold	Hiccup detect (H > L)		60		%
t_{HICCUP_WAIT}	Hiccup on Time	V_{IN}=48V		0.7		ms
t_{HICCUP_RE}	Hiccup Time Before Restart	V_{IN}=48V		6		ms
UVLO						
V_{UVLO}	UVLO Threshold	Wake up V_{IN} voltage		4.5	4.8	V
		Shutdown V_{IN} voltage	3.5	3.8		
		Hysteresis V_{IN} voltage		0.7		

Note(1) Not production tested, design assurance.

Application and Implementation

Note

Information in the following applications sections is not part of the ETEK component specification. ETEK does not warrant its accuracy or completeness and Customers should be responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

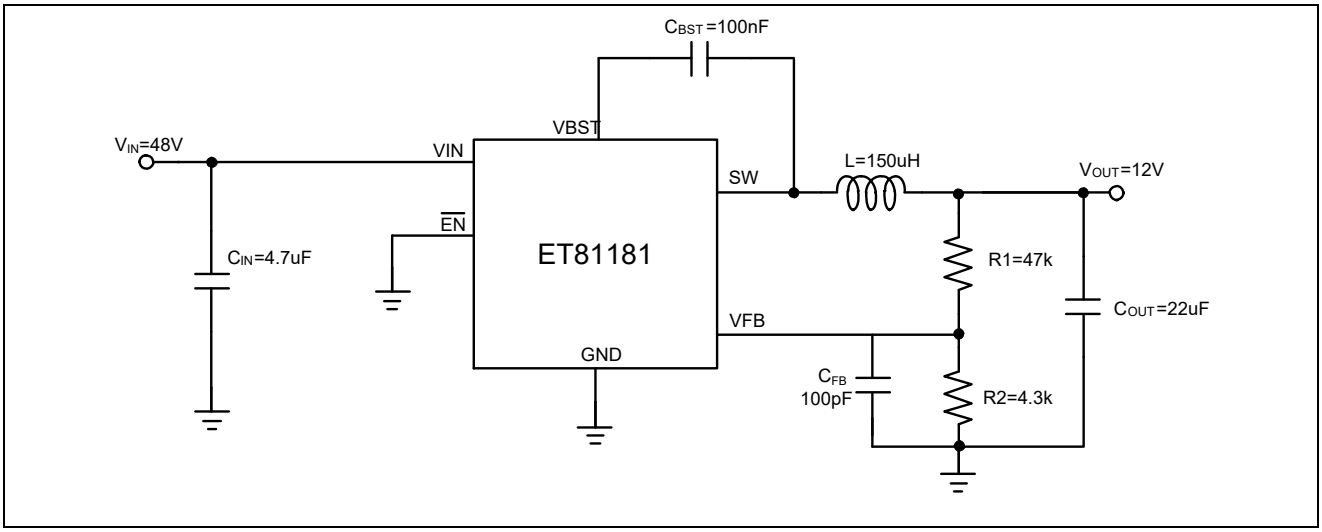
Application Information

ET81181 is typical step-down DC-DC converter. It's typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 200mA. The following design procedure can be used to select component values for the ET81181.

Typical Application

The application schematic below was developed to meet the previous requirements. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

The figure shows 12V output converter schematics.



V_{OUT}=12V/200mA Reference Design

Design Requirements

This table below shows the design parameters for this application.

Table1. 48V to 12V application condition

Parameter	Example Value
Input voltage range	48V
Output voltage	12V
Transient response, 200mA load step	ΔV_{OUT} = ±2.5 %
Output ripple voltage@200mA load	≤ 0.5% * VOUT
Output current rating	200mA
Operating frequency	250KHz

Detailed Design Procedure

Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. ETEK recommends using 1% tolerance or better divider resistors. Start by using Equation 2 to calculate VOUT.

If customers want to improve efficiency at very light loads，we recommend using larger value resistors. High value of resistor will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 1 \times (1 + \frac{R1}{R2}) \quad (2)$$

Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_p = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

The overall loop gain is set by the output set-point resistor divider network and the internal gain of the device at low frequencies. The low frequency phase is 170°C. At the output filter pole frequency, the gain rolls off at a －40dB per decade rate and the phase drops rapidly. The inductor and capacitor for the output filter should be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit.

Example for V_{FB}=1V

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 4,Equation 5, and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$I_{p\text{-}p} = \frac{V_{OUT}}{V_{IN}(MAX)} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{sw}} \quad (4)$$

$$I_{peak} = I_O + \frac{I_{p\text{-}p}}{2} \quad (5)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{P-P}^2} \quad (6)$$

For this design example, the calculated peak current is 250mA and the calculated RMS current is 200mA.

The inductor should be used with a peak current rating of 250mA and an RMS current rating of 200mA.

The capacitor value and ESR determines the amount of output voltage ripple. The ET81181 is intended for use with ceramic or other low ESR capacitors. We recommend using values range from 60uF to 150uF. Equation 7 determines the required RMS current rating for the output capacitor

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{sw}} \quad (7)$$

One 22uF output capacitors are used for this design. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286A and each output capacitor is rated for 0.3A.

Input Capacitor Selection

The ET81181 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. We recommend a ceramic capacitor over 4.7uF for the decoupling capacitor. An additional 0.1uF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

Bootstrap Capacitor Selection

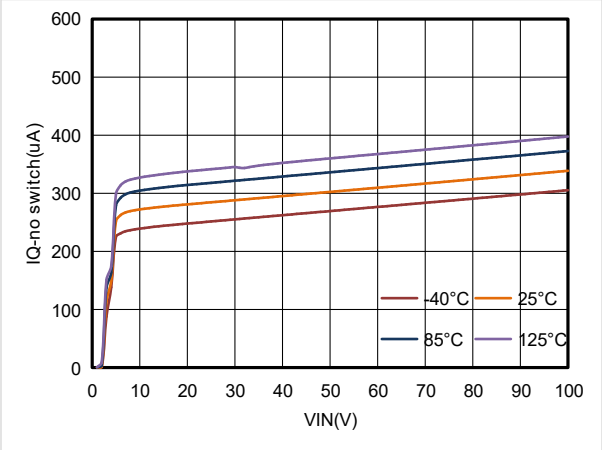
A 0.1uF ceramic capacitor must be connected between the VBST to SW pin for proper operation. We recommend using a ceramic capacitor.

Power Supply Recommendations

ET81181 is designed to operate from input supply voltage in the range of 5V to 100V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 75%. Using that criteria, the minimum recommended input voltage is VO/0.75.

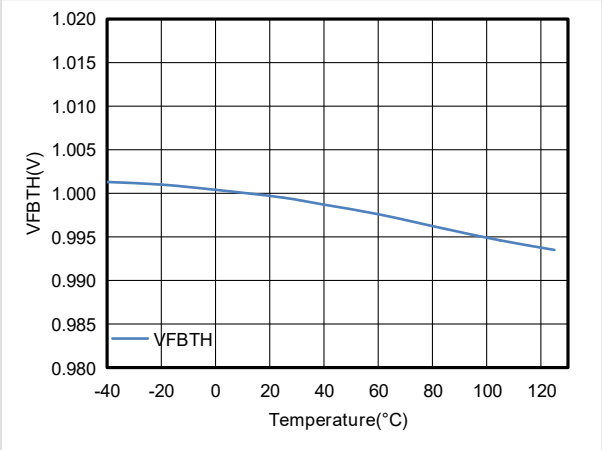
Application Curves

V_{IN} = 48V, V_{OUT} = 12V, L=150uH(unless otherwise noted)



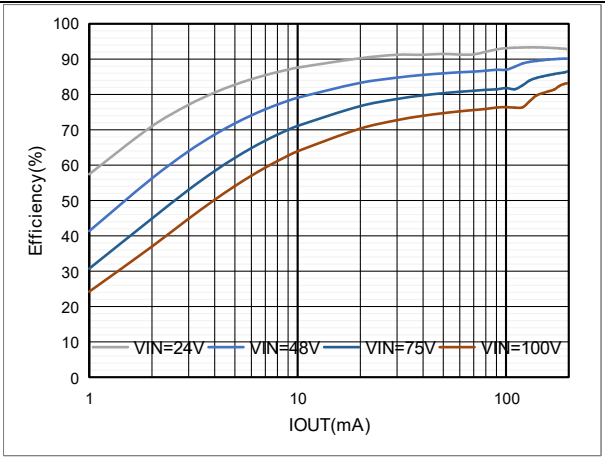
V_{OUT} = 12V

Figure1. Operating–non-switching Supply Current vs VIN in different Temperature



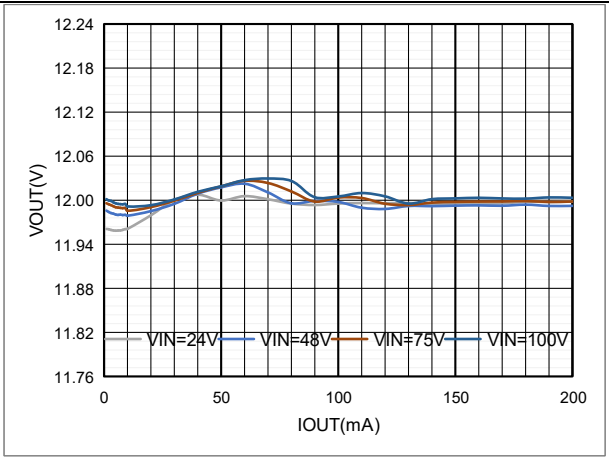
V_{IN} = 48V, V_{OUT} = 12V

Figure2. VFBTH vs Temperature



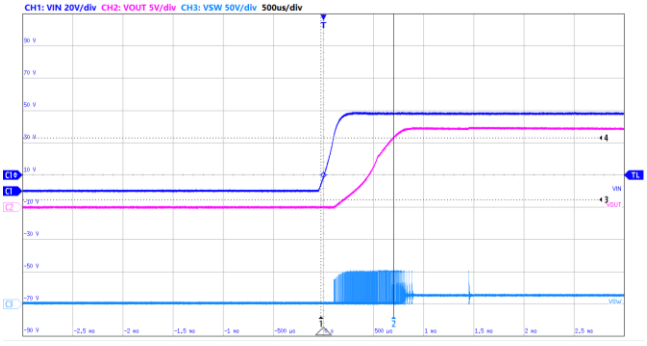
V_{OUT} = 12V, L=150uH, DCR=350mΩ

Figure3. Efficiency vs IOUT



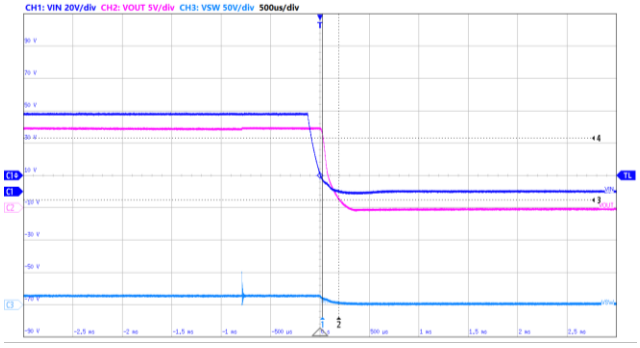
V_{OUT} = 12V

Figure4. VOUT Voltage vs IOUT



V_{IN} = 0V to 48V, V_{OUT} = 12V, I_{OUT} = 0mA

Figure5. Startup from V_{IN}

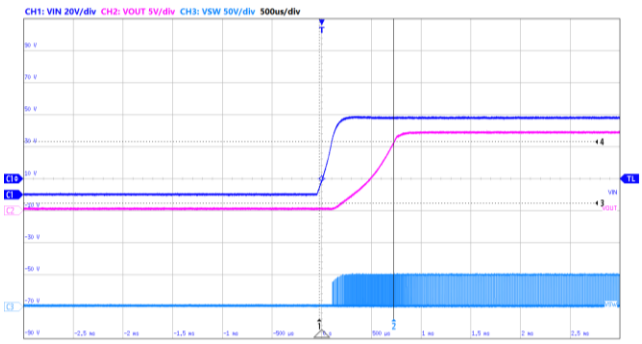


V_{IN} = 48V to 0V, V_{OUT} = 12V, I_{OUT} = 0mA

Figure5. Shutdown from V_{IN}

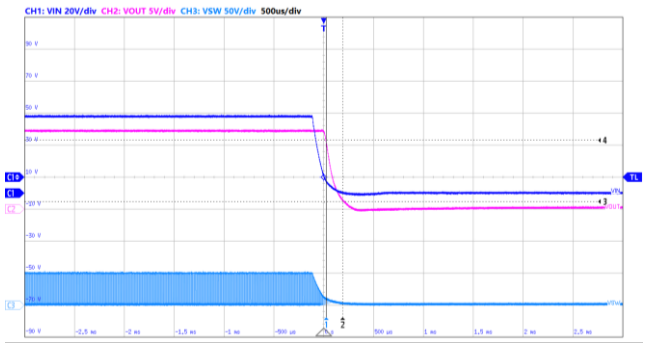
Application Curves(Continued)

V_{IN} = 48V, V_{OUT} = 12V, L=150uH(unless otherwise noted)



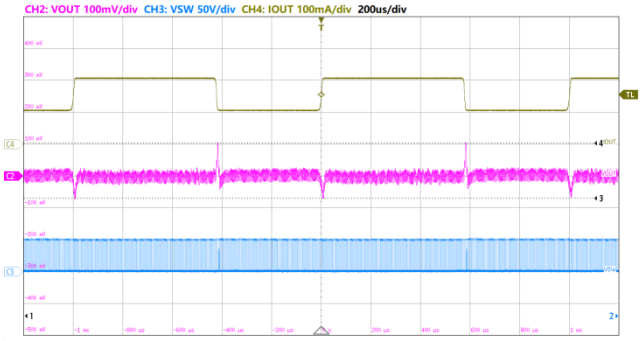
V_{IN} = 0V to 48V, V_{OUT} = 12V, I_{OUT} = 200mA

Figure7. Startup from V_{IN}



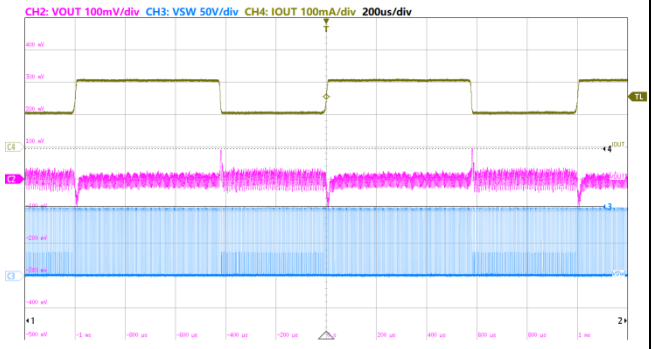
V_{IN} = 48V to 0V, V_{OUT} = 12V, I_{OUT} = 200mA

Figure8. Shutdown from V_{IN}



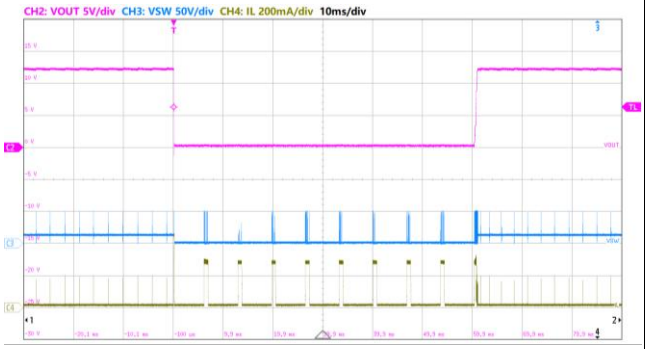
V_{IN} = 48V, V_{OUT} =12V, I_{OUT} = 100mA to 200mA

Figure9. Load Transient



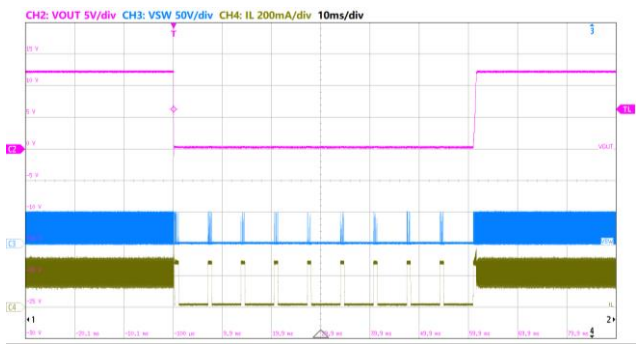
V_{IN} = 100V, V_{OUT} =12V, I_{OUT} = 100mA to 200mA

Figure10. Load Regulation



V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 0mA to Short

Figure11. Short Circuit Protection

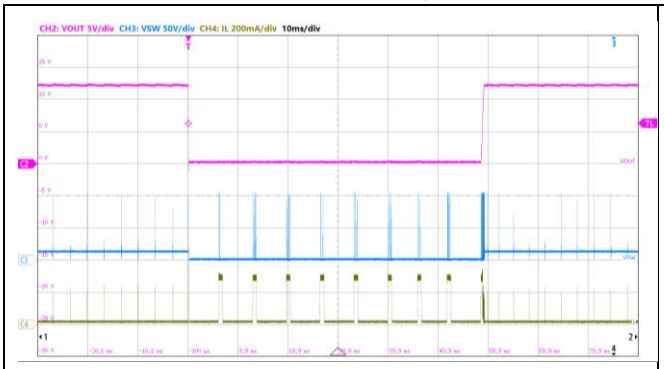


V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 200mA to Short

Figure12. Short Circuit Protection

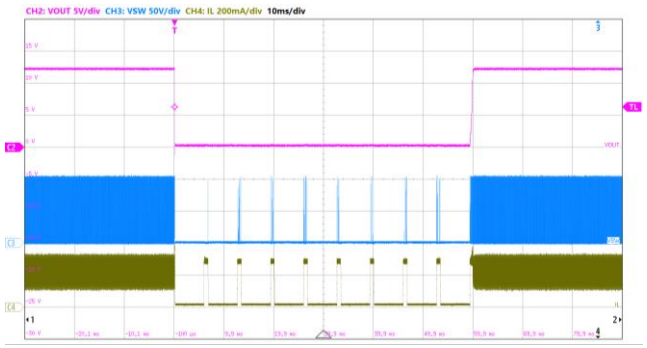
Application Curves(Continued)

V_{IN} = 48V, V_{OUT} = 12V, L=150uH(unless otherwise noted)



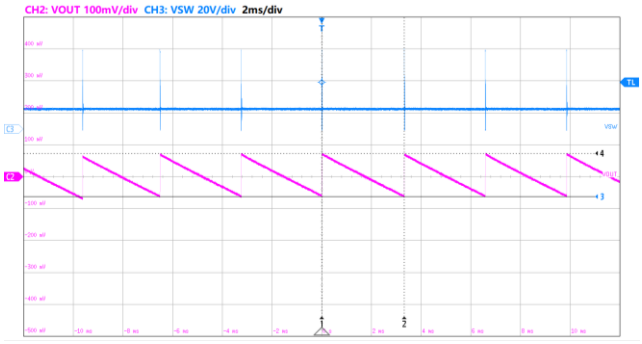
V_{IN} = 100V, V_{OUT} = 12V, I_{OUT} = 0mA to Short

Figure13. Short Circuit Protection



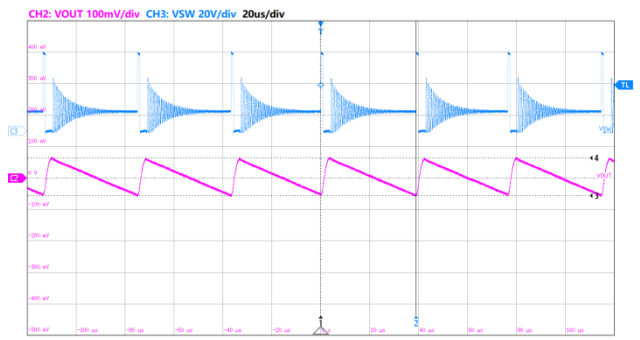
V_{IN} = 100V, V_{OUT} = 12V, I_{OUT} = 200mA to Short

Figure14. Short Circuit Protection



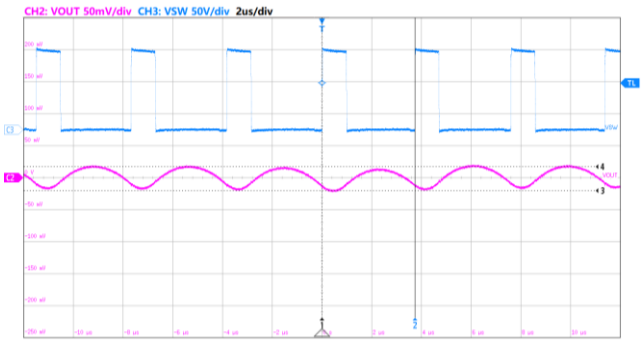
V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 0mA

Figure15. Output Voltage Ripple



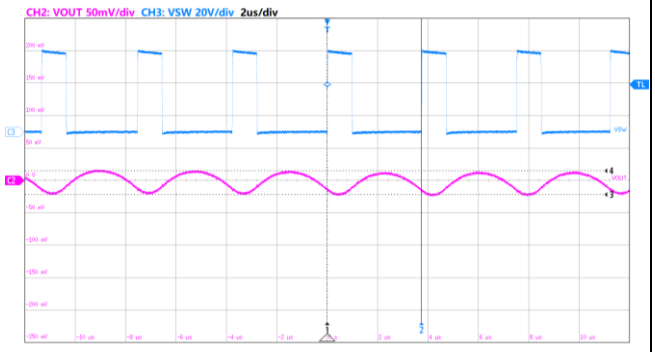
V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 10mA

Figure16. Output Voltage Ripple



V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 100mA

Figure17. Output Voltage Ripple

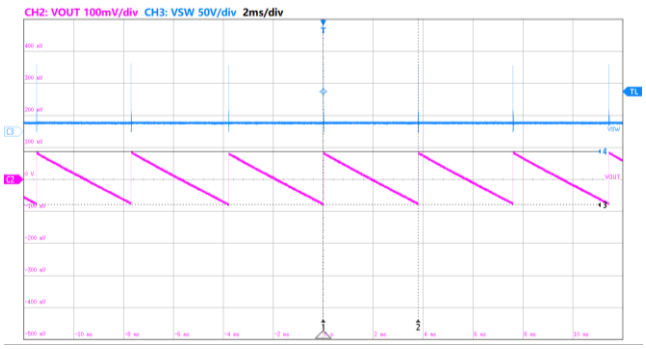


V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 200mA

Figure18. Output Voltage Ripple

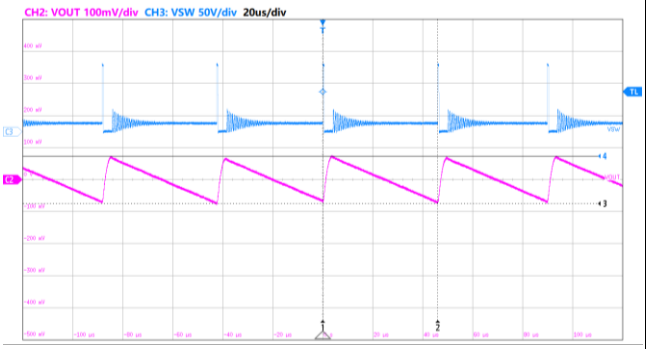
Application Curves(Continued)

V_{IN} = 48V, V_{OUT} = 12V, L=150uH(unless otherwise noted)



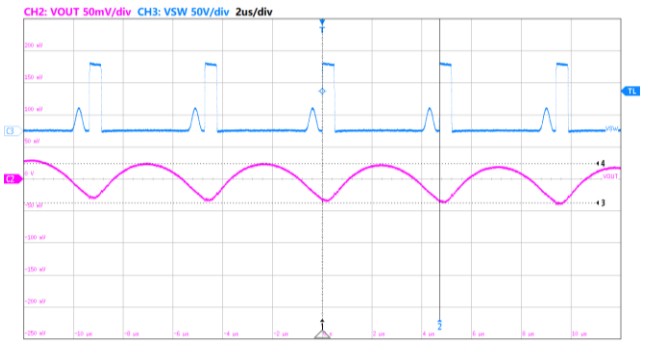
V_{IN} = 100V, V_{OUT} = 12V, I_{OUT} = 0mA

Figure19. Output Voltage Ripple



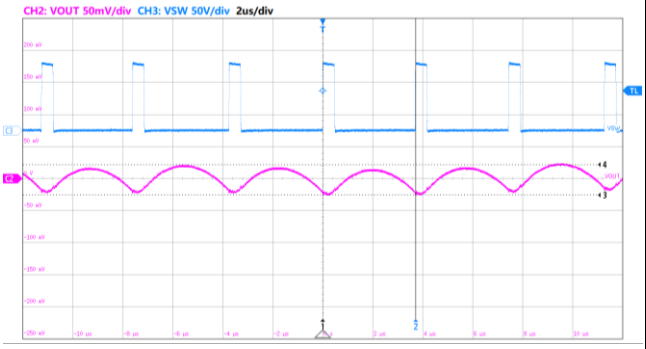
V_{IN} = 100V, V_{OUT} = 12V, I_{OUT} = 10mA

Figure20. Output Voltage Ripple



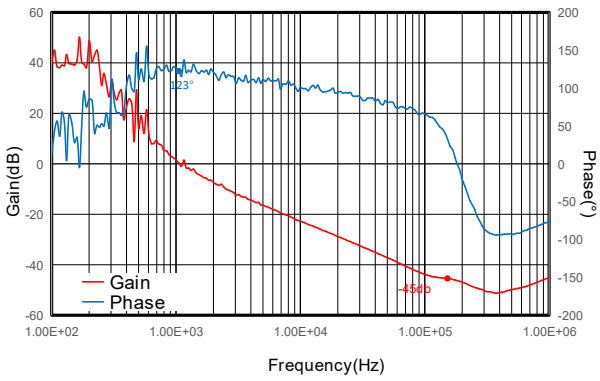
V_{IN} = 100V, V_{OUT} = 12V, I_{OUT} = 100mA

Figure21. Output Voltage Ripple



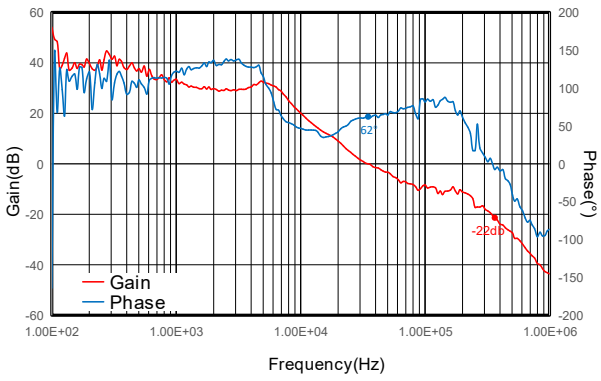
V_{IN} = 100V, V_{OUT} = 12V, I_{OUT} = 200mA

Figure22. Output Voltage Ripple



V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 0mA

Figure23. Bode plot

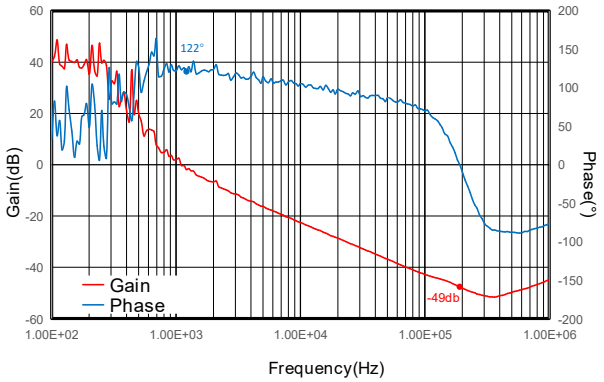


V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 200mA

Figure24. Bode plot

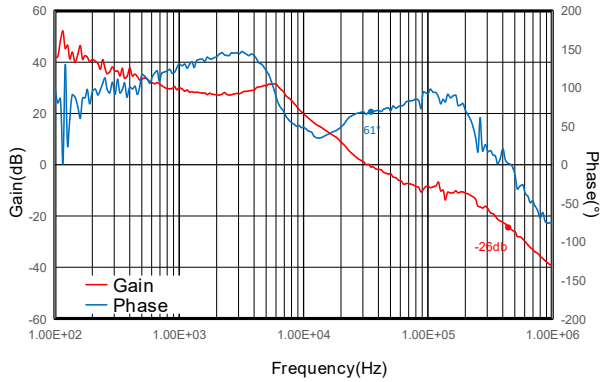
Application Curves(Continued)

V_{IN} = 48V, V_{OUT} = 12V, L=150uH(unless otherwise noted)



V_{IN} = 80V, V_{OUT} = 12V, I_{OUT} = 0mA

Figure25. Bode plot

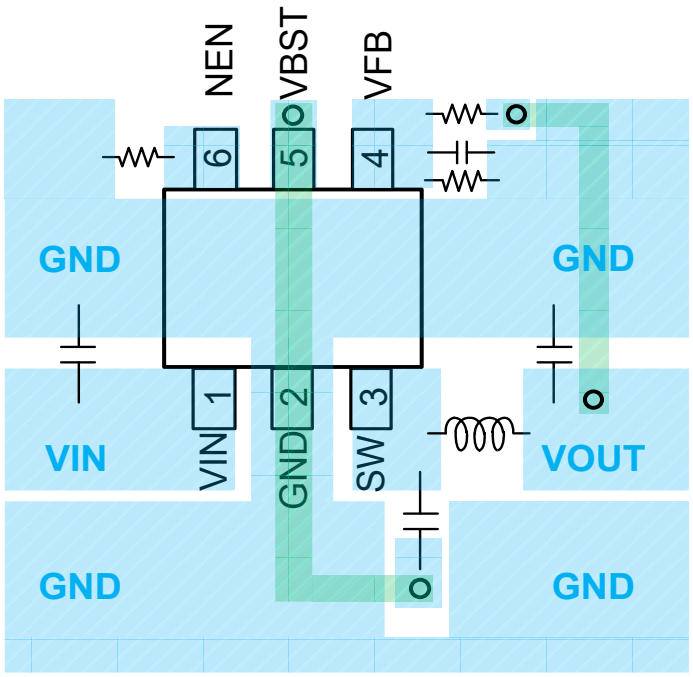


V_{IN} = 80V, V_{OUT} = 12V, I_{OUT} = 200mA

Figure26. Bode plot

Layout

Layout Example



* Circuit diagram is for reference only.

Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance and better heet dissipation.

2. The input capacitor and output capacitor should be placed as close to the device as possible to minimizetrace impedance.

3. Provide sufficient vias for the input capacitor and output capacitor.

4. Keep the SW trace physically short and wide to minimize radiated emissions.

5. Do not allow switching current to flow under the device.

6. A separate VOUT path should be connected to the upper feedback resistor.

7. Make a Kelvin connection to the GND pin for the feedback path.

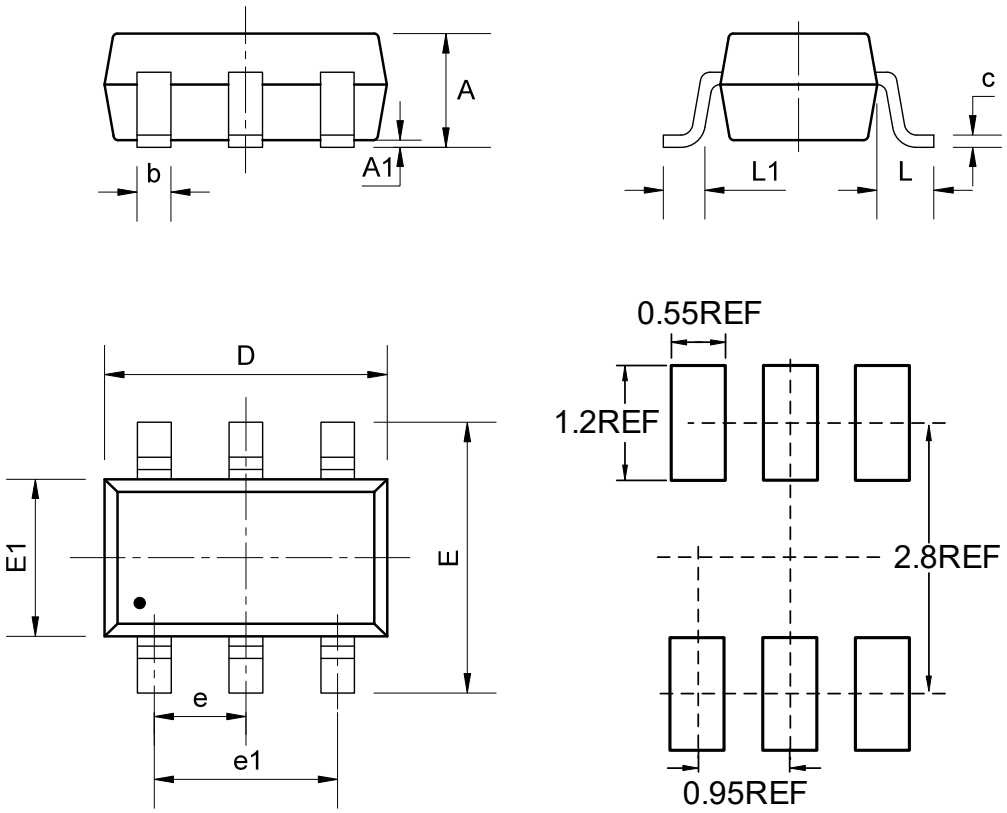
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.

9. The trace of the VFB node should be as small as possible to avoid noise coupling.

10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize itstrace impedance.

Package Dimension

SOT23-6



COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.25
A1	0	-	0.15
b	0.36	-	0.50
c	0.12	-	0.20
D	2.75	2.9	3.05
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
E	2.60	2.80	3.00
E1	1.45	1.6	1.75
L	0.59REF		
L1	0.35	0.45	0.60

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2025-04-21	Preliminary Version	Xielh	Xielh	Liujy
0.1	2025-10-21	Update Typeset	Liuc	Xielh	Liujy
1.0	2025-12-8	Initial Version	Liuc	Xielh	Liujy
1.1	2025-12-15	Update T_A&T_J and Typical Application	Liuc	Xielh	Liujy
1.2	2026-7-15	Update AMR	Liuc	Gexj	Liujy