Single Bus Buffer Gate with 3-State Output

General Description

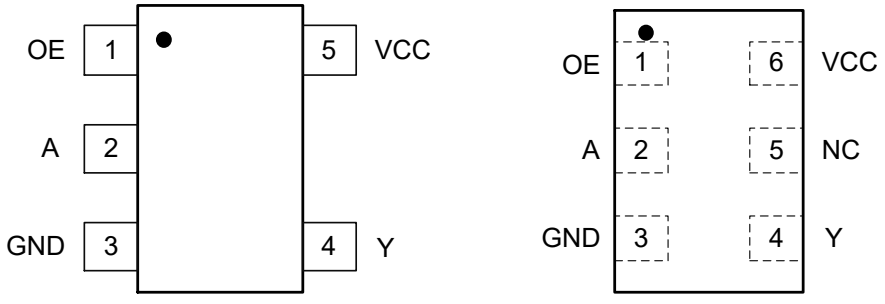
The ET74AUP1G126 device is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable (OE) input is low. When OE is high, data is passed from the A input to the Y output.

Features

- Designed for 0.8V to 3.6V V_{CC} Operation
- Over-Voltage Tolerant Inputs Accept Voltages to 3.6V
- ±4mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- These Devices are Pb-Free and RoHS Compliant
- ESD Protection Complies with JESD22 Standard
  -- HBM: ±4000V Pass (JEDEC JS-001)
  -- CDM: ±1000V Pass (JEDEC JS-002)
- Latch-up Performance Exceeds ±100mA per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
ET74AUP1G126	SC70-5 (1.3mm × 2.1mm)	Tape and Reel, 3K/Reel	1
ET74AUP1G126T	SOT23-5 (1.6mm × 2.9mm)	Tape and Reel, 3K/Reel	3
ET74AUP1G126Y	DFN6 (1.0mm × 1.5mm)	Tape and Reel, 3K/Reel	1

Pin Configuration



SOT23-5/SC70-5 DFN6

Figure1. Pin Configuration

Pin Function

SC70-5/ SOT23-5

Pin No.	Pin Name	Function
1	OE	Enable Input
2	A	Input
3	GND	Ground
4	Y	Output
5	VCC	Supply Voltage

DFN6

Pin No.	Pin Name	Function
1	OE	Enable Input
2	A	Input
3	GND	Ground
4	Y	Output
5	NC	No Connect
6	VCC	Supply Voltage

Block Diagram

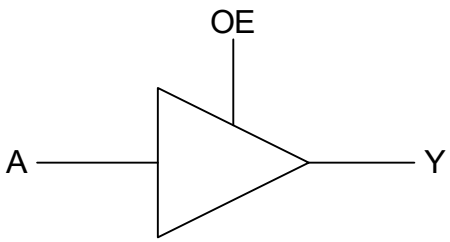


Figure2. Logic Symbol

Functional Table

Input		Output
OE	**A**	**Y**
H	L	L
H	H	H
L	X	Z

Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		-0.5 to 4.6	V
V_I	DC Input Voltage		-0.5 ≤ V_I ≤ 4.6	V
V_O	DC Output Voltage Output in Higher or Low State (1)		-0.5 to 4.6	V
I_{IK}	DC Input Diode Current, V_I < GND		-50	mA
I_{OK}	DC Output Diode Current, V_O < GND, V_O > V_{CC}		±50	mA
I_O	DC Output Sink Current		±20	mA
I_{CC}	DC Supply Current per Supply Pin		±50	mA
I_{GND}	DC Ground Current per Supply Pin		±50	mA
T_{STG}	Storage Temperature Range		-65 to 150	°C
T_L	Lead Temperature, Soldering 10 Seconds		260	°C
T_J	Max Junction Temperature		150	°C
V_{ESD}	ESD Classification	Human Body Model (2)	±4000	V
		Charged Device Model (3)	±1000	
I_{LU}	Max Latch Up Current Above V_{CC} and GND at 85°C (4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch up Current Maximum Rating tested per JEDEC JESD78F.

Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
$R_{\theta JA}$	SC70-5	Thermal Characteristics, Thermal Resistance, Junction-to-Air	300	°C/W
	SOT23-5		250	
	DFN6 (1mm × 1.5mm)		440	
P_D	SC70-5	Power Dissipation in Still Air at 85°C	215	mW
	SOT23-5		260	
	DFN6 (1mm × 1.5mm)		150	

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage Operating		0.8	3.6	V
V_I	DC Input Voltage		0	V_{CC}	V
V_O	DC Output Voltage (High or Low State)		0	V_{CC}	V
T_A	Operating Temperature Range		-40	85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 0.8V to 3.6V	0	20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied.

Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Condition	V_{CC}(V)	T_A = 25°C			-40°C ≤ T_A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High-Level Input Voltage		0.8	0.75V_{CC}			0.75V_{CC}		V
			0.9~1.95	0.7V_{CC}			0.7V_{CC}		
			2.3~2.7	1.6			1.6		
			3.0~3.6	2.0			2.0		
V_{IL}	Low-Level Input Voltage		0.8			0.25V_{CC}		0.25V_{CC}	V
			0.9~1.95			0.3V_{CC}		0.3V_{CC}	
			2.3~2.7			0.7		0.7	
			3.0~3.6			0.9		0.9	
V_{OH}	High-Level Output Voltage	I_{OH} = -20uA	0.8~3.6	V_{CC} - 0.1			V_{CC} - 0.1		V
		I_{OH} = -1.1mA	1.1	0.82	1.02		0.77		
		I_{OH} = -1.7mA	1.4	1.11	1.32		1.03		
		I_{OH} = -1.9mA	1.65	1.32	1.58		1.30		
		I_{OH} = -2.3mA	2.3	2.05	2.24		1.97		
		I_{OH} = -3.1mA		1.9	2.22		1.85		
		I_{OH} = -2.7mA	3.0	2.72	2.95		2.67		
		I_{OH} = -4.0mA		2.6	2.92		2.55		
V_{OL}	Low-Level Output Voltage	I_{OL} = 20uA	0.8~3.6			0.1		0.1	V
		I_{OL} = 1.1mA	1.1		0.11	0.33		0.33	
		I_{OL} = 1.7mA	1.4		0.12	0.31		0.37	
		I_{OL} = 1.9mA	1.65		0.11	0.31		0.35	
		I_{OL} = 2.3mA	2.3		0.14	0.31		0.33	
		I_{OL} = 3.1mA			0.19	0.44		0.45	
		I_{OL} = 2.7mA	3.0		0.11	0.31		0.33	
		I_{OL} = 4.0mA			0.16	0.44		0.45	
I_{IN}	Input Leakage Current	V_I = V_{CC} or GND	0~3.6			±0.1		±0.2	uA
I_{OFF}	Power Off Leakage Current	V_I = 3.6V or V_O = 3.6V	0			±0.2		±0.5	uA
I_{CC}	Quiescent Supply Current	V_I = 3.6V or GND	3.6			±0.2		±0.7	uA

AC Electrical Characteristics

$t_r = t_f = 3ns$

Symbol	Parameter	Condition	V_{CC}(V)	T_A = 25°C			-40°C ≤ T_A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay (Figure 3 & 4)	C_L = 15pF[(5)]	0.8	15.3	32.5	106	13.8	259	ns
			1.2	5.8	8.9	16.3	5.3	16.3	
			1.5	4.0	5.6	10.1	3.5	10.9	
			1.8	3.1	4.2	7.8	2.6	8.6	
			2.5	2.1	2.8	5.8	1.8	6.4	
			3.3	1.7	2.2	4.9	1.4	5.4	
		C_L = 30pF[(5)]	0.8	18.3	37.5	130	16.6	323	ns
			1.2	7.0	10.7	19.3	6.4	19.3	
			1.5	4.8	6.9	12.0	4.2	12.9	
			1.8	3.7	5.1	9.2	3.2	10.2	
			2.5	2.6	3.5	6.7	2.2	7.5	
			3.3	2.0	2.2	5.6	1.7	6.3	

Note5: C_L includes probe and jig capacitance.

Capacitance Characteristics

Symbol	Parameter	Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{CC} = 3.6V, V_I = 0V or V_{CC}		2	pF
C_O	output capacitance	V_{CC} = 0V, V_O = GND		3	pF
C_{PD}	Power Dissipation Capacitance (6)	1MHz, V_I = 0V to V_{CC}	V_{CC} = 0.8V	7.6	pF
			V_{CC} = 1.2V	8.1	
			V_{CC} = 1.5V	8.5	
			V_{CC} = 1.8V	8.6	
			V_{CC} = 2.5V	9.0	
			V_{CC} = 3.3V	9.6	

Note6: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}{}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

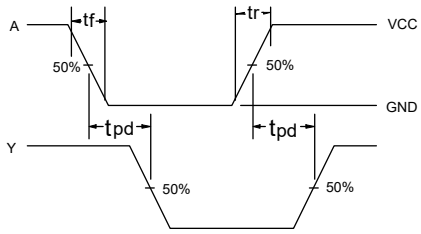
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = sum of outputs.

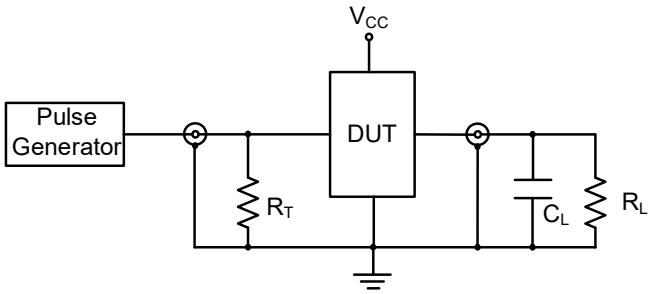
AC Test Circuit



PROPAGATION DELAYS:

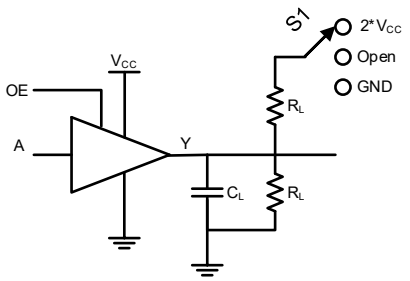
$t_R = t_F$ = 3ns, 10% to 90%; f =1MHz;

Figure3. Switch Waveform



R_T = 50Ω(typ)

Figure4. Test Circuit



Test	Switch
t_{PD}	Open
t_{PZL} t_{PLZ}	$2*V_{CC}$
t_{PZH} t_{PHZ}	GND

Figure5. Output Enable/Disable Time Test Circuit

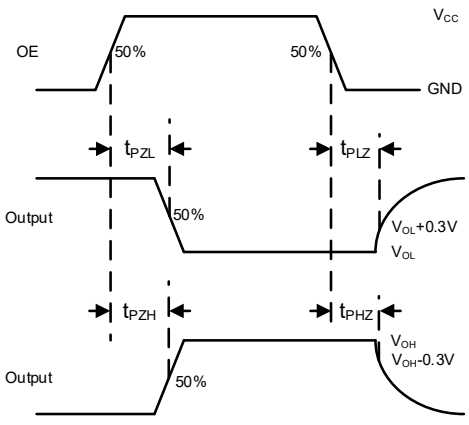
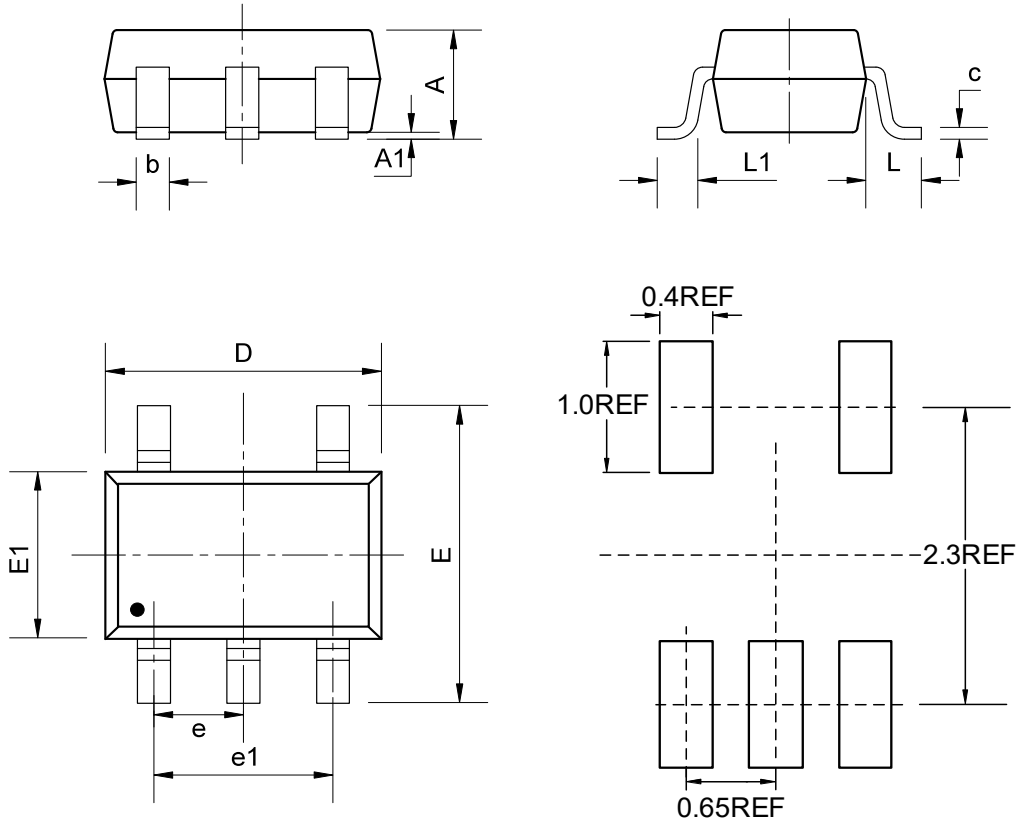


Figure6. Output Enable/Disable Waveform

Package Dimension

SC70-5 (1.3mm × 2.1mm)

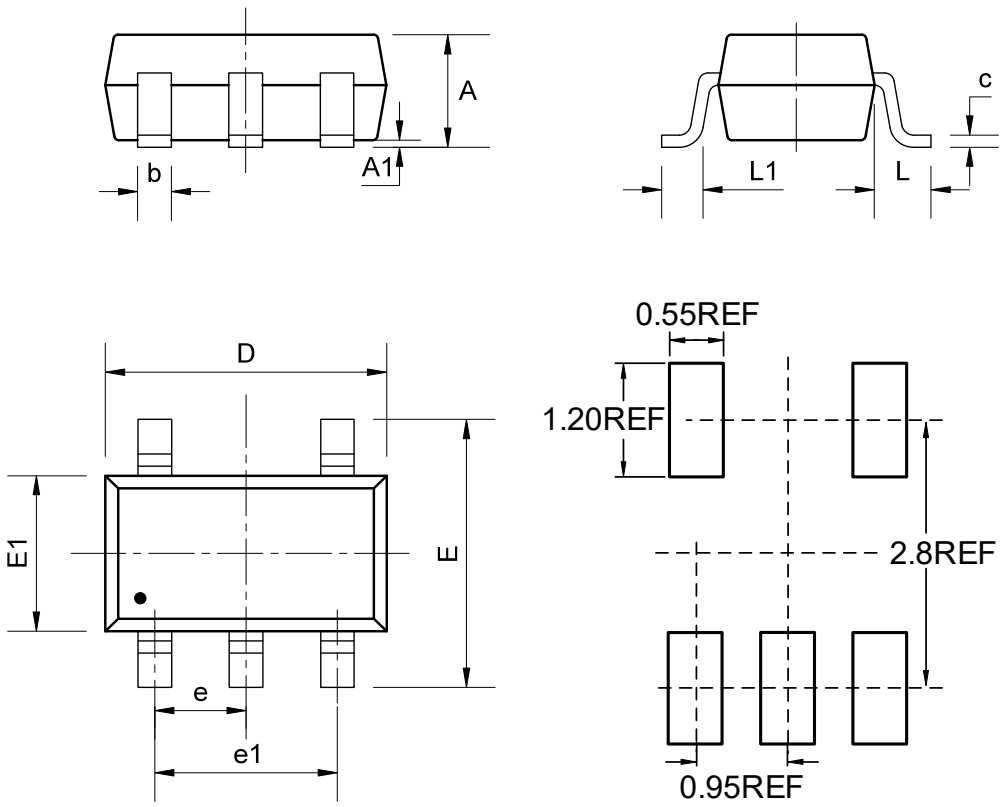


COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	-	0.15
b	0.15	-	0.35
c	0.08	-	0.20
D	2.00	2.10	2.30
e	0.65BSC		
e1	1.30BSC		
E	2.15	2.30	2.50
E1	1.15	1.30	1.45
L	0.50REF		
L1	0.33REF		

SOT23-5 (1.6mm × 2.9mm)

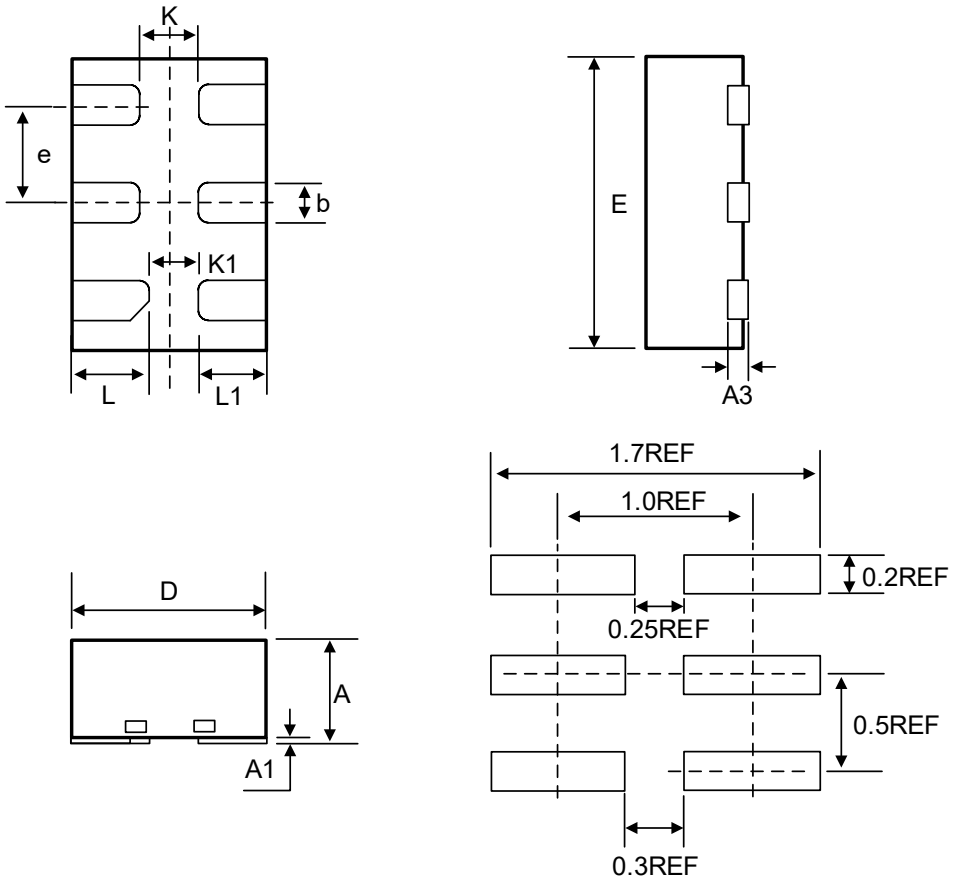


COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.45
A1	0.00	-	0.15
b	0.28	0.35	0.50
c	0.08	0.15	0.22
D	2.75	2.9	3.05
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
E	2.60	2.80	3.00
E1	1.45	1.6	1.75
L	0.60REF		
L1	0.30	0.45	0.60

DFN6 (1.0mm × 1.5mm)



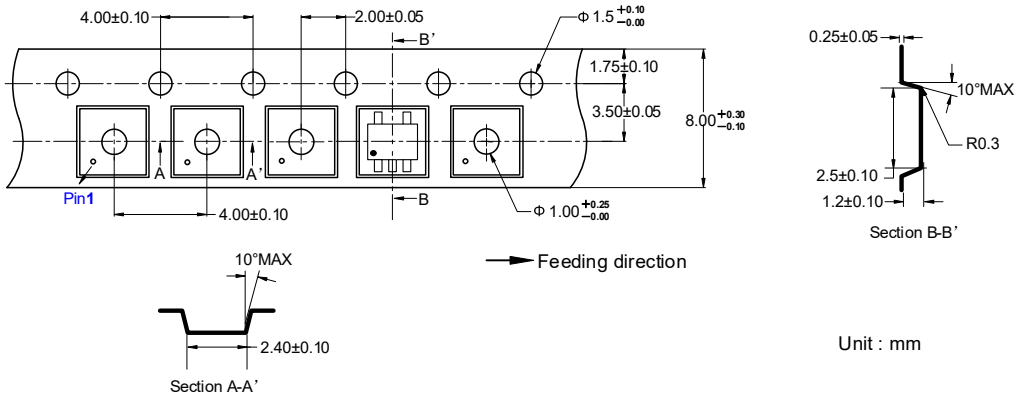
COMMON DIMENSIONS

(Unit: mm)

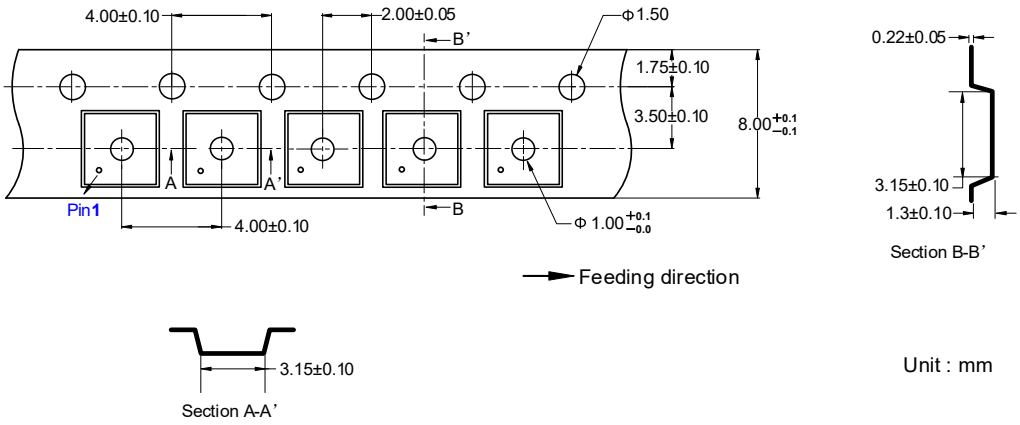
SYMBOL	MIN	NOM	MAX
A	0.50	--	0.60
A1	0.00	0.02	0.05
A3		0.10REF	
b	0.15	0.20	0.25
D	0.90	1.00	1.10
E	1.40	1.50	1.60
e		0.50BSC	
K		0.30REF	
K1		0.25REF	
L	0.35	0.40	0.45
L1	0.30	0.35	0.40

Tape Information

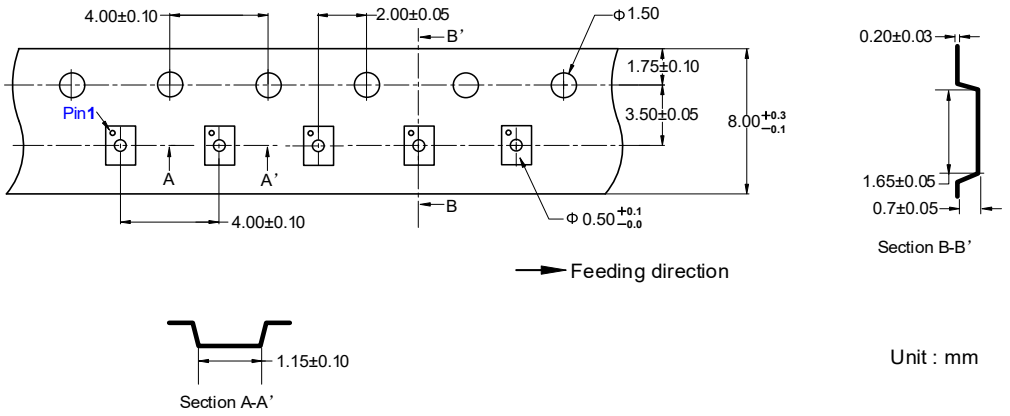
SC70-5 (1.3mm × 2.1mm)



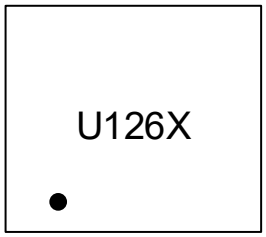
SOT23-5 (1.6mm × 2.9mm)



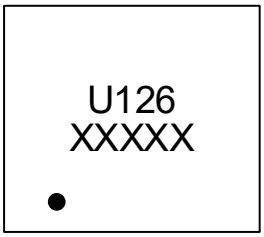
DFN6 (1.0mm × 1.5mm)



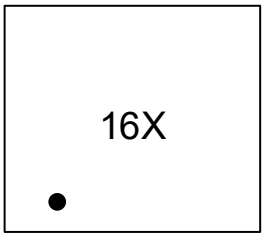
Marking Information



ET74AHC1G126
A126 = Part Number
X = Tracking Number



ET74AHC1G126T
A126 = Part Number
XXXXX = Tracking Number



ET74AHC1G126Y
16X = Part Number
X = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2023-6-22	Initial Version	Shi bo	Lu hao	Liu jiaying
1.1	2023-11-29	Update Typeset /ESD/Package Picture	Shi bo	Shi bo	Liu jiaying
1.2	2025-06-03	Add Packing Option	Yang xiaoxu	Yang xiaoxu	Liu jiaying
1.2.a	2026-03-10	Update Format, Add Tape and Marking	Xu tao	Yang xiaoxu	Liu jiaying
1.2.b	2026-03-20	Update Title	Xu tao	Yang xiaoxu	Liu jiaying
1.2.c	2026-04-22	Correct Words	Xu tao	Yang xiaoxu	Liu jiaying
1.2.d	2026-09-09	Correct Words	Xu tao	Yang xiaoxu	Liu jiaying