Dual Bidirectional I2C Bus and SMBus Voltage-Level Trasnslator

General Description

The ET9306 device is a dual bidirectional I2C and SMBus voltage-level translator with an enable (EN) input, and is operational from 0.95V to 3.3V V_{REF1} and 1.8V to 5.0V V_{REF2}. The NCA9306 device allows bidirectional voltage translations between 0.95V and 5V, without the use of a direction pin. The low ON-state resistance (R_{ON}) of the switch allows connections to be made with minimal propagation delay. When EN is high, the translator switch is ON, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, respectively, allowing bidirectional data flow between ports. When EN is low, the translator switch is off, and a high-impedance state exists between ports.

Features

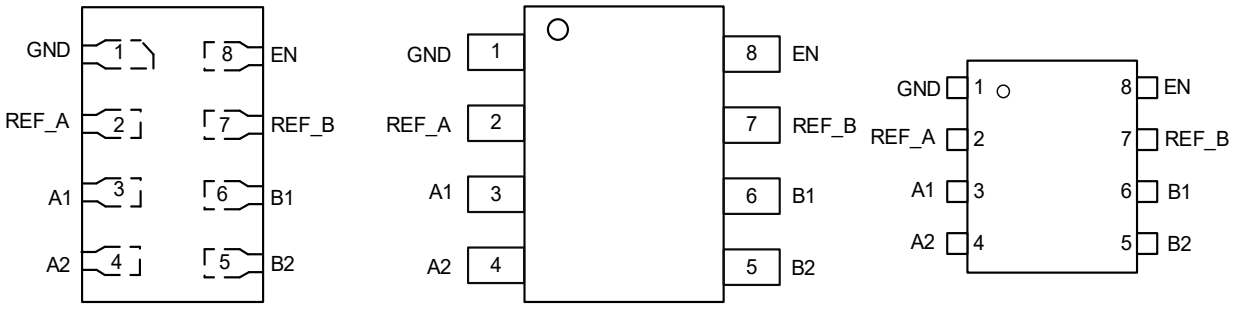
- 2 Bit bidirectional translator for SDA and SCL lines in mixed-mode I2C Applications
- I2C and SMBus Compatible
- Allows Voltage-level Translation Between
  - -- 0.95V V_{REF1} and 1.8V, 2.5V, 3.3V, or 5V V_{REF2}
  - -- 1.8V V_{REF1} and 2.5V, 3.3V, or 5V V_{REF2}
  - -- 2.5V V_{REF1} and 3.3V or 5V V_{REF2}
  - -- 3.3V V_{REF1} and 5V V_{REF2}
- Provides Bidirectional Voltage Translation with no Direction Pin
- Open-drain I2C I/O ports (SCL1, SDA1, SCL2, and SDA2)
- 5V Tolerant I2C I/O Ports to Support Mixed-mode Signal Operation
- High-impedance SCL1, SDA1, SCL2, and SDA2 pins for EN = Low
- I^3C compatible (12.5MHz Supported)
- ESD Protection Complies with JESD22 Standard
  - -- HBM: ±2000V Pass (JEDEC JS-001)
  - -- CDM: ±1000V Pass (JEDEC JS-002)
- Latch-up Performance Exceeds ±100mA per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	MSL	Packing Option
ET9306Y	DFN8 (1.4mm × 1mm)	1	Tape and Reel, 5K/Reel
ET9306M	SOP8 (3.9mm × 4.9mm)	3	Tape and Reel, 4K/Reel
ET9306U	VSSOP8 (2.0mm × 2.3mm)	3	Tape and Reel, 3K/Reel
ET9306U1	MSOP8 (3.0mm × 3.0mm)	3	Tape and Reel, 4K/Reel

Applications

- I^2C, I^3C, MDIO, UART, SDIO, GPIO, and Other Two-signal Interfaces
- Enterprise Systems
- Communications Equipment
- Personal Computers
- Industrial Automation

Pin Configuration



Top View

Figure 1. Pin Configuration

Pin Function

Pin No. DFN8/SOP8/VSSOP8/MSOP8	Pin Name	Pin Function
1	GND	Ground Pin.
2	REF_A	Reference Supply Voltage.
3,4	An	Auto-Bidirectional Data Port.
5,6	Bn	Auto-Bidirectional Data Port.
7	REF_B	Reference Supply Voltage.
8	EN	Enable Input. Connect to REF_B and pull-up through a high resistor(200kΩ).

Block Diagram

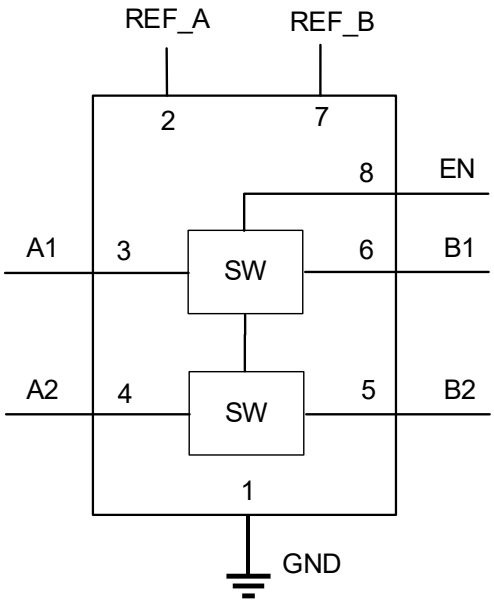


Figure 2. Block Diagram

Functional Description

The ET9306 can be used in level-translation applications for interfacing devices or systems operating with one another that operate at different interface voltages. The ET9306 is ideal for use in applications where an open-drain driver is connected to the data I/Os. The ET9306 can also be used in applications where a push-pull driver is connected to the data I/Os.

Auto Bidirectional Voltage Translation

The device is an auto bidirectional voltage level translator that is operational from 0.95 to 5.5V on REF_A and 1.8 to 5.5V on REF_B. This allows bidirectional voltage translation between 0.95V and 5.5V without the need for a direction pin in open-drain or push-pull applications. Both the output driver of the controller and the peripheral device output can be push-pull or open-drain (pull-up resistors may be required). In both up and down translation, the B-side is often referred to as the high side and refers to devices connected to the B ports. The A-side can be referred to as the low side.

Output Enable

To enable the I/O pins, the EN input should be tied directly to REF_B during operation and both pins must be pulled up to the HIGH side (V_{CCB}) through a bias resistor (typically 200kΩ). To be in the high impedance state during power-up, power-down, or during operation, the EN pin must be LOW. The EN pin should always be tied directly to the REF_B pin and is recommended to be disabled by an open-drain driver without a pull-up resistor. This allows REF_B to regulate the EN input and bias the channels for proper translation. A filter capacitor on REF_B is recommended for a stable supply at the device.

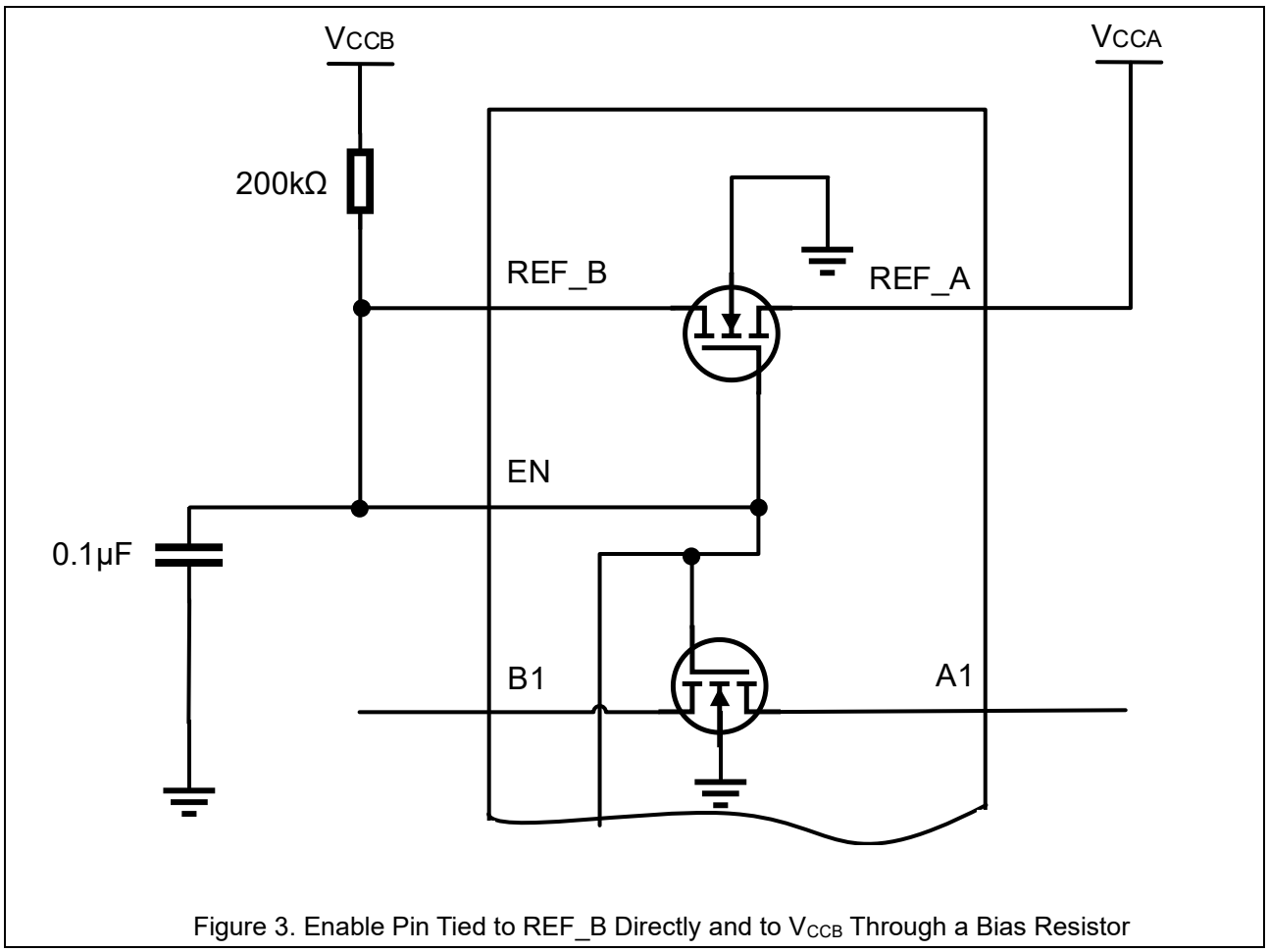


Figure 3. Enable Pin Tied to REF_B Directly and to V_{CCB} Through a Bias Resistor

The supply voltage of open drain I/O devices can be completely different from the supplies used for the ET9306 and has no impact on the operation.

Table 1. Enable Pin Function Table (EN is controlled by V_{CCB} logic levels.)

EN PIN	Data Port State
Tied directly to REF_B	An = Bn
L	Hi-Z

Device Functional Modes

For each channel (n), when either the An or Bn port is LOW, the switch provides a low impedance path between the An and Bn ports; the corresponding Bn or An port will be pulled LOW. The low R_{ON} of the switch allows connections to be made with minimal propagation delay and signal distortion. Table 2. provides a summary of device operation.

Table 2. Device Functionality

Signal Direction[1]	Input State	Switch State	Functionality
B to A (Down Translation)	B = LOW	ON (Low Impedance)	A-side voltage is pulled low through the switch to the B-side voltage
	B = HIGH	OFF (High Impedance)	A-side voltage is clamped at V_{REF_A} [2]
A to B (Up Translation)	A = LOW	ON (Low Impedance)	B-side voltage is pulled low through the switch to the A-side voltage
	A = HIGH	OFF (High Impedance)	B-side voltage is clamped at V_{REF_A} and then pulled up to the V_{PU} supply voltage

Note1: The downstream channel should not be actively driven through a low impedance driver, or else bus contention may occur.

Note2: The A-side can have a pull up to V_{REF_A} for additional current drive capability or may also be pulled above V_{REF_A} with a pull up resistor. Specifications in the Recommended Operating Conditions section should always be followed.

Up Translation

When the signal is being driven from A to B and the An port is HIGH, the switch will be OFF and the Bn port will then be driven to a voltage higher than V_{REF_A} by the pull-up resistor that is connected to the pull-up supply voltage (V_{PU}). This functionality allows seamless translation between higher and lower voltages selected by the user, without the need for directional control. Pull-up resistors are always required on the high side, and pull-ups are only required on the low side, if the low side of the device's output is open drain or its input has a leakage greater than 1μA.

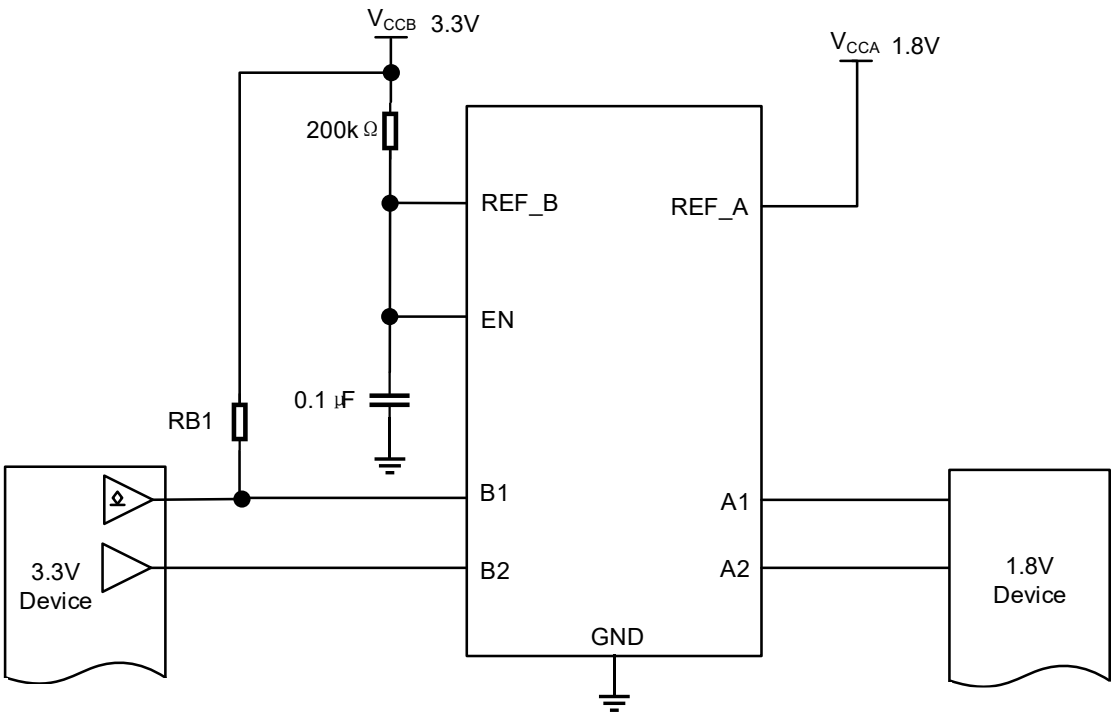


Figure 4. Up Translation Example Schematic with Push-Pull and Open Drain Configuration

Up translation with the ET9306 requires attention to two important factors: maximum data rate and sink current. Maximum data rate is directly related to the rising edge of the output signal. Sink current depends on supply values and the chosen pull-up resistor values. Equation 1 shows the maximum data rate formula and Equation 2 shows the maximum sink current formula, both of which are estimations. A low RC value is needed to reach high speeds, which also require strong drivers.

$$\frac{1}{3\times 2R_{B1}C_{B1}} \equiv \frac{1}{6R_{B1}C_{B1}}\left(\frac{\text{bits}}{second}\right) \quad (1)$$

$$I_{OL} \cong \frac{VCCA}{R_{A1}} + \frac{VCCB}{R_{B1}}(A) \quad (2)$$

Down Translation

When the signal is being driven HIGH from the Bn port to An port, the switch will be OFF, clamping the voltage on the An port to the voltage set by V_{REF_A}. A pull-up resistor can be added on either side of the device. There are special circumstances that allow the removal of one or both of the pull-up resistors. If the signal is always going to be down translated from a push-pull transmitter, then the resistor on the B-side can be removed. If the leakage current into the receiver on the A-side is less than 1μA, then the resistor on the A-side can also be removed. This arrangement with no external pull-up resistors can be used when down translating from a push-pull output to a low-leakage input. For an open drain transmitter, the pull-up resistor on the B-side is necessary because an open drain output can't drive high by itself.

Absolute Maximum Ratings

Symbol	Parameters (Items)	Value	Unit
V_I	Input Voltage (REF_A, REF_B, OE)	-0.3 to 6.0	V
$V_{I/O}$	Input/output Voltage	-0.3 to 6.0	V
I_O	Continuous Channel Current	0 to 128	mA
I_{IK}	Input Clamp Current	-50	mA
T_{STG}	Storage Temperature Range	-65 to +150	ºC
T_J	Operating Junction Temperature	-40 to +150	ºC
$R_{\theta JA}$	Junction-to-ambient Thermal Resistance	250	°C/W
V_{ESD}	Human Body Model (JEDEC JS-001)	±2000	V
	Charged Device Model (JEDEC JS-002)	±1000	V
I_{LU}	Latch Up Current (JEDEC JESD78F)	±100	mA

Recommended Operating Conditions

Symbol	Parameters	Rating	Unit
$V_{I/O}$	Input/Output Voltage	0 to 5.5	V
V_{CCB}	V_{REF_B} Supply Voltage	0 to 5.5	V
V_{REF_A} (V_{CCA})	Reference Voltage	0 to 5.5	V
V_{EN}	EN Pin Voltage	0 to 5.5	V
I_{PASS}	Pass Transistor Current	64	mA
T_A	Operating Ambient Temperature	-40 to +85	ºC

Electrical Characteristics

T_A=-40ºC~85ºC, from A to B or B to A (unless otherwise noted, all typical values are at T_A = 25°C.)

Symbol	Parameters	Conditions		Min	Typ	Max	Unit
V_{IK}	I/O Input Clamp Voltage	I_I = -18mA, V_{EN} = 0V				-1.2	V
I_{IH}	Input Leakage Current	V_I = 5V, V_{EN} = 0V				5.0	uA
I_{CC}	Input Current	V_{CCB} = V_{EN} = 5.5V, V_{CCA} = 4.5V, I_O = 0mA, V_I = V_{CC} or GND			0.1	1	uA
$C_{I(REF_A/B/EN)}$ (3)	Input Capacitance	V_I = 3V or 0V， T_A = 25°C.			11		pF
$C_{IO(off)}$ (3)	Off Capacitance	V_I = 3V or 0V, V_{EN} = 0V, T_A = 25°C.			4.0	6.0	pF
$C_{IO(on)}$ (3)	On Capacitance	V_I = 3V or 0V, V_{EN} = 3V, T_A = 25°C.			12	17	pF
R_{ON}(4)	On-state Resistance	V_I = 0V, I_O=64mA	V_{CCA} = 3.3V; V_{CCB}=V_{EN}=5V		3.0	7.0	Ω
			V_{CCA} = 1.8V; V_{CCB} = V_{EN} = 5V		4.0	10	
			V_{CCA} = 1.0V; V_{CCB} =V_{EN} = 5V		5.0	25	
		V_I = 0V, I_O=32mA	V_{REF_A}= 1.8V; V_{CCB} = V_{EN} =5V		4.0	9.0	
			V_{CCA}= 2.5V; V_{CCB} = V_{EN}= 5V		3.0	8.0	
		V_I = 1.8V, I_O=15mA	V_{CCA} = 3.3V; V_{CCB} = V_{EN} = 5V		4.0	13	
		V_I = 1.0V, I_O=10mA	V_{CCA} = 1.8V; V_{CCB} = V_{EN} =3.3V		7.0	24	
		V_I = 0V, I_O=10mA	V_{CCA} = 1.0V; V_{CCB} = V_{EN} = 3.3V		5.0	18	
		V_I = 0V, I_O=10mA	V_{CCA} = 1.0V; V_{CCB} = V_{EN} = 1.8V		6.0	19	

Note3: Guaranteed by design and characterization, not a FT item.

Note4: Measured by the voltage drop between the A and B pins at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) pins.

AC Performance (Translating Down) Switching Characteristics

T_A=-40ºC~85ºC, from B to A, R_L=1KΩ (unless otherwise noted, all typical values are at T_A = 25°C.)

Symbol	Parameters	Conditions		Min	Typ	Max	Unit
t_{PLH}	Low-to-High Propagation Delay	V_{CCB} = V_{IH} =1.8V, V_{CCA} = 0.95V, V_{IL} = 0V, and V_M = 0.5 V_{CCA}	C_L = 20pF		0.6	1.5	ns
			C_L = 30pF		0.8	2.0	
			C_L = 50pF		1.0	2.5	
		V_{CCB} = V_{IH} =1.8V, V_{CCA} = 1.2V, V_{IL} = 0V, and V_M = 0.5 V_{CCA}	C_L = 20pF		0.8	1.5	
			C_L = 30pF		1.4	2.5	
			C_L = 50pF		3.0	4.0	
		V_{CCB} = V_{IH} =3.3V, V_{CCA} = 1.8V, V_{IL} = 0V, and V_M = 0.5 V_{CCA}	C_L = 20pF		0.3	1.2	
			C_L = 30pF		0.5	2.0	
			C_L = 50pF		0.9	2.5	
		V_{CCB} = V_{IH} =5V, V_{CCA} = 3.3V, V_{IL} = 0V, and V_M = 0.5 V_{CCA}	C_L = 20pF		0.8	1.2	
			C_L = 30pF		1.0	1.5	
			C_L = 50pF		1.2	2.0	
t_{PHL}	High-to-Low Propagation Delay	V_{CCB} = V_{IH} =1.8V, V_{CCA} = 0.95V, V_{IL} = 0V, and V_M = 0.5 V_{CCA}	C_L = 20pF		0.4	2.5	
			C_L = 30pF		1.0	3.0	
			C_L = 50pF		2.0	4.0	
		V_{CCB} = V_{IH} =1.8V, V_{CCA} = 1.2V, V_{IL} = 0V, and V_M = 0.5 V_{CCA}	C_L = 20pF		0.7	2.0	
			C_L = 30pF		1.3	3.0	
			C_L = 50pF		2.0	4.0	
		V_{CCB} = V_{IH} =3.3V, V_{CCA} = 1.8V, V_{IL} = 0V, and V_M = 0.5 V_{CCA}	C_L = 20pF		0.4	2.0	
			C_L = 30pF		0.9	2.5	
			C_L = 50pF		1.5	3.0	
		V_{CCB} = V_{IH} =5V, V_{CCA} = 3.3V, V_{IL} = 0V, and V_M = 0.5 V_{CCA}	C_L = 20pF		0.4	1.5	
			C_L = 30pF		1.0	2.5	
			C_L = 50pF		1.4	3.0	

AC Performance (Translating Up) Switching Characteristics

T_A=-40ºC~85ºC, from A to B, R_L=1KΩ (unless otherwise noted, all typical values are at T_A = 25°C.)

Symbol	Parameters	Conditions		Min	Typ	Max	Unit
t_{PLH}	Low-to-High Propagation Delay	V_{CCB} =1.8V, V_{CCA} = V_{IH} = 0.95V, V_{IL} = 0V, and V_M = 0.5 V_{CCA}	C_L = 20pF		0.8	1.5	ns
			C_L = 30pF		1.0	2.0	
			C_L = 50pF		1.2	3.0	
		V_{CCB} = 1.8V, V_{CCA} = V_{IH} = 1.2V, V_{IL} = 0V, and V_M = 0.5 V_{CCA}	C_L = 20pF		1.1	1.5	
			C_L = 30pF		1.3	2.0	
			C_L = 50pF		1.9	3.0	
		V_{CCB} = 3.3V, V_{CCA} = V_{IH} = 1.8V, V_{IL} = 0V, and V_M = 0.5 V_{CCA}	C_L = 20pF		0.6	1.0	
			C_L = 30pF		0.8	1.5	
			C_L = 50pF		1.0	2.0	
		V_{CCB} = 5V, V_{CCA} = V_{IH} = 3.3V, V_{IL} = 0V, and V_M = 0.5 V_{CCA}	C_L = 20pF		0.6	1.5	
			C_L = 30pF		0.8	2.5	
			C_L = 50pF		1.2	3.0	
t_{PHL}	High-to-Low Propagation Delay	V_{CCB} =1.8V, V_{CCA} = V_{IH} = 0.95V, V_{IL} = 0V, and V_M = 0.5 V_{CCA}	C_L = 20pF		2.0	3.5	
			C_L = 30pF		2.8	4.5	
			C_L = 50pF		4.2	6.5	
		V_{CCB} = 1.8V, V_{CCA} = V_{IH} = 1.2V, V_{IL} = 0V, and V_M = 0.5 V_{CCA}	C_L = 20pF		1.7	3.0	
			C_L = 30pF		2.6	3.5	
			C_L = 50pF		4.2	4.5	
		V_{CCB} = 3.3V, V_{CCA} = V_{IH} = 1.8V, V_{IL} = 0V, and V_M = 0.5 V_{CCA}	C_L = 20pF		1.2	3.0	
			C_L = 30pF		1.8	4.0	
			C_L = 50pF		2.6	5.0	
		V_{CCB} = 5V, V_{CCA} = V_{IH} = 3.3V, V_{IL} = 0V, and V_M = 0.5 V_{CCA}	C_L = 20pF		0.8	2.0	
			C_L = 30pF		1.2	3.0	
			C_L = 50pF		1.8	4.0	

Maximum Data Rate

C_L = 20pF, R_L=1KΩ, and T_A = -40°C to 85°C.

V_{VCCA}	Condition	V_{VCCB}			Unit
		1.8V	3.3V	5V	
0.95V	Push-Pull	140	140	140	Mbps
	Open-Drain	6	6	6	
1.2V	Push-Pull	140	140	140	
	Open-Drain	6	6	6	
1.8V	Push-Pull	140	140	140	
	Open-Drain	6	6	6	
3.3V	Push-Pull	-	140	140	
	Open-Drain	-	6	6	

AC Performance Test Circuit

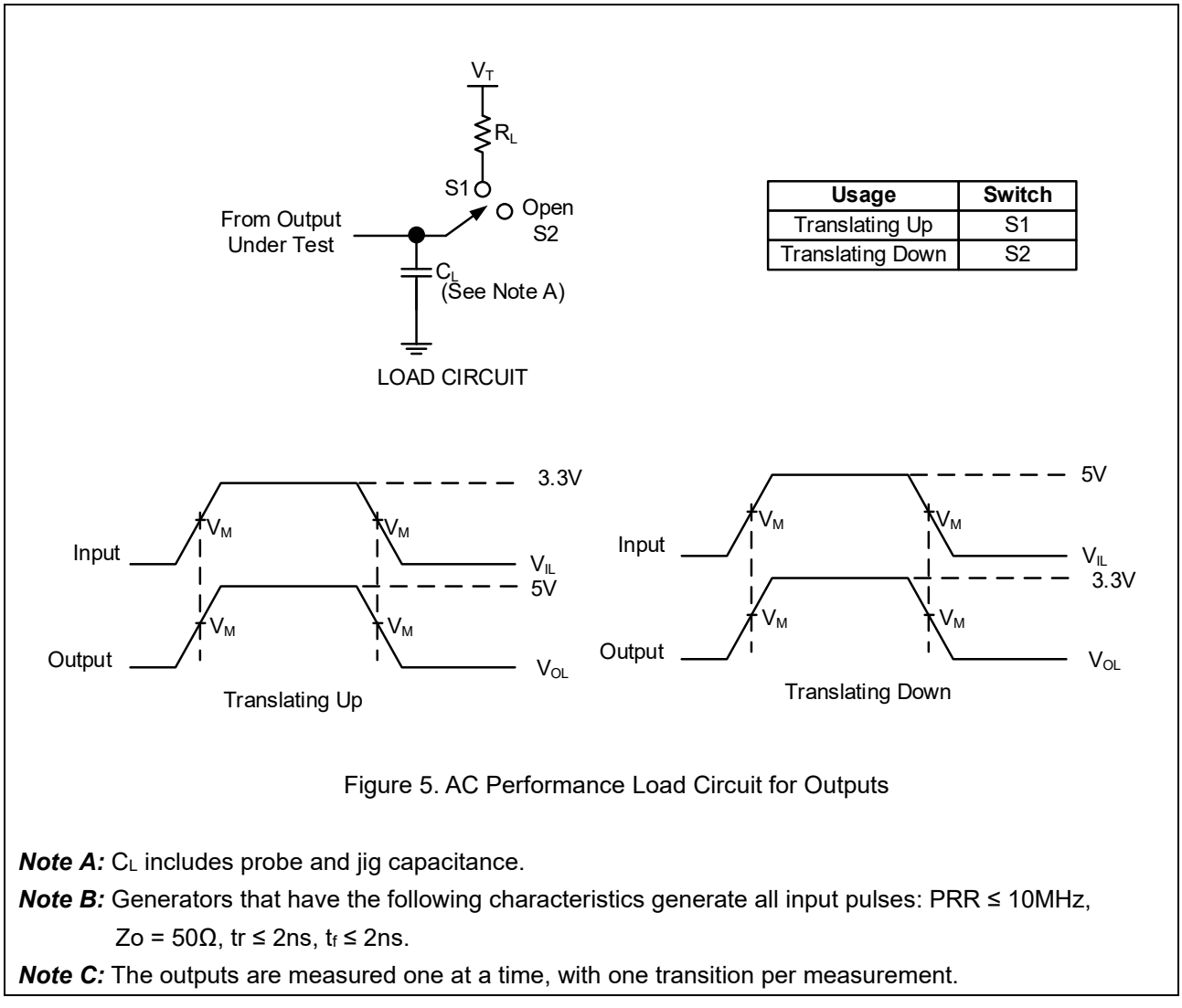


Figure 5. AC Performance Load Circuit for Outputs

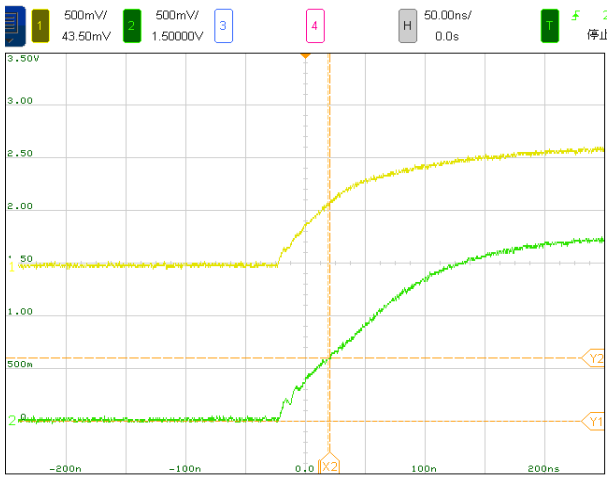
Note A: C_L includes probe and jig capacitance.

Note B: Generators that have the following characteristics generate all input pulses: PRR ≤ 10MHz, Zo = 50Ω, tr ≤ 2ns, t_f ≤ 2ns.

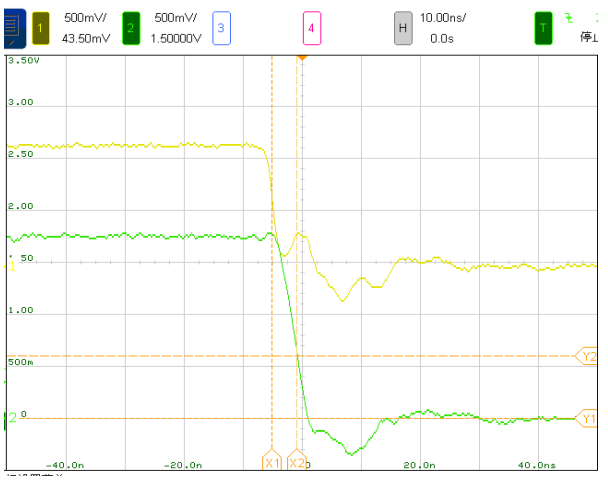
Note C: The outputs are measured one at a time, with one transition per measurement.

Typical Characteristics

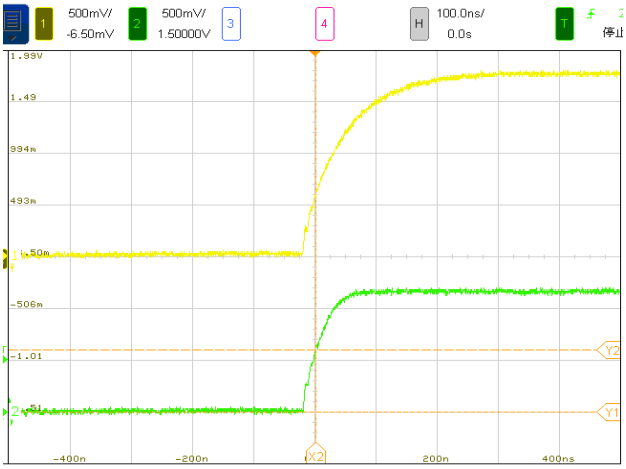
(V_{CCB}=1.8V, V_{CCA}=1.2V, C_L=50pF, R_{PU} =1KΩ，C_L = 50pF unless otherwise noted T_A=25°C.)



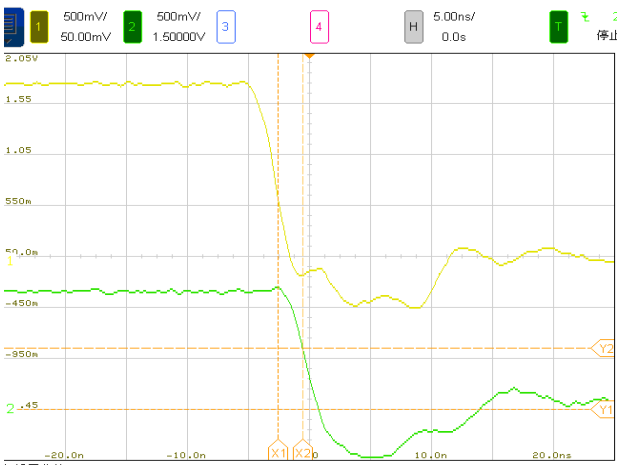
AC Performance t_{PLH} 1.2V to 1.8V



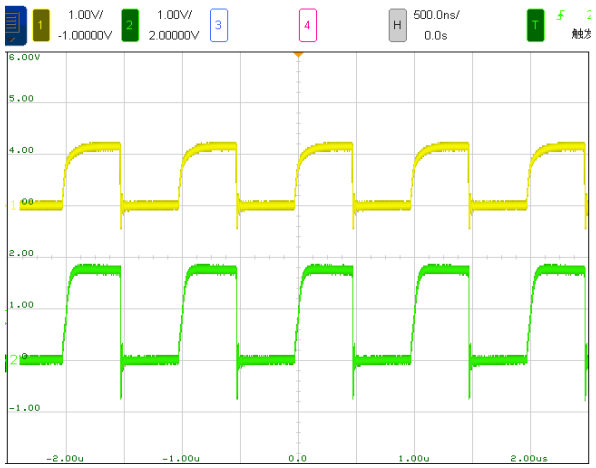
AC Performance t_{PHL} 1.2V to 1.8V



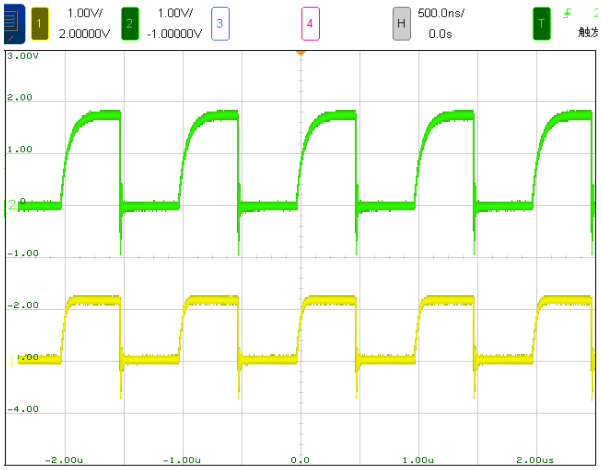
AC Performance t_{PLH} 1.8V to 1.2V



AC Performance t_{PHL} 1.8V to 1.2V



Voltage Translation, 1.2V to 1.8V, f=1MHz



Voltage Translation, 1.8V to 1.2V, f=1MHz

Application Circuits

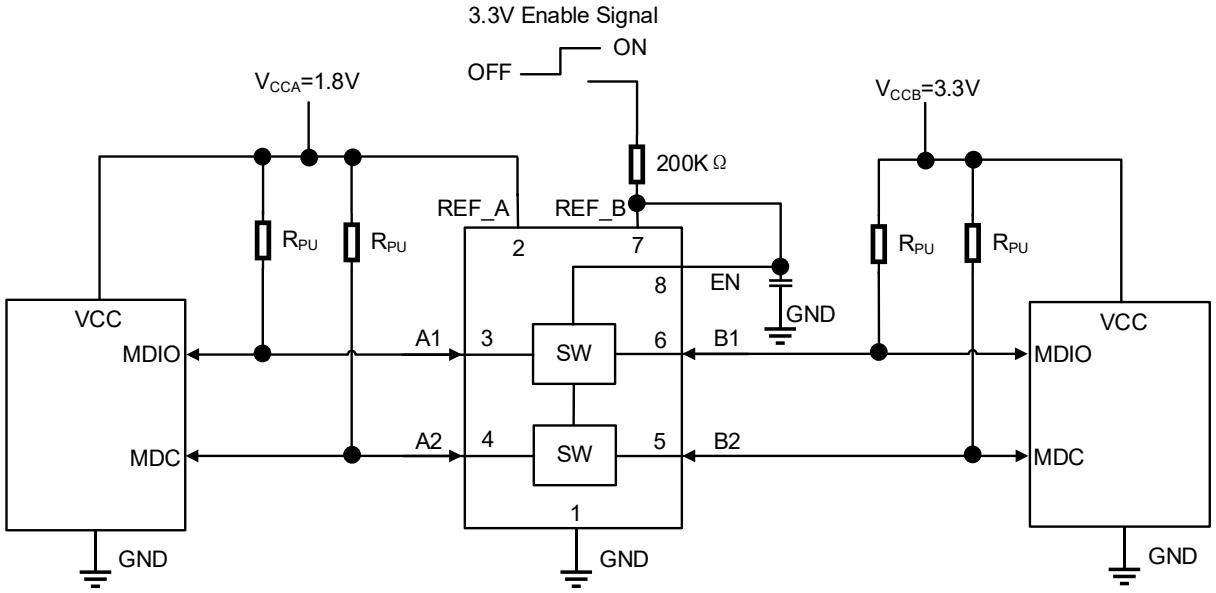
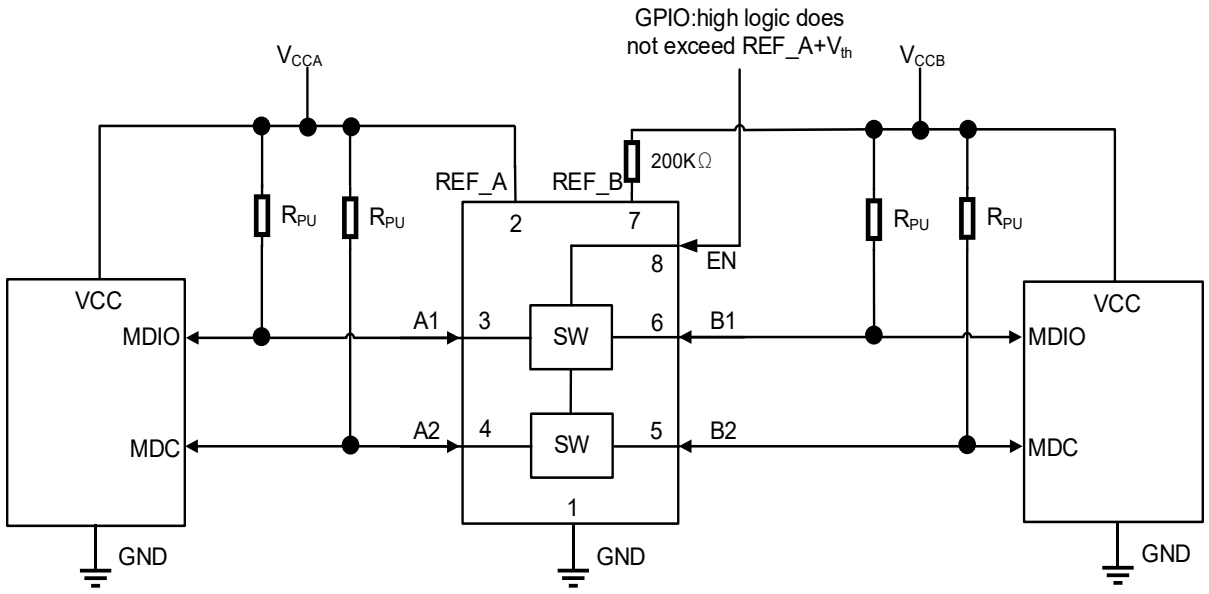


Figure 6. Typical Application Circuit for Open-Drain Translation (MDIO Shown as an Example)



V_{th} is approximately 0.7V

Figure 7. Special Application Circuit for EN Configured through GPIO Ports (MDIO Shown as an Example)

In the Figure 6, V_{CCB} is connected through a 200kΩ resistor to a 3.3V power supply and V_{REF_A} is set to 1.8V. The A1 and A2 channels have a maximum output voltage equal to V_{REF_A} and the B1 and B2 channels have has a maximum output voltage equal to V_{PU}.

The ET9306 has an EN input that is used to disable the device by setting EN LOW, placing all I/Os in the high-impedance state. Since the ET9306 of devices are switch-type voltage translators, the power consumption is very low.

In the Figure 7, the EN pin of the ET9306 can be configured through GPIO(VCCB ≥ VCCA). However, using this connection method may degrade the propagation delay (tpd) performance.

Table 3. Application Operating Condition

Symbol	Parameters	Min	Typ	Max	Unit
$V_{CCA}(V_{REF_A})$ (5)	Reference Voltage (A)	0.9		5.5	V
V_{CCB}	V_{REF_B} Supply Voltage (B)	V_{CCA} + 0.8		5.5	V
V_{EN}	Input Voltage on EN Pin	V_{CCA} + 0.8		5.5	V
V_{PU}	Pull-up Supply Voltage	0		V_{CCB}	V

Note5: $V_{CCA}(V_{REF_A})$ is required to be the lowest voltage level across all inputs and outputs. The 200kΩ, bias resistor is required to allow V_{CCB} to regulate the EN input and properly bias the device for translation.

Systems Examples: I3C Usage Considerations

The ET9306 has bandwidth to support the high speeds needed for I3C, but there are special considerations which are required. Since I3C uses both push-pull and open-drain, it may not be possible to support all I3C applications with a FET-based translator.

I3C Bus Switching

Bus switching is when the bus path is enabled or disabled, but does not translate the bus voltage. External pull-up resistors are not needed for I3C, because the controller enables or disables the pull-up resistor on the SDA line. This presents a unique challenge for FET-based translators, like the ET9306, because they rely on a pull-up resistor to pull the output side of the switch all the way to supply. For the switching use case, there is no translation, but the enable voltage must be high enough for the switch to stay on for the entire voltage range of the bus (0V to bus voltage).

R_{ON} must be low enough for the full push-pull voltage range. The EN voltage must be at least 1 V_t (~0.6 V) above the maximum desired pass-voltage. This comes out to $V_{EN} \geq V_{BUS}$ + 0.6V. Since the switch enable voltage is being directly controlled, the V_{REFA} and V_{REFB} pins are not needed, and can be shorted to ground to improve power consumption.

It is possible to control the EN pin with a voltage equal to V_{BUS}, but external pull-up resistors on the downstream side are a requirement to ensure the bus is pulled entirely to V_{BUS}.

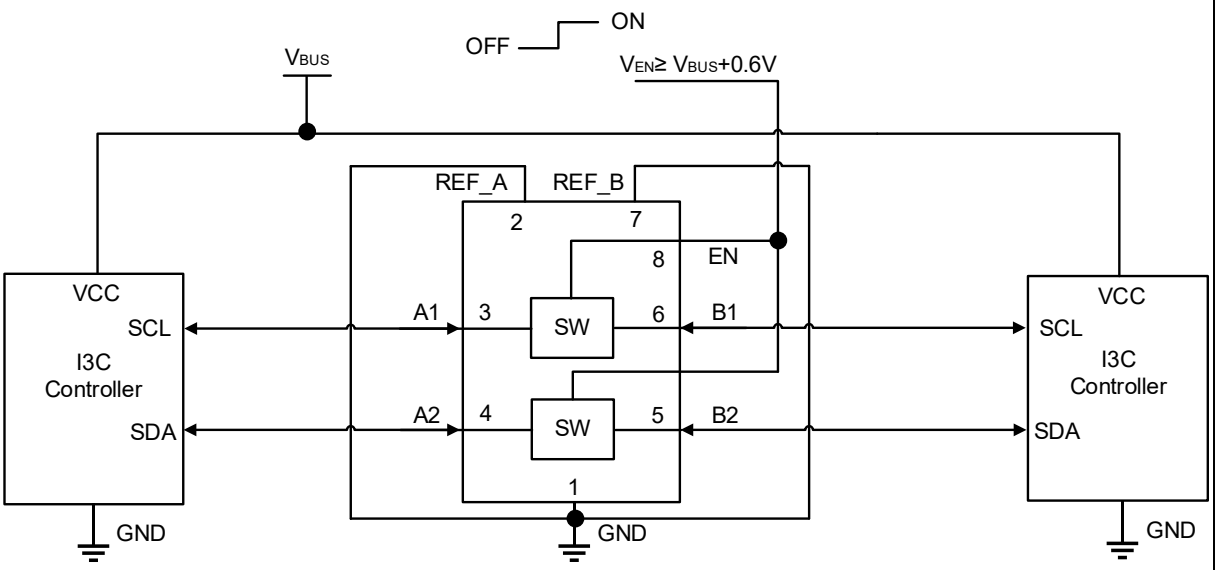


Figure 8. I3C Bus Switching Application (Without Pull-up Resistors)

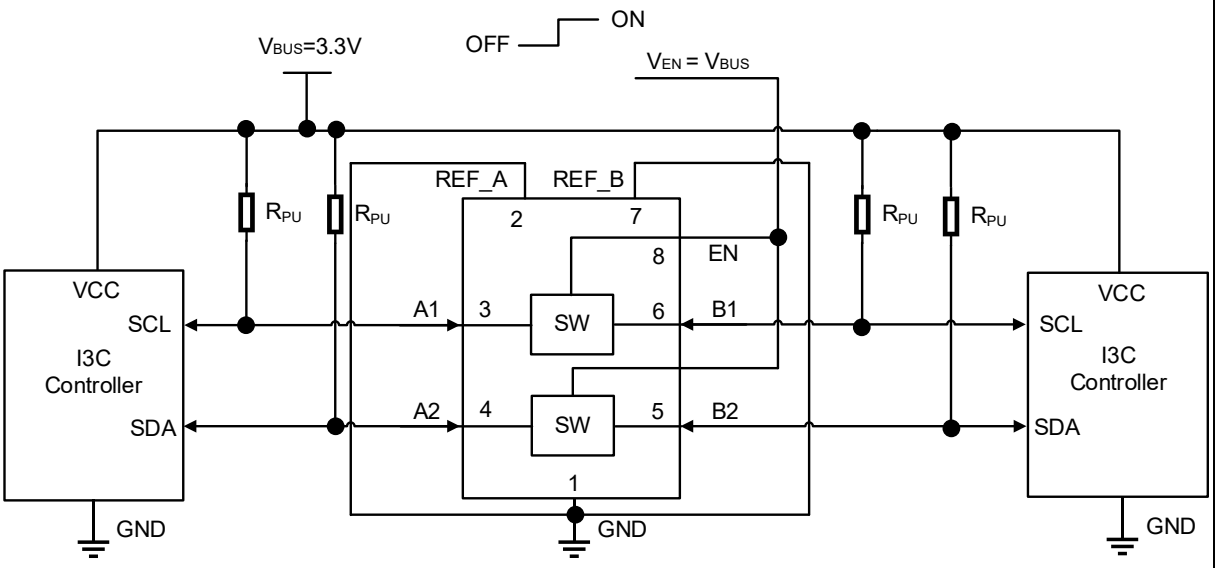


Figure 9. I3C Bus Switching Application (With Pull-up Resistors)

I3C Bus Voltage Translation

Bus voltage translation is when the bus voltage is translated up or down. This presents a unique challenge with I3C for FET-based translators, like the ET9306, because they rely on a pull-up resistor to translate the voltage up from the low-voltage side. The pull-up resistor selected must be strong enough to meet the timing requirements (based on bus capacitance and translation voltages), but not so strong to violate the V_{IL} requirements of the I3C devices.

The pull-up resistors are needed on both sides. The reason for this is that with the normal translation setup, the switch is "on" when either side's bus voltage drops to roughly V_{PU_1}. This means that the pull-up resistors are required to pull the bus voltage on the high-voltage side from V_{PU_1} to V_{PU_2}. When the device on the high-voltage side is controlling the bus, the switch will turn off at V_{PU_1}. The pull-up resistors on the low-voltage side are used to bleed off any additional current that might "leak" through the switch.

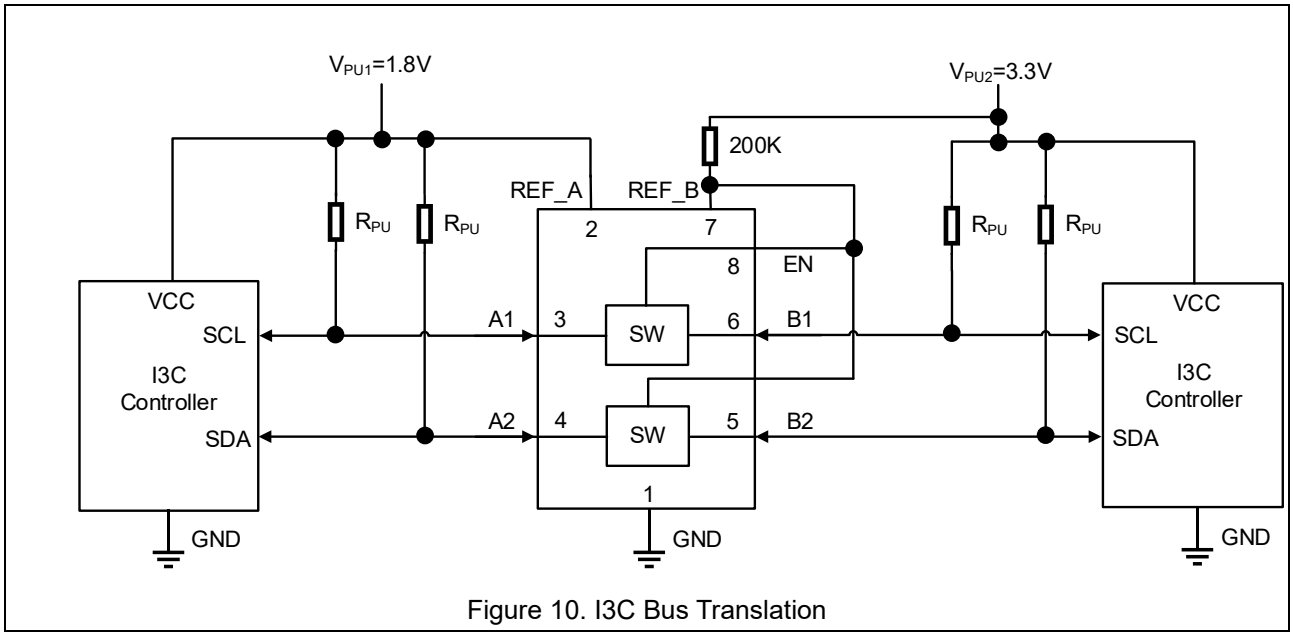
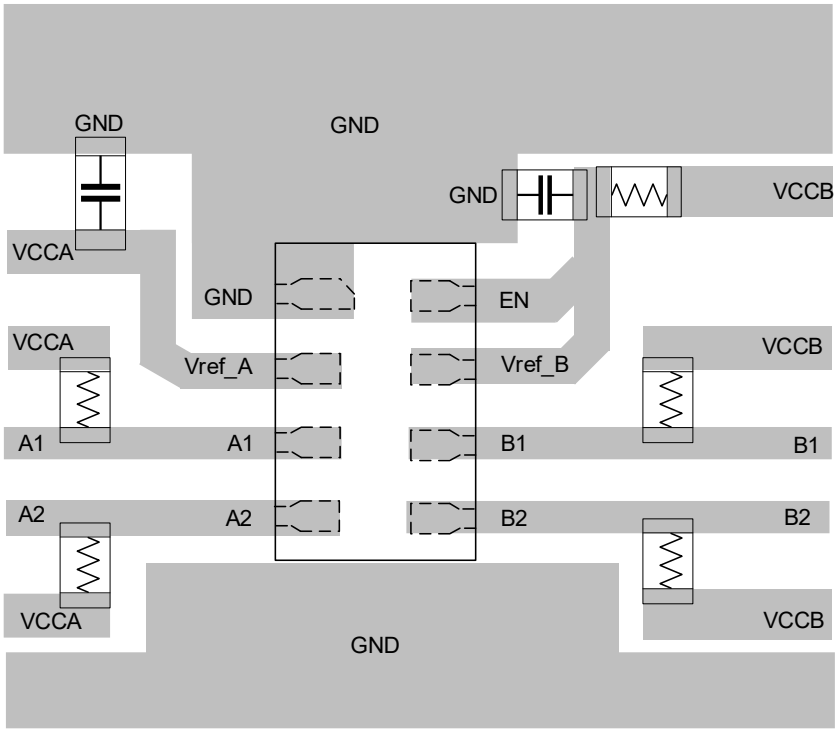
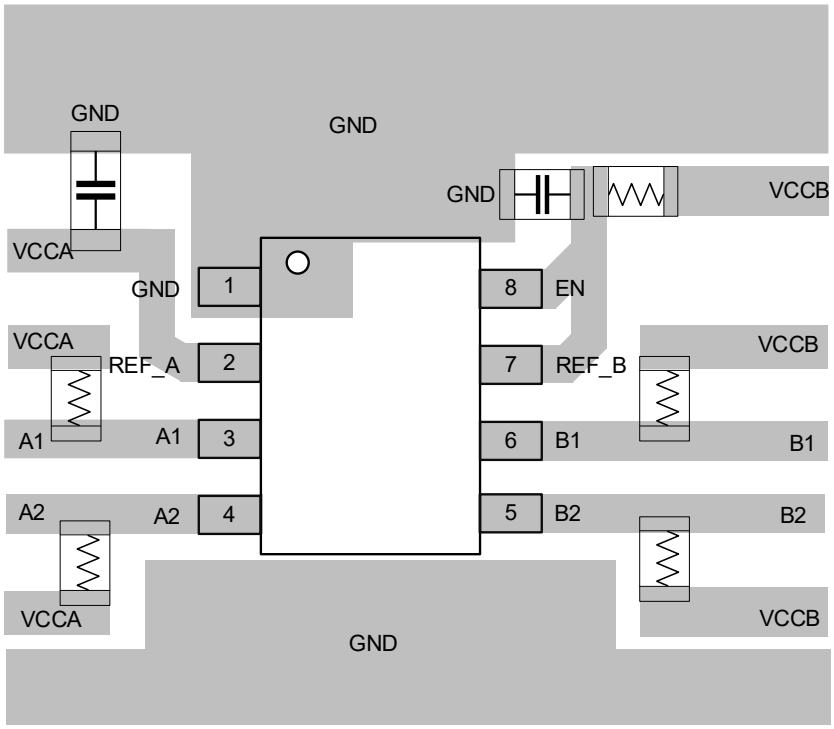


Figure 10. I3C Bus Translation

PCB Layout Guide

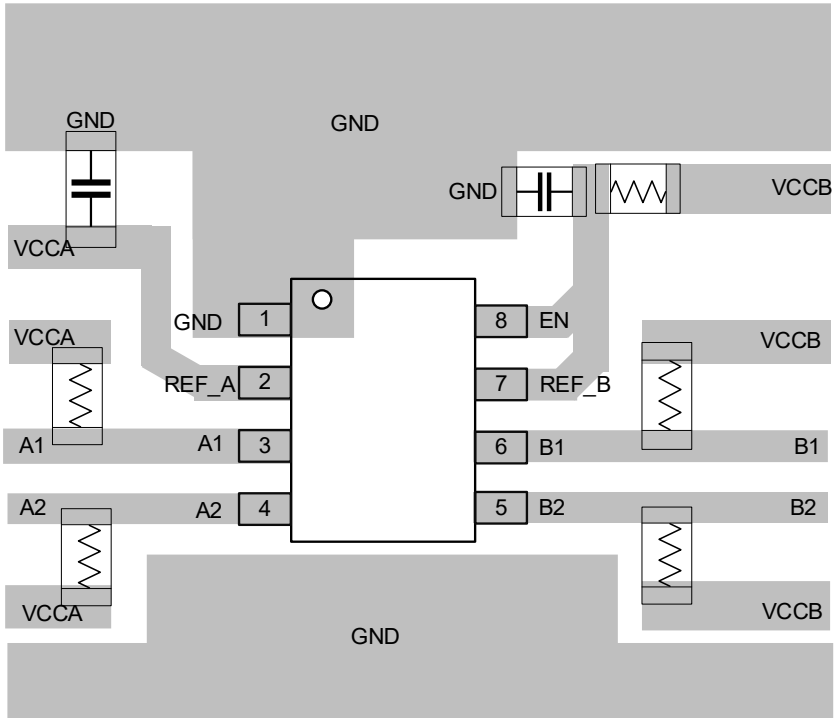


DFN8

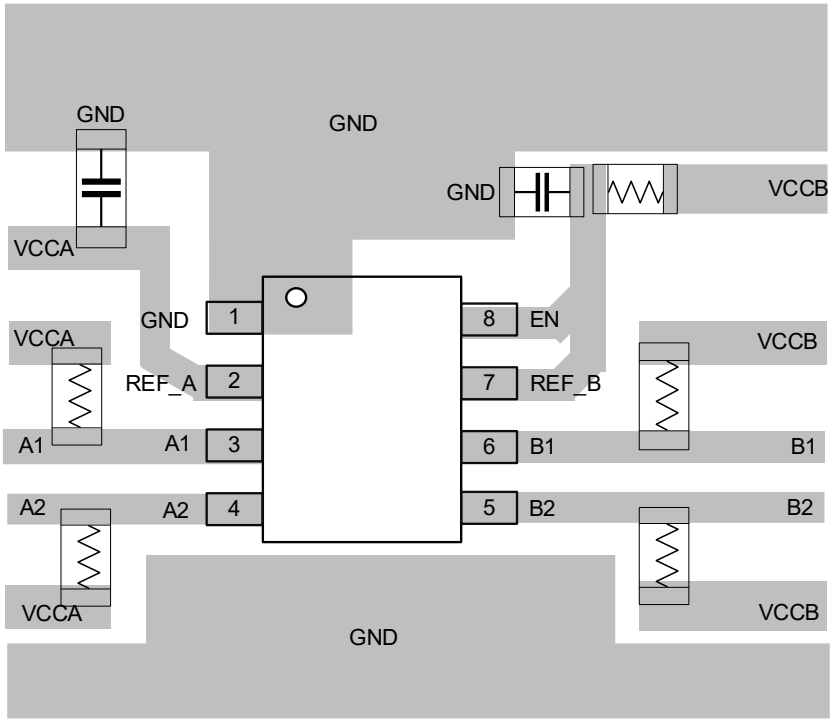


SOP8

PCB Layout Guide(Continued)



VSSOP8

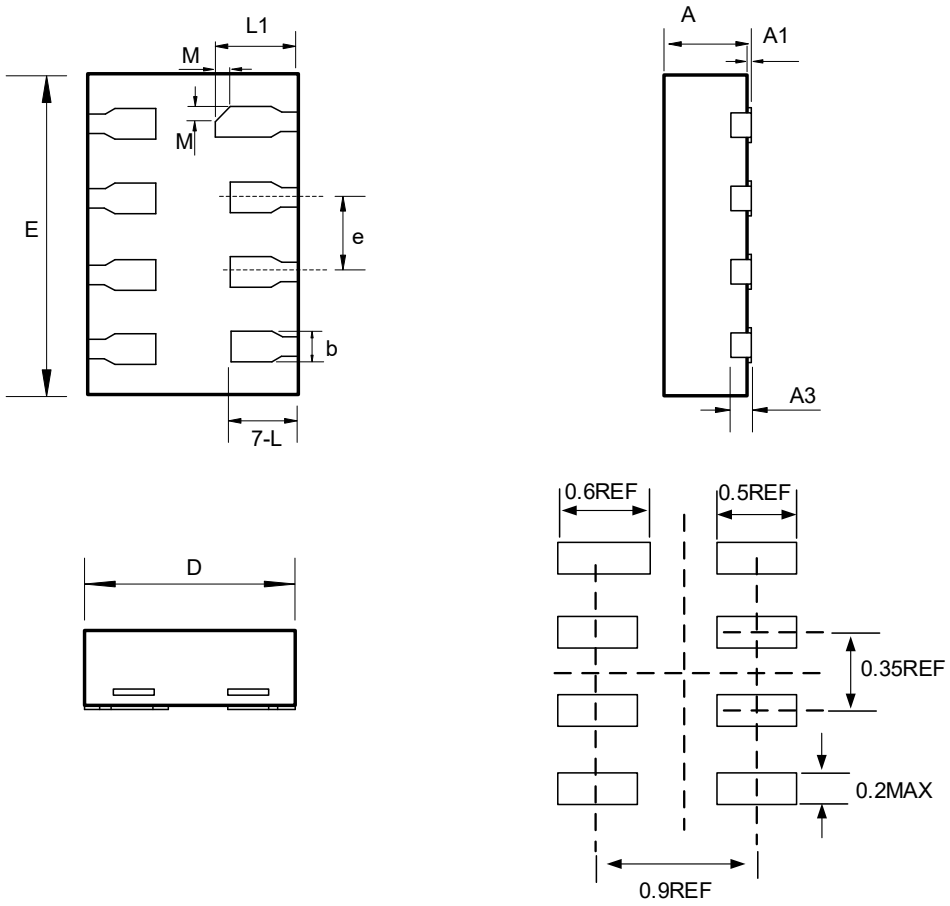


MSOP8

Figure 11. PCB Layout Guide

Package Dimension

DFN8(1.4mm × 1.0mm)

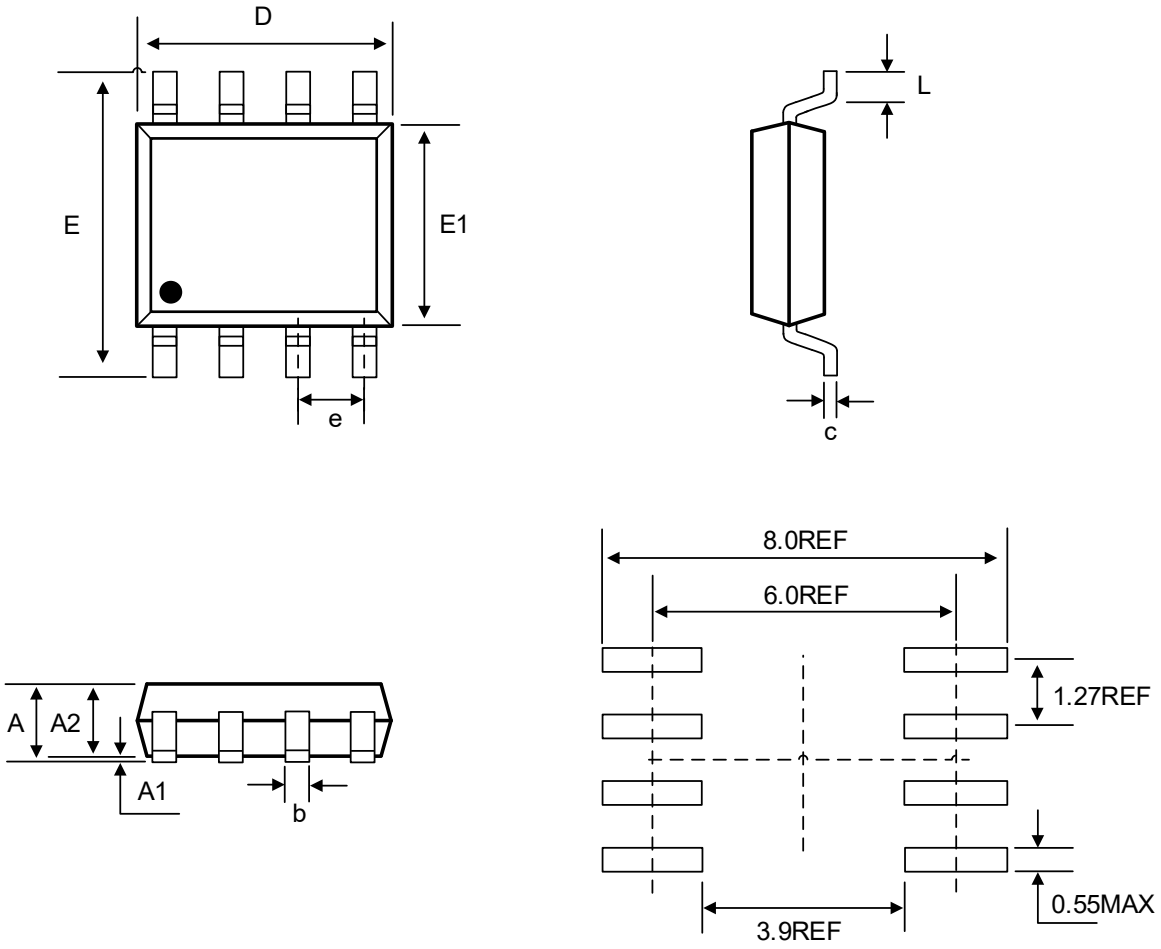


COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	0.34	0.37	0.40
A1	0.00	0.02	0.05
A3		0.10 REF	
b	0.125	0.175	0.225
D	0.90	1.00	1.10
E	1.30	1.40	1.50
e	0.30	0.35	0.40
L	0.25	0.30	0.35
L1	0.35	0.40	0.45
M		0.10 REF	

SOP8(3.9mm × 4.9mm)

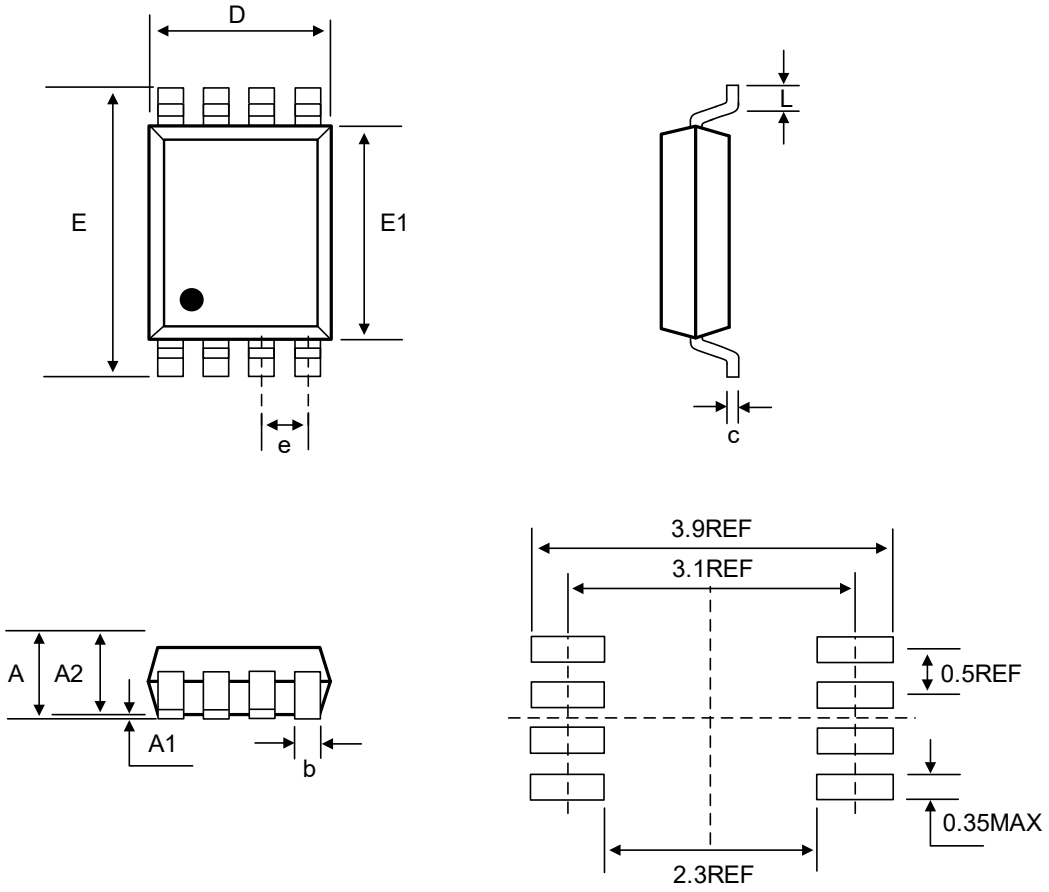


COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.90
A1	0.00	-	0.30
A2	1.20	1.40	1.60
b	0.35	-	0.47
c	0.15	-	0.27
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
L	0.35	0.60	0.85

VSSOP8 (2.3 mm × 2.0 mm)

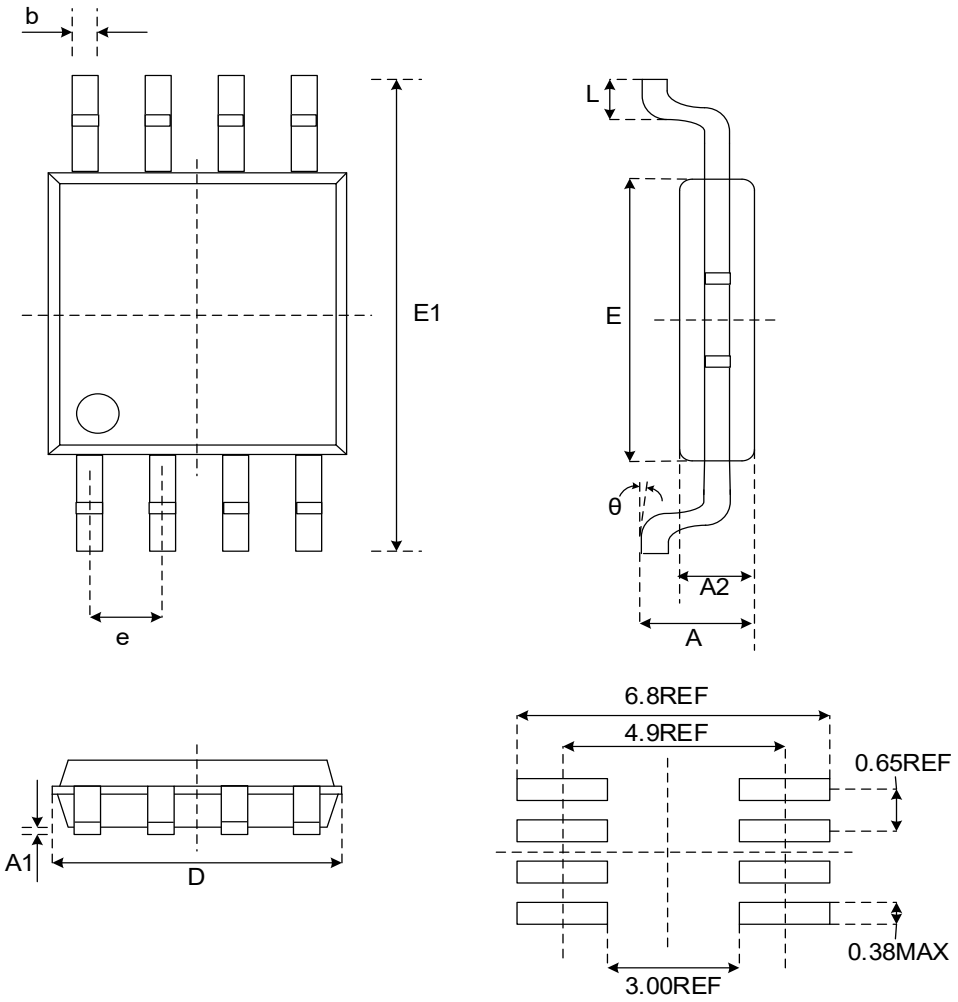


COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	0.90
A1	0.00	-	0.10
A2	0.65	0.75	0.80
b	0.17	-	0.27
c	0.08	-	0.20
D	1.90	2.00	2.10
E	3.00	3.10	3.20
E1	2.20	2.30	2.40
e	0.50 BSC		
L	0.20	-	0.35

MSOP8 (3.0 mm × 3.0 mm)



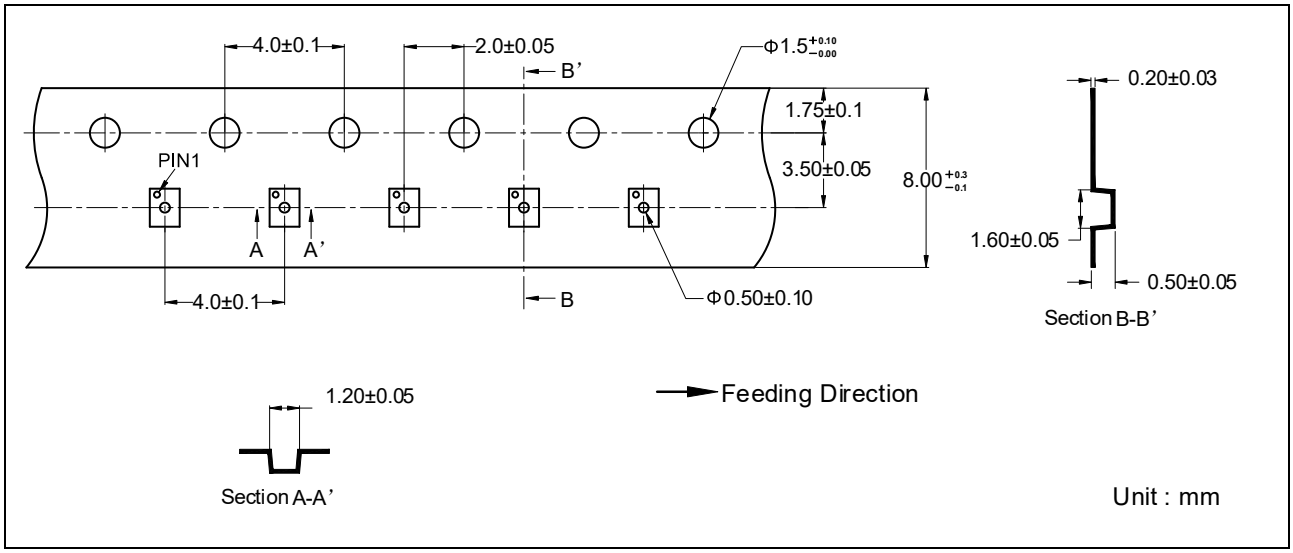
COMMON DIMENSIONS

(Unit: mm)

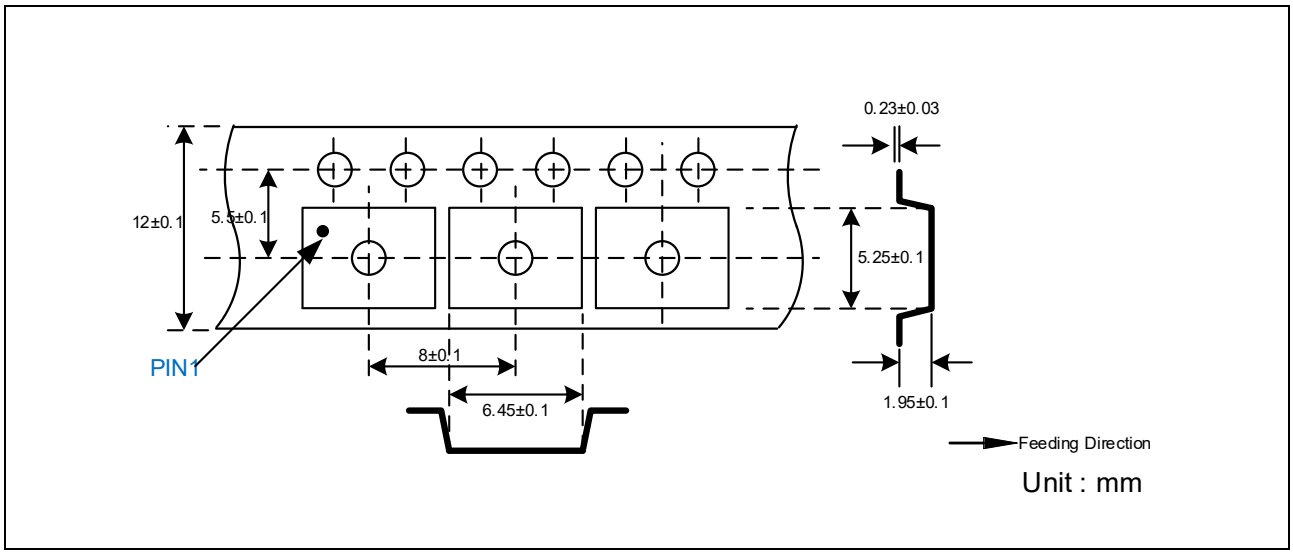
SYMBOL	MIN	NOM	MAX
A	0.82	-	1.10
A1	0.02	-	0.15
A2	0.75	-	0.95
b	0.25	-	0.38
c	0.09	-	0.22
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.75	-	5.05
e	0.65 BSC		
L	0.40	-	0.80
θ	0°	-	6°

Tape Information

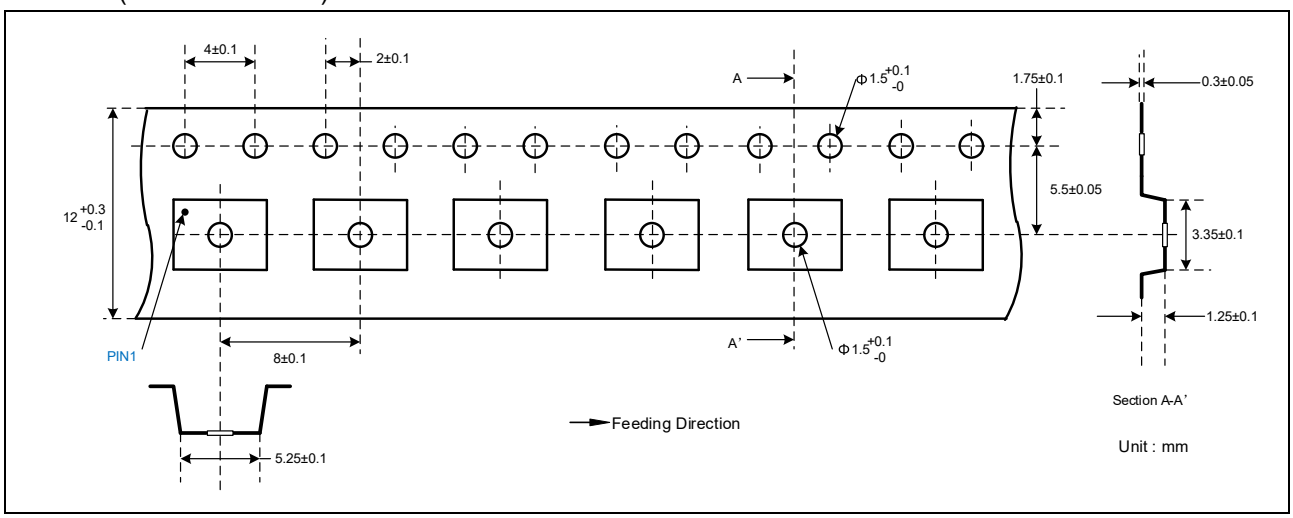
DFN8 (1.4mm × 1mm)



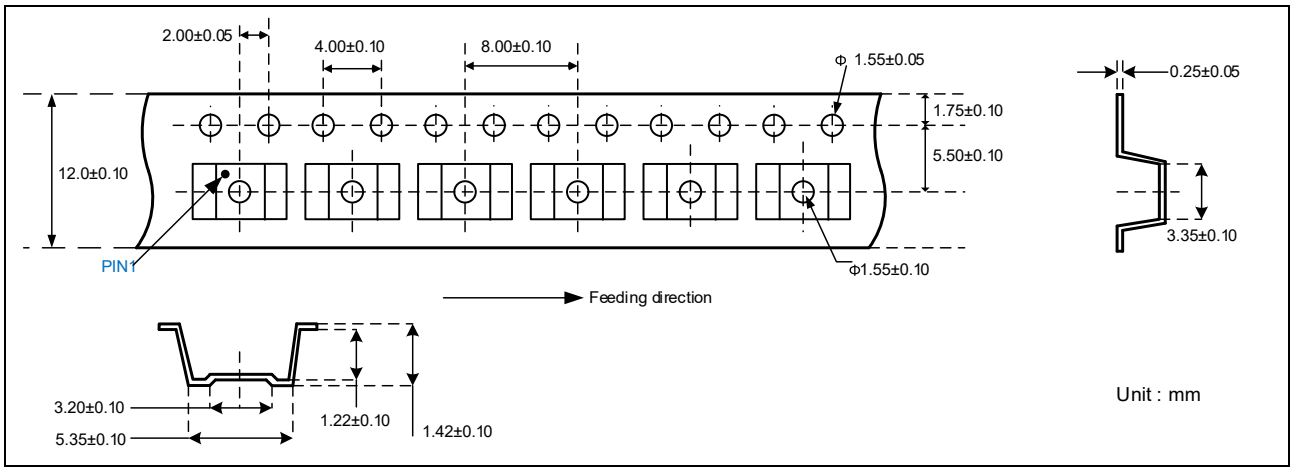
SOP8 (2.0mm × 2.3mm)



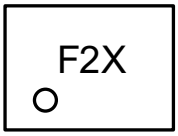
VSSOP8 (2.0mm × 2.3mm)



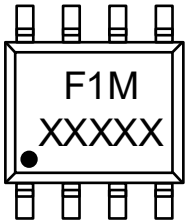
MSSOP8 (3.0mm × 3.0mm)



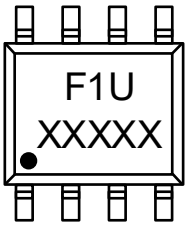
Marking Information



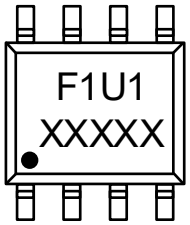
F2 = Part Number
X = Tracking Number
DFN8 (1.4mm × 1mm)



F1M = Part Number
XXXXX = Tracking Number
SOP8 (3.9mm × 4.9mm)



F1U = Part Number
XXXXX = Tracking Number
VSSOP8 (2.0mm × 2.3mm)



F1U1 = Part Number
XXXXX = Tracking Number
MSOP8 (3.0mm × 3.0mm)

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2026-09-11	Official Version	Lu Shao Jie	Liu Yi Guo	Liu Jia Ying