ET61696 - Constant Current LED Matrix Driving Circuit

General Description

ET61696 is a high-performance single-channel, controllable brightness constant current LED matrix driver control specialized integrated circuit. It can drive a 16×6 dot matrix LED display at its maximum capacity and supports the I^2C communication protocol for flexible control. Its internal circuit integrates a group of multi-function registers, allowing for programmable implementation of various display effects. It also features a 256-level single-channel brightness adjustment function, capable of meeting the high-quality driving requirements for various household appliance display screens.

Features

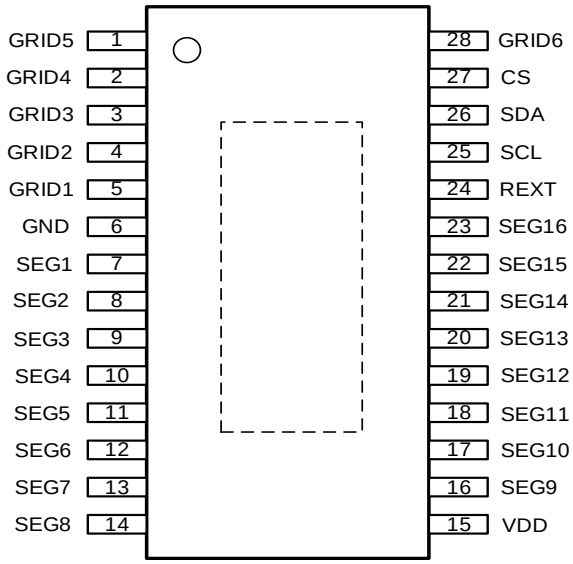
- Power supply voltage range: 2.7～5.5V
- Maximum application dot matrix: 16×6, maximum driving capacity: 96 LEDs
- 16-channel constant current drive, maximum output current: 30mA (under internal resistance condition)
- Overall current supports 64-level adjustment
- Each point supports 256-level brightness adjustment
- Communication interface: I^2C interface
- Built-in clock module
- Built-in power-on reset module
- Built-in sleep mode
- Built-in blanking function
- Product name and packaging form:

Part No.	Package	MSL
ET61696S	EQSOP28	3

Applications

- Smart Furniture Devices, Smart Panels, Small Home Appliances
- Smart portable devices, Toy display

Pin Configuration



ET61696S

Figure 1. pin configuration (Top View)

Pin Function

Pin No. EQSOP28	Pin Name	Pin Function
7~14,16~23	SEG1~SEG16	Segment output port, connect LED positive
24	REXT	Connect external resistor to GND set the output current of all output channels.; it is recommended to use a minimum value of 2kΩ.
25	SCL	I^2C clock input
26	SDA	I^2C data input
27	CS	Communication interface slave address configuration port
1~5,28	GRID1~GRID6	Grid output port, connected to LED negative
6	GND	Ground pad
15	VDD	Power supply.

Block Diagram

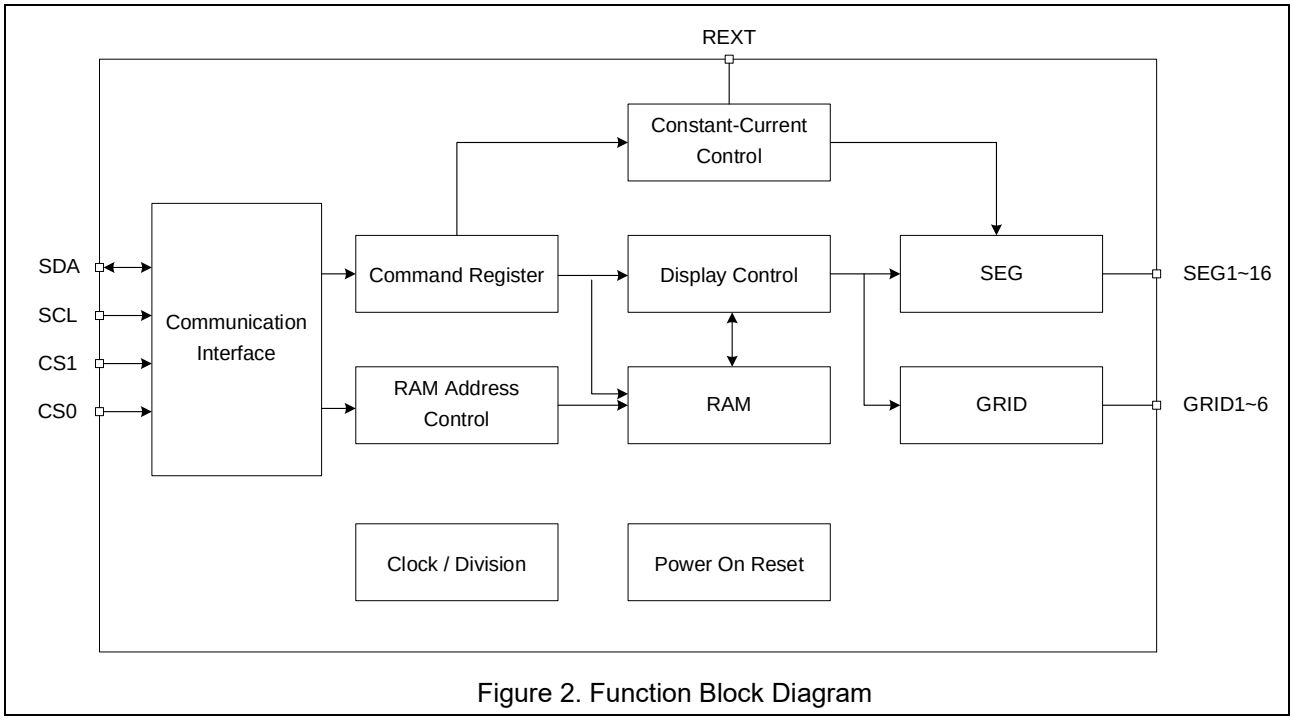


Figure 2. Function Block Diagram

Functions Description

Communication Protocol

Bus Interface

The MCU transmits data to ET61696 through the SDA and SCL ports. SDA and SCL form the I^2C communication interface; an upper pull-up resistor needs to be connected to the power terminal; the slave address is matched through the CS port.

Data Validity

Each byte of the data line consists of 8 bits. The first data transmitted is the MSB.

When the SCL signal is at a high level, the data on the SDA port is stable and valid. Only when the SCL signal is at a low level can the level of the SDA port be changed.

Start (Re-start) and Stop Working Conditions

When the SCL signal is at a high level, the SDA signal starts to work or resumes working when it changes from a high level to a low level. And when the SCL signal is at a high level and the SDA signal changes from a low level to a high level, the working stops.

Acknowledge

During the response clock period, the host keeps the SDA port at a high level. During the write mode period, the ET61626Y will send a response signal to make the SDA port at a low level during the response period.

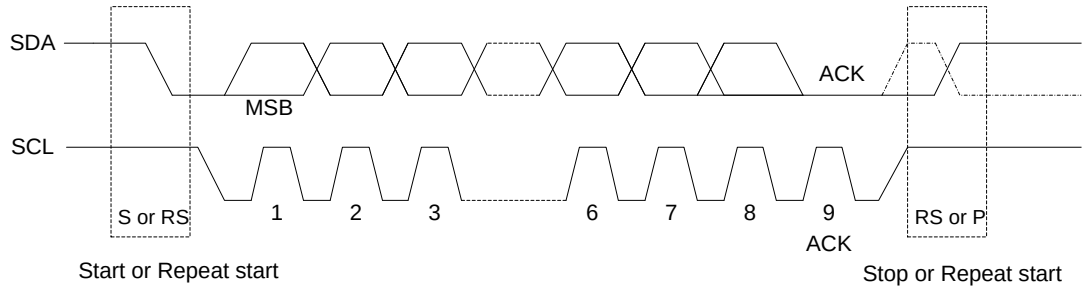


Figure 3. I²C write mode

- ACK = Acknowledge
- MSB = Most Significant Bit
- S = Start
- RS = Restart
- P =Stop
- Restart: SDA-level turnover as expressed by the dashed line waveform

Chip-Address

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	1	1	1	1	0	CS	W/R

CS	Chip-Address (Write)	Chip-Address (Read)
0	0x78	0x79
1	0x7A	0x7B

Data writing format

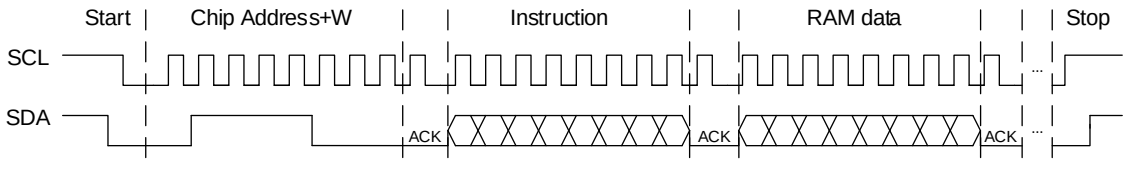


Figure 4. Data writing format

- Start = Start Conditions
- Chip Address=0111100+0(w)b (Taking the case where CS ground are at 0, when the W/R bit is 0, a write operation is executed.)
- ACK = Acknowledge
- Register Instruction

- ACK = Acknowledge
- RAM data
- ACK = Acknowledge
- ……
- Stop

Note1： Starting from the third byte (the RAM data) until the STOP signal is received to indicate the end, all the data written are transferred from the display data to the internal RAM of the chip.

Note2： The starting address of RAM is controlled by the ADS bit (5 bits of the 2nd bit):
When ADS = 0, the starting address of RAM begins at 0x00, and for each display data written, the RAM address will automatically increase by 1;

When ADS = 1, the starting address of RAM is controlled by instructions 10 and 11's AD[7:0], and for each display data written, the RAM address will automatically increase by 1.

Note3： The length of the valid display data written is related to the number of scan lines. When the written display data exceeds this length, the excess display data will be invalid.

Instruction 2		Data RAM data address range display	
G_N[3:0]	**Scan Line**	**ADS=0**	**ADS=1**
0000	1 Scan Line (GRID1)	0x00~0x0F	AD[7:0]~0x0F
0001	2 Scan Line (GRID1~2)	0x00~0x1F	AD[7:0]~0x1F
0010	3 Scan Line (GRID1~3)	0x00~0x2F	AD[7:0]~0x2F
0011	4 Scan Line (GRID1~4)	0x00~0x3F	AD[7:0]~0x3F
0100	5 Scan Line (GRID1~5)	0x00~0x4F	AD[7:0]~0x4F
0101	6 Scan Line (GRID1~6)	0x00~0x5F	AD[7:0]~0x5F

Register instruction

Ins	Bit	Bit name	Default	Access	Description	
1	[7:6]	RESERVED	00	W	Reserved	
	[5:0]	SEGn Output current I	000000	W	Built-in resistor	2kΩ external resistor
					000000b = 6.375mA …… 011111b = 18mA …… 111111b = 30mA	000000b = 9.52mA …… 011111b = 26.88mA …… 111111b = 44.8mA

Note1： When using the internal resistance (instruction 5 RES[1]=0), ISEGn = 0.375 × (17 + I[5:0]).

Note2： When using an external resistor (instruction 5 RES[1]=1), ISEGn = 1.12 × (17 + I[5:0]) ÷ REXT, and it is recommended to use a minimum value of 2kΩ.

Ins	Bit	Bit name	Default	Access	Description
2	[7:4]	RESERVED	0100	W	Reserved
	[3:0]	Scan line G_N	0000	W	0000b = 1 scan line (GRID1)

					…… 0100b = 5 scan line (GRID1~5) 0101b = 6 scan line (GRID1~6)

Ins	Bit	Bit name	Default	Access	Description
4	[7:4]	RESERVED	0101	W	Reserved
	[3:2]	DT	00	W	00b = 4 system clock 01b = 8 system clock 10b = 16 system clock 11b = 24 system clock
	[1]	TP2	0	W	0b = Enable Over-temperature Protection 2. When the IC temperature exceeds 150℃, turn off the SEG output. 1b = Disable over-temperature protection 2
	[0]	TP1	0	W	0b = Enable Over-temperature Protection 1. When the IC temperature exceeds 125℃, the SEG output current changes to 2/3 of the originally set value. 1b = Disable over-temperature protection 1

Ins	Bit	Bit name	Default	Access	Description
5	[7:4]	RESERVED	0110	W	Reserved
	[3]	SVGD	0	W	0b = SEG output current ≥ 10mA,it is recommended to set it to 0 1b = SEG output current < 10mA,it is recommended to set it to 1
	[2]	ADS	0	W	0b = When RAM is read or written, the address starts at 0x00 and automatically increments. 1b = When RAM is read or written, the address starts from AD[7:0] and automatically increments.
	[1]	RES	0	W	0b = Set constant current using internal resistor 1b = Set constant current using external resistor via REXT port
	[0]	SLEEP	0	W	0b = Work mode 1b = Sleep mode

Ins	Bit	Bit name	Default	Access	Description
6	[7:4]	RESERVED	1000	W	Reserved
	[3:2]	FR	00	W	9 scan conditions： 00b = 400Hz 01b = 800Hz 10b = 1600Hz 11b = 3200Hz

	[1]	DON	0	W	0b = SEG display disable 1b = SEG display enable
	[0]	GS	0	W	0b = SEG blanking function disable 1b = SEG blanking function enable

Ins	Bit	Bit name	Default	Access	Description
8	[7:4]	RESERVED	1001	W	Reserved
	[3:2]	RESERVED	00	W	Reserved
	[1]	GRE	0	W	0b = working mode 1b = Soft reset. Cleared after the Stop signal
	[0]	LVRE	0	W	0b = Disable power-off reset 1b = Enable power-off reset. The reset voltage is approximately 2V.

Note： After performing a soft reset, all the instruction registers will be reset to their default values, while the data in the RAM remains unchanged.

Ins	Bit	Bit name	Default	Access	Description
10	[7:5]	RESERVED	110	W/R	Reserved
	[4]	RESERVED	0	W/R	Reserved
	[3:0]	ADS mode RAM address AD[7:4]	0000	W/R	0b = This bit can be set, but it is ineffective. 1b = This is the starting address of the control RAM.

Ins	Bit	Bit name	Default	Access	Description
11	[7:5]	RESERVED	111	W/R	Reserved
	[4]	RESERVED	0	W/R	Reserved
	[3:0]	ADS mode RAM address AD[3:0]	0000	W/R	0b = This bit can be set, but it is ineffective. 1b = This is the starting address of the control RAM

LEDn PWM (n=1~144)			
RAM Addr	**Bit**	**Bit Name**	**Description**
00H~5FH	[7:0]	LEDn PWM DATA	00000000b = 0/255 duty cycle ..... 01111111b = 127/255 duty cycle ..... 11111111b = 255/255 duty cycle

LED dot matrix diagram

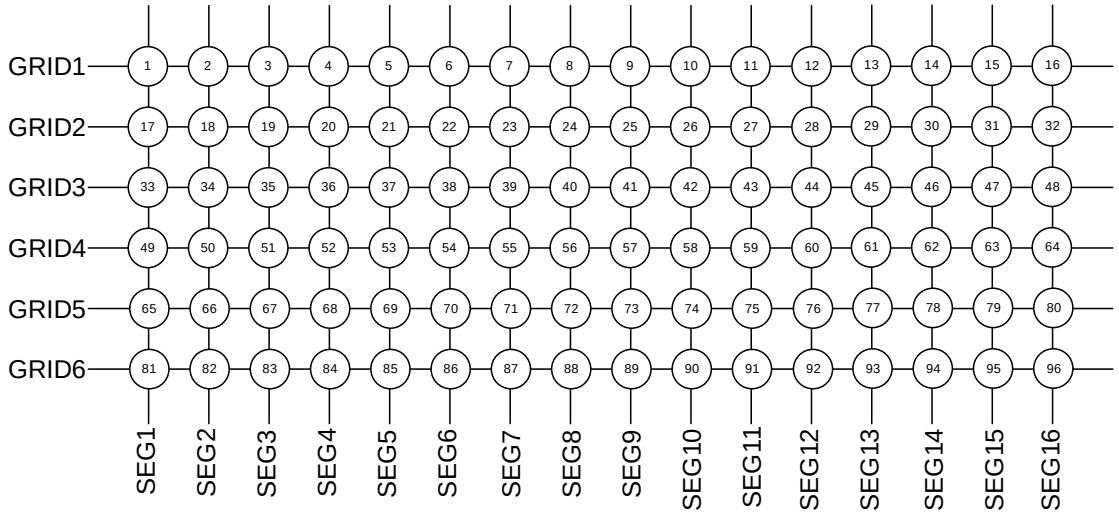


Figure 5. LED dot matrix diagram

Note： The PWM data corresponding to the 1st point in the RAM starting address diagram of this position is as shown in the table as LED1PWM. The PWM data corresponding to the 96th point in the diagram is as shown in the table as LED96PWM. The data for other points follows the same pattern.

RAM Address and LED Matrix Correspondence Table

ADDR	Description	ADDR	Description	ADDR	Description	ADDR	Description
00H	LED1PWM	01H	LED2PWM	02H	LED3PWM	03H	LED4PWM
04H	LED5PWM	05H	LED6PWM	06H	LED7PWM	07H	LED8PWM
08H	LED9PWM	09H	LED10PWM	0AH	LED11PWM	0BH	LED12PWM
0CH	LED13PWM	0DH	LED14PWM	0EH	LED15PWM	0FH	LED16PWM
10H	LED17PWM	11H	LED18PWM	12H	LED19PWM	13H	LED20PWM
14H	LED21PWM	15H	LED22PWM	16H	LED23PWM	17H	LED24PWM
18H	LED25PWM	19H	LED26PWM	1AH	LED27PWM	1BH	LED28PWM
1CH	LED29PWM	1DH	LED30PWM	1EH	LED31PWM	1FH	LED32PWM
20H	LED33PWM	21H	LED34PWM	22H	LED35PWM	23H	LED36PWM
24H	LED37PWM	25H	LED38PWM	26H	LED39PWM	27H	LED40PWM
28H	LED41PWM	29H	LED42PWM	2AH	LED43PWM	2BH	LED44PWM
2CH	LED45PWM	2DH	LED46PWM	2EH	LED47PWM	2FH	LED48PWM
30H	LED49PWM	31H	LED50PWM	32H	LED51PWM	33H	LED52PWM
34H	LED53PWM	35H	LED54PWM	36H	LED55PWM	37H	LED56PWM
38H	LED57PWM	39H	LED58PWM	3AH	LED59PWM	3BH	LED60PWM
3CH	LED61PWM	3DH	LED62PWM	3EH	LED63PWM	3FH	LED64PWM
40H	LED65PWM	41H	LED66PWM	42H	LED67PWM	43H	LED68PWM
44H	LED69PWM	45H	LED70PWM	46H	LED71PWM	47H	LED72PWM

48H	LED73PWM	49H	LED74PWM	4AH	LED75PWM	4BH	LED76PWM
4CH	LED77PWM	4DH	LED78PWM	4EH	LED79PWM	4FH	LED80PWM
50H	LED81PWM	51H	LED82PWM	52H	LED83PWM	53H	LED84PWM
54H	LED85PWM	55H	LED86PWM	56H	LED87PWM	57H	LED88PWM
58H	LED89PWM	59H	LED90PWM	5AH	LED91PWM	5BH	LED92PWM
5CH	LED93PWM	5DH	LED94PWM	5EH	LED95PWM	5FH	LED96PWM

Note： Each address contains 8 bits of data, corresponding to the PWM level of that point (256 levels).

Absolute Maximum Ratings

Symbol	Characteristic	Rating	Unit
V_{DD}	Supply Voltage	-0.3~6.0	V
V_I	Logic Input Voltage	-0.3~V_{DD}+0.3	V
T_{JMAX}	Max Junction Temperature	150	°C
P_D	Power Dissipation	1200	mW
T_{STG}	Storage Temperature Range	-65～150	°C
V_{ESD}	HBM	±2	KV
	CDM	±1	KV

Recommended Operating Conditions

Symbol	Characteristic	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	2.7	5.0	5.5	V
V_{IH}	High Level Input Voltage	3.0	-	V_{DD}	V
V_{IL}	Low Level Input Voltage	0	-	1.5	V
T_A	Operating Temperature	-40	-	+85	°C

Electrical Characteristics

(Unless otherwise specified，T_A = 25°C，V_{DD}= 5V，GND= 0V)

Symbol	Characteristic	Test Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		2.7	5.0	5.5	V
I_{SEG}	High Level Output Current	V_{SEGn} = 4V (n=1~16), RES[6] = 0 (Built-in resistor), I[5:0] = 111111.	-28	-30	-32	mA
		V_{SEGn} = 4V (n=1~16), RES[6] = 1 (2kΩ external resistor)，I[5:0] = 111111.	-42	-44.8	-48	mA
I_{GRID}	Low Level Output Current	V_{GRIDn}=0.4V（n=1~6）	500	-	-	mA
V_{IH}	High Level Input Voltage	SCL, SDA	3.0	-	V_{DD}	V
V_{IL}	Low Level Input	SCL, SDA	0	-	1.5	V

	Voltage					
I_{DD}	Dynamic current Dissipation	No load, Display off	-	-	5	mA
I_{SLEEP}	Sleep current	Sleep mode	-	-	300	uA

Communication timing characteristics

(Unless otherwise specified，T_A = 25°C，V_{DD}= 5V，GND= 0V)

Symbol	Test Condition	Min	Typ	Max	Unit
F_{SCL}	SCL Clock Frequency	-	-	1	MHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	-	0.5	-	μs
$t_{HD:STA}$	Hold Time(Repeated) START Condition	-	0.26	-	μs
t_{LOW}	Low Period of SCL Clock	-	0.5	-	μs
t_{HIGH}	HIGH Period of SCL Clock	-	0.26	-	μs
$t_{SU:STA}$	Setup Time for a Repeated START Condition	-	0.26	-	μs
$t_{HD:DAT}$	Data Hold Time	-	0	-	μs
$t_{SU:DAT}$	Data Setup Time	-	50	-	ns
t_R	Data Hold Time2	-	-	300	ns
t_F	Data Hold Time2	-	-	300	ns
$t_{SU:STO}$	Setup Time for STOP Condition	-	0.26	-	μs

I²C Timing Waveform

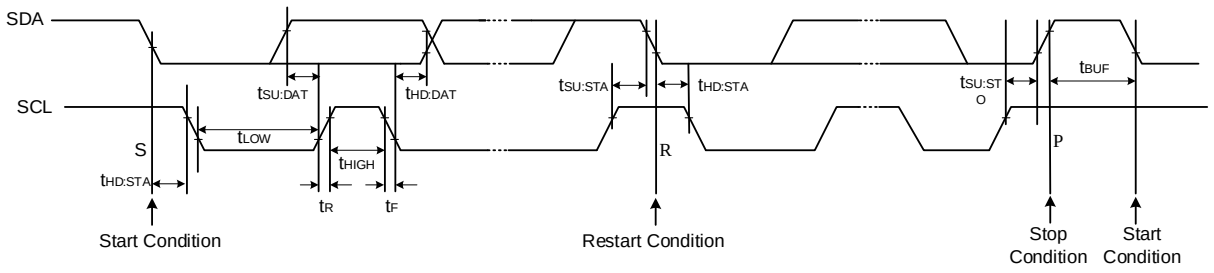


Figure 6. I²C Timing Waveform

Application circuit

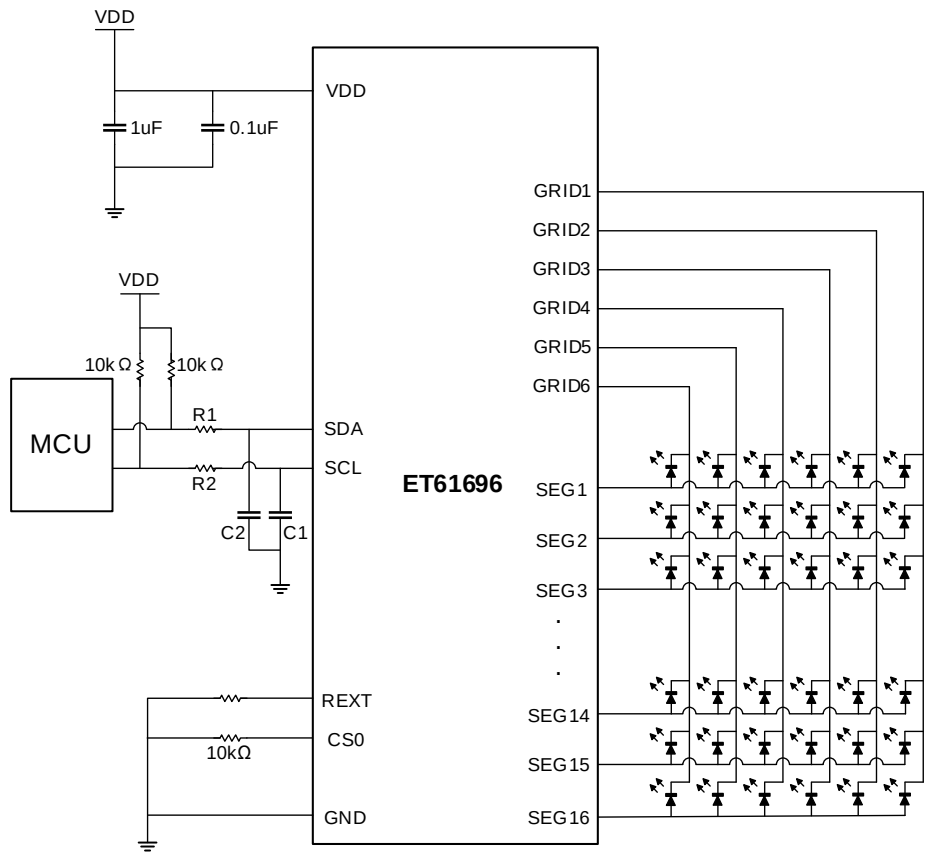


Figure 7. Application Circuit

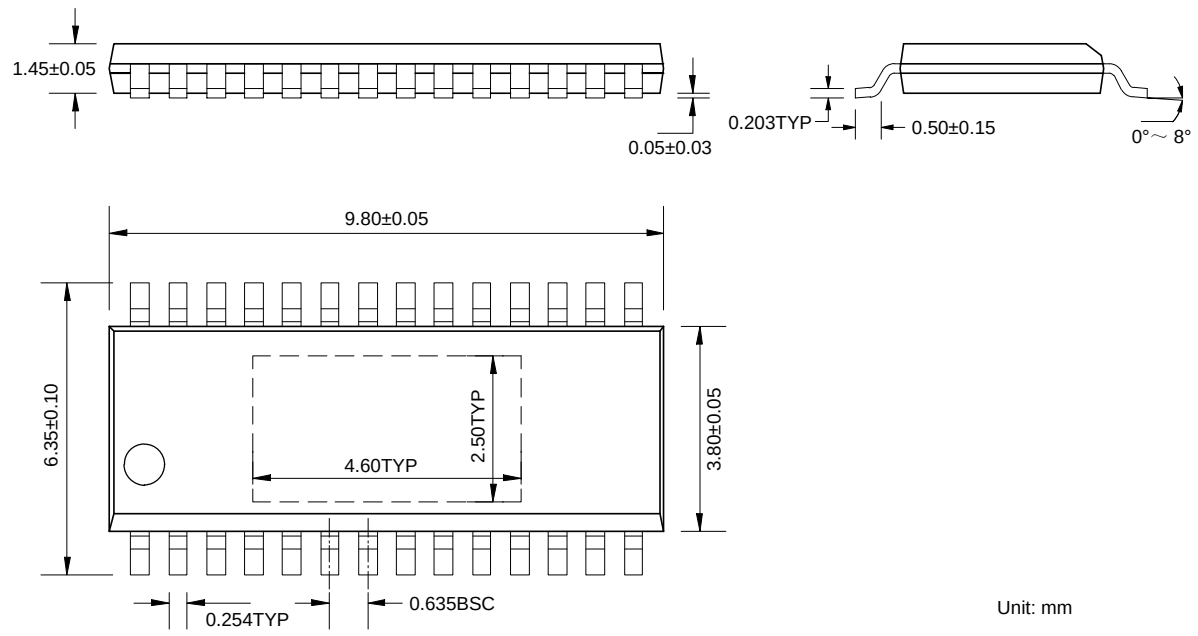
Note： This application diagram is for reference only.

It is recommended that the power filter capacitor be placed as close as possible to the VDD pin;

Adding RC filtering at the communication port can enhance the anti-interference performance, and it should be placed as close as possible to the chip end. The values of the resistors and capacitors (R1 = R2 = 100Ω, C1 = C2 = 100pF) can be adjusted according to the actual anti-interference requirements and verification results.

Package Dimension

EQSOP28



Marking



XXXXX=Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2026-09-10	Original Version	Zhuang Chao	Li Chen Xuan	Liu Jia Ying