SD3.0-SDR104 Compliant Integrated Auto-direction Control Memory Card Voltage Level Translator

General Description

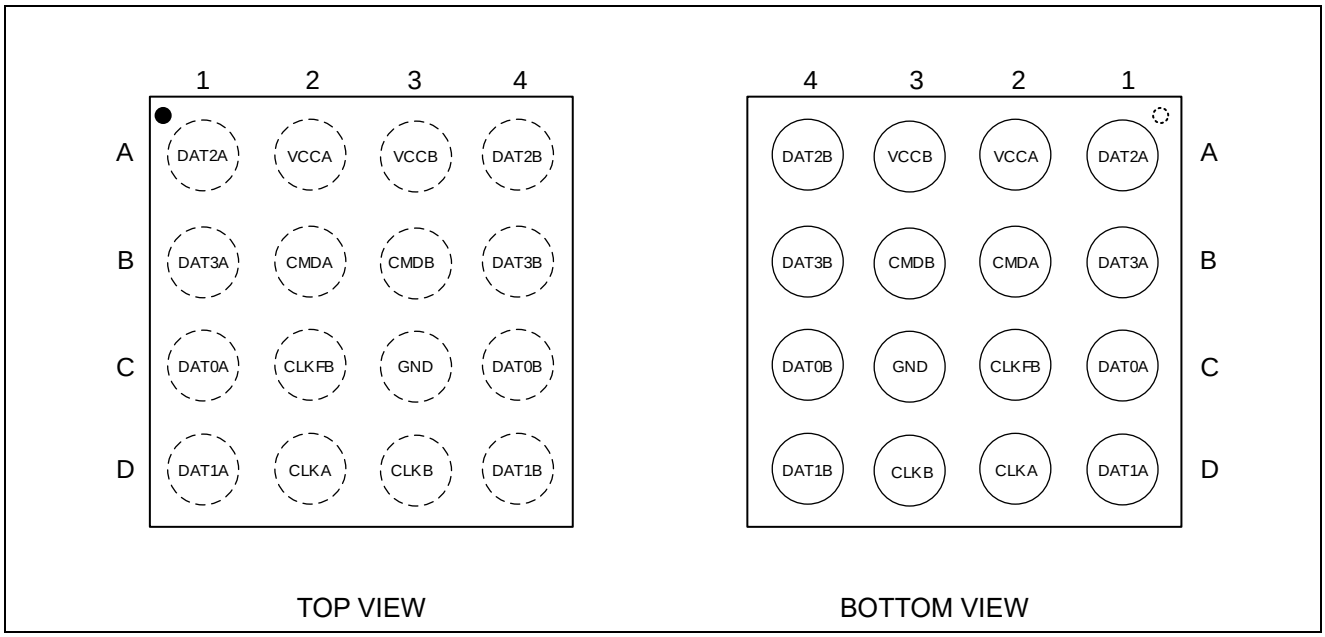
The ET4860 is a SD 3.0-compliant bidirectional dual voltage level translator with auto-direction control. It is designed to interface between a memory card operating at 1.8V or 3.3V (up to 3.6V) signal levels and a host with a nominal supply voltage of 1.2V to 1.8V. The IC supports SD3.0 SDR104、SDR50、DDR50、SDR25、SDR12 and SD2.0 High-Speed (50MHz) and Default-Speed (25MHz) modes.

Features

- Supports up to 208MHz clock rate
- SD3.0 specification-compliant voltage translation to support SDR104, SDR50, DDR50, SDR25, SDR12, High-Speed and Default-Speed modes
- 1.2V to 1.8V host side interface voltage support
- Feedback channel for clock synchronization
- Low power consumption by push-pull output stage with break-before-make architecture
- Integrated pull-up and pull-down resistors: no external resistors required
- Integrated EMI filters suppress higher harmonics of digital I/Os
- Integrated 8kV ESD protection according to IEC 61000-4-2, level 4 on card side
- Level shifting buffers keep ESD stress away from the host (zero-clamping concept)
- Package information:

Part No.	Package	Packing	MSL
ET4860	WLCSP16 (1.38mm × 1.38mm)	3.0K/Reel	1

Pin Configuration



Pin Function

Pin No.	Pin Name	Pin Function
A1	DAT2A	Data 2 input or output on host side
A2	VCCA	Supply Voltage from host side
A3	VCCB	supply voltage B (memory card side)
A4	DAT2B	Data 2 input or output on memory card side
B1	DAT3A	Data 3 input or output on host side
B2	CMDA	Command input or output on host side
B3	CMDB	Command input or output on memory card side
B4	DAT3B	Data 3 input or output on memory card side
C1	DAT0A	Data 0 input or output on host side
C2	CLK_FB	Clock feedback output on host side
C3	GND	Supply Ground
C4	DAT0B	Data 0 input or output on memory card side
D1	DAT1A	Data 1 input or output on host side
D2	CLKA	Clock signal input on host side
D3	CLKB	Clock signal output on memory card side
D4	DAT1B	Data 1 input or output on memory card side

Block Diagram

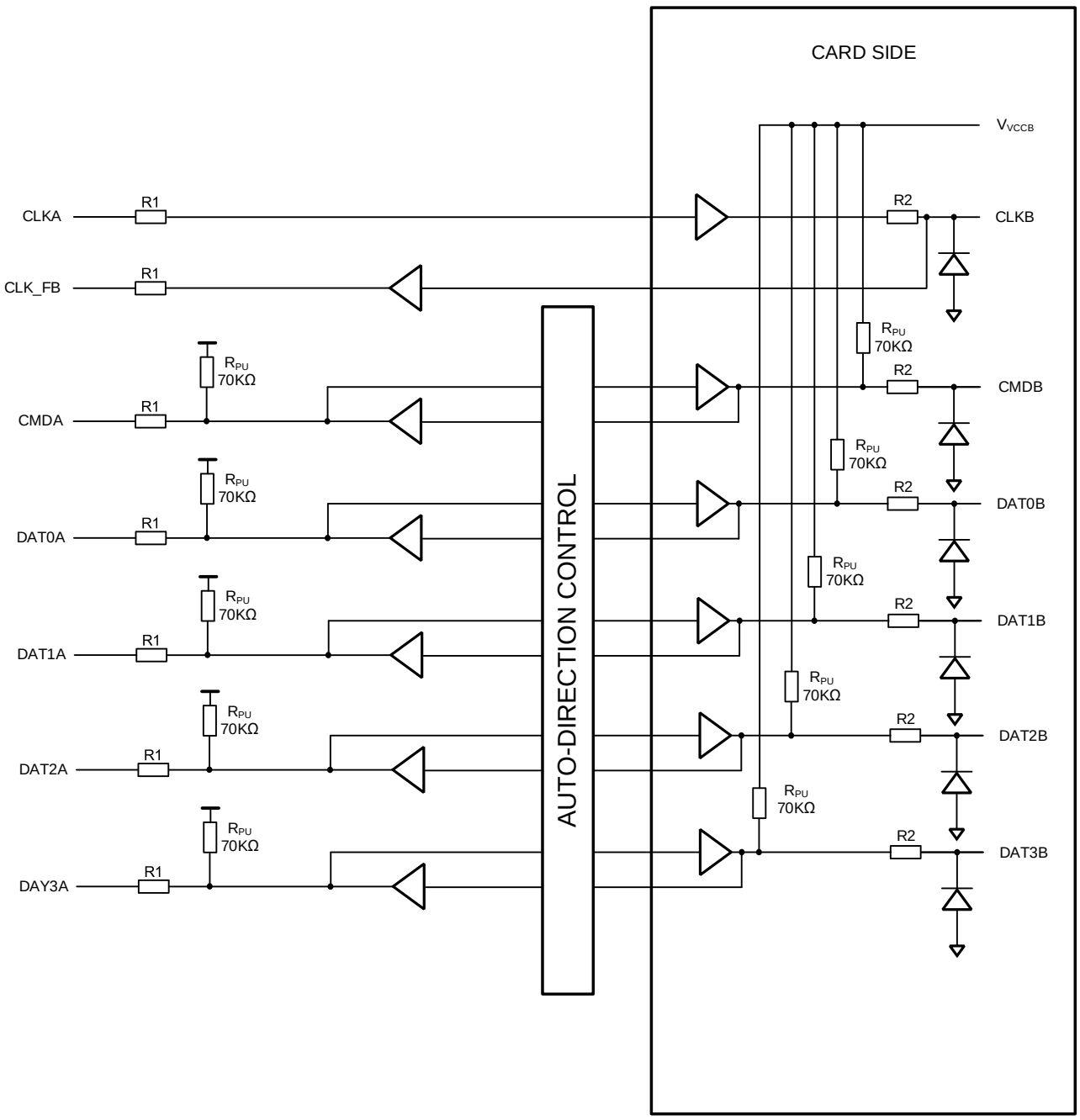


Figure1. Block Diagram

Functional Description

Level Translate

The bidirectional level translator shifts the data between the I/O supply levels of the host and the memory card. The voltage translator has to support several clock and data transfer rates at the signaling levels specified in the SD 3.0 standard specification.

Supported Modes table+

Bus Speed Mode	Signal Level (V)	Clock Rate (MHz)	Data Rate (MB/s)
Default Speed	3.3	25	12.5
High-Speed	3.3	50	25
SDR12	1.8	25	12.5
SDR25	1.8	50	25
SDR50	1.8	100	50
SDR104	1.8	208	104
DDR50	1.8	50	50

Feedback clock channel

The clock is transmitted from the host to the memory card side. The voltage translator and the Printed-Circuit Board (PCB) tracks introduce some amount of delay. It reduces timing margin for data read back from memory card, especially at higher data rates. Therefore, a feedback path is provided to compensate the delay. The reasoning behind this approach is the fact that the clock is always delivered by the host, while the data in the timing critical read mode comes from the card.

EMI filter

ET4860's all input/output ports are equipped with EMI filters to reduce interferences towards sensitive mobile-communication.

ESD protection

ET4860 has robust ESD protections on all memory card pins. The architecture prevents any stress for the host: the voltage translator discharges any stress to supply ground.

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters		Condition	Rating	Unit
V_{CC}	Supply Voltage		VCCA pins (4ms transient)	-0.5 ~ 4.6	V
V_{IN}	Input Voltage		I/O pins (4ms transient)	V_{SS}-0.3 ~ V_{DD}+0.3	V
P_D	Power Dissipation		T_A = 25°C	250	mW
T_J	Junction Temperature Range		-	-40 ~ +150	°C
T_{STG}	Storage Temperature Range		-	-65 ~ +150	°C
V_{ESD}[(1)]	(IEC 61000-4-2)	Contact discharge	All memory card side pins	±8	kV
		Air discharge		±15	
	HBM (JESD22-A114)		All Pins	±2	
	CDM (JESD22-C101)		All Pins	±0.5	
I_{LU}	Max Latch-up Current (JESD78B)		I/O port: -0.5V_{CC} < V_I <1.5V_{CC}	±100	mA

Note(1): ESD test, all system level tests are performed with the application-specific capacitors connected to the supply pins V_{CCA} and V_{CCB}.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. We do not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameters	Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	V_{CCB}[(2)]	1.7	-	3.6	V
		V_{CCA}	1.1	-	2.0	
V_{IN}	Input Voltage	Host side[(3)]	-0.3	-	V_{CCA}+0.3	V
		Memory card side	-0.3	-	V_{CCB}+0.3	
C_{EXT}	Recommended External Capacitance	Capacitor connect to V_{CCB}		2.2		µF
		Capacitor connect to V_{CCA}		0.1		µF
ESR	Equivalent series resistance	At pin V_{CCB}	0	-	50	mΩ
T_A	Operate Temperature Range		-40		+85	°C

Note(2): By minimum value the device is still fully functional.

Note(3): The voltage must not exceed 3.6V.

Integrated Resistors in Block Diagram (T_A=25°C)

Symbol	Parameters	Condition	Min	Typ	Max	Unit
R_{PU}	Pull-up Resistance	All data lines and CMDx	49	70	91	KΩ
R_S	Series Resistance	Host side, R1, tolerance ±30%	-(4)	22.5		Ω
		Card side, R2, tolerance ±30%	-(4)	15		Ω

Note(4): Guaranteed by design.

Electrical Characteristics

Recommended operating conditions: T_A= -40 ~ 85°C(5)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Host-side input signals: CMDA and DAT0A to DAT3A, CLKA; host-side control singnal:1.1V≤V_{CCA}≤2.0V						
V_{IH}	Input voltage high level		0.75×V_{CCA}	-	V_{CCA}+0.3	V
V_{IL}	Input voltage low level		-0.3	-	0.25×V_{CCA}	V
Host-side output signals: CLK_FB, CMDA, DATA0A to DATA3A; 1.1V≤V_{CCA}≤2.0V						
V_{OH}	Output voltage high level for CLK_FB	I_O=-2mA, V_I=V_{IH}(card side)	0.8×V_{CCA}	-	-	V
	Output voltage high level for CMDA, DATxA	I_O=-2μA, V_I=V_{IH}(card side)	0.8×V_{CCA}	-	-	V
V_{OL}	Output voltage low level	I_O=2mA, V_I=V_{IL}(card side)	-	-	0.15×V_{CCA}	V
Card-side input signals: CMDB and DAT0B to DAT3B						
V_{IH}	Input voltage high level	1.8V card interface	0.625×V_{CCB}	-	V_{CCB} + 0.3	V
V_{IL}	Input voltage low level	1.8V card interface	-0.3	-	0.3 × V_{CCB}	V
Card-side output signal (CMDB and DAT0B to DAT3B, CLKB)						
V_{OH}	Output voltage high level for CLKB only	I_O=-2mA, V_I=V_{IH}(host side);	0.85×V_{CCB}	-	2.0	V
	Output voltage high level for CMDB, DATxB	I_O=-2μA, V_I=V_{IH}(host side);	0.85×V_{CCB}	-	2.0	V
V_{OL}	Output voltage low level	I_O=2mA, V_I=V_{IL}(host side);	-0.3	-	0.125× V_{CCB}	V
Bus signal equivalent capacitance						
C_{ch}	Channel capacitance (V_I=0 V, f_i=1MHz, V_{CCA}=1.8 V)	Host side	-(6)	7	-	pF
		Card side	-	15	-	pF
Current consumption						
$I_{CC(stb)}$	Standby supply current	V_{CCA} ≥ 1.0V, All host side input = High	-	-	7	μA

Note(5): Typical values are measured at T_A = 25°C.

Note(6): EMI filter line capacitance per data channel from I/O driver to pin; C_{ch} is guaranteed by design.

Level Translator(T_A=25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Host side transition times[7]						
t_r	Rise time	V_{CCA}=1.8V	-	0.4	1.0	ns
t_f	Fall time		-	0.4	1.0	ns
t_r	Rise time	V_{CCA}=1.2V	-	0.4	1.0	ns
t_f	Fall time		-	0.4	1.0	ns
Card side transition times[8]						
t_r	Rise time	-40°C ≤T_A≤ 85°C	0.4	0.88	1.32	ns
t_f	Fall time		0.4	0.88	1.32	ns
Card input transition times[9]						
t_r	Rise time	-40°C ≤T_A≤ 85°C	0.2	0.5	0.96	ns
t_f	Fall time		0.2	0.45	0.96	ns
Host to card propagation delay						
DATAxA to DATAxB, CMDA to CMDB, CLKA to CLKB						
t_{pd}	Propagation delay	V_{CCA}=1.2V, VCCB = 1.8 V	-	3.1	5.4	ns
		V_{CCA}=1.2V, VCCB = 3.3 V	-	2.2	4.0	ns
		V_{CCA}=1.8V, VCCB = 1.8 V	-	2.7	4.8	ns
		V_{CCA}=1.8V, VCCB = 3.3 V	-	1.7	3.1	ns
t_{SK}	output skew time	V_{CCA}=1.2V, VCCB = 1.8 V	-	-	200	ps
		V_{CCA}=1.2V, VCCB = 3.3 V	-	-	200	ps
		V_{CCA}=1.8V, VCCB = 1.8 V	-	-	200	ps
		V_{CCA}=1.8V, VCCB = 3.3 V	-	-	200	ps
Card to host propagation delay						
DATxB to DATxA, CMDB to CMDA						
t_{pd}	Propagation delay	V_{CCA}=1.2V, VCCB = 1.8 V	-	2.7	4.6	ns
		V_{CCA}=1.2V, VCCB = 3.3 V	-	1.7	3.0	ns
		V_{CCA}=1.8V, VCCB = 1.8 V	-	2.7	4.6	ns
		V_{CCA}=1.8V, VCCB = 3.3 V	-	1.6	2.7	ns
t_{SK}	output skew time	V_{CCA}=1.2V, VCCB = 1.8 V	-	-	200	ps
		V_{CCA}=1.2V, VCCB = 3.3 V	-	-	200	ps
		V_{CCA}=1.8V, VCCB = 1.8 V	-	-	200	ps
		V_{CCA}=1.8V, VCCB = 3.3 V	-	-	200	ps
Host to host propagation delay						
CLKA to CLK_FB						
t_{pd}	Propagation delay	V_{CCA}=1.2V, VCCB = 1.8 V	-	5.8	10	ns
		V_{CCA}=1.2V, VCCB = 3.3 V	-	3.9	7.0	ns
		V_{CCA}=1.8V, VCCB = 1.8 V	-	5.4	9.4	ns
		V_{CCA}=1.8V, VCCB = 3.3 V	-	3.3	5.8	ns

Note(7): Transition between V_{OL}=0.35×V_{CCA} and V_{OH}=0.65×V_{CCA}.

Note(8): Transition between V_{OL}=0.45V and V_{OH}=1.4V.

Note(9): Guaranteed by design; transition between V_{IL}=0.58V and V_{IH}=1.27V with C_{trace}=3.5pF and C_{card}+C_{RADLE} =12pF, trace length=11mm.

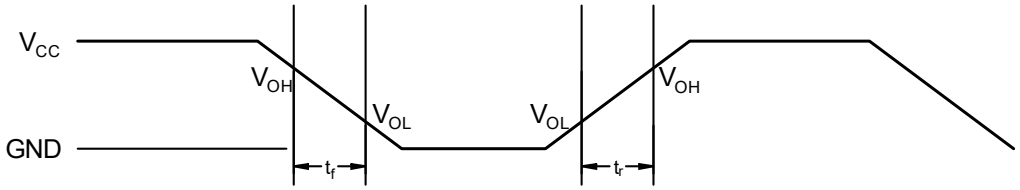


Figure2. Output rise and fall times

Test point: V_{OH} and V_{OL} are specified as ***Note(7)*** and ***Note(8)***

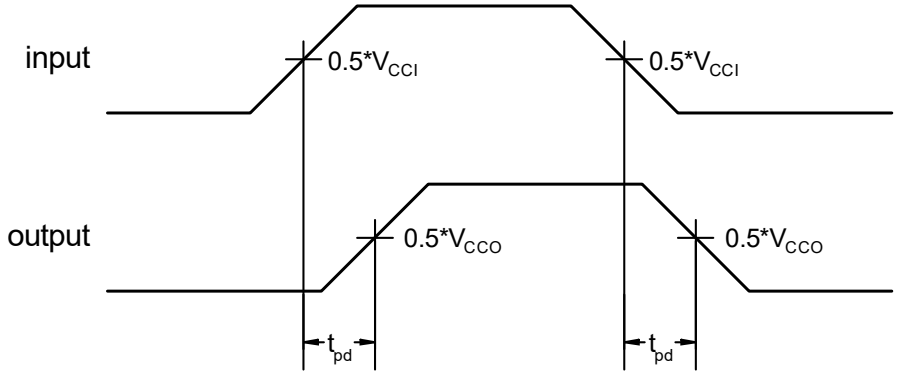
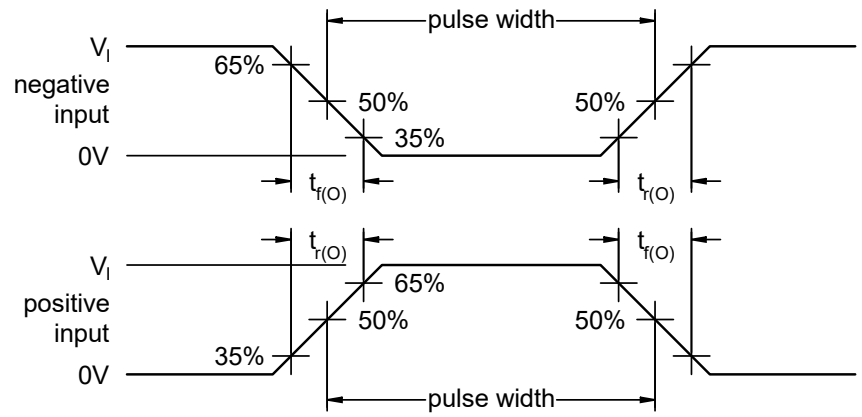


Figure3. Output delay timing

Test point: Output delay is for every single channel, from input to output, 0.5×V_{CCI} to 0.5×V_{CCO}, in which V_{CCI} and V_{CCO} are the input and output voltage domain.

Test Information



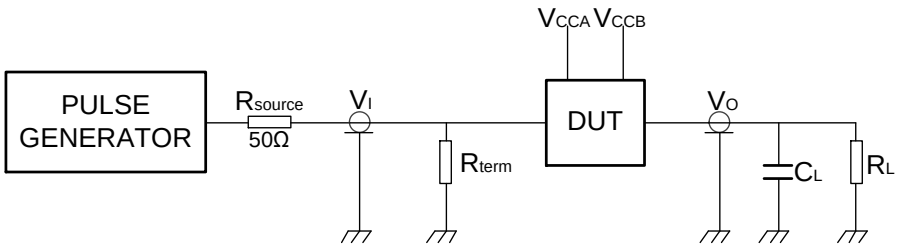


Figure4. Load circuitry for measuring switching time

Definitions test circuit:

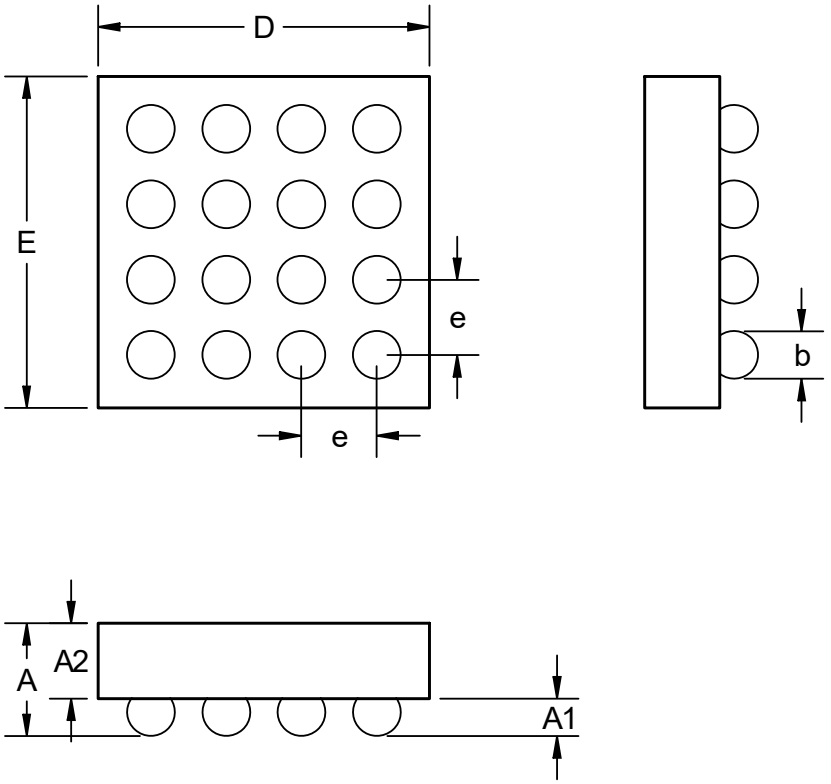
R_{source} = source resistance of pulse generator.

R_{term} = termination resistance should be equal to output impedance Zo of pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

Package Dimension

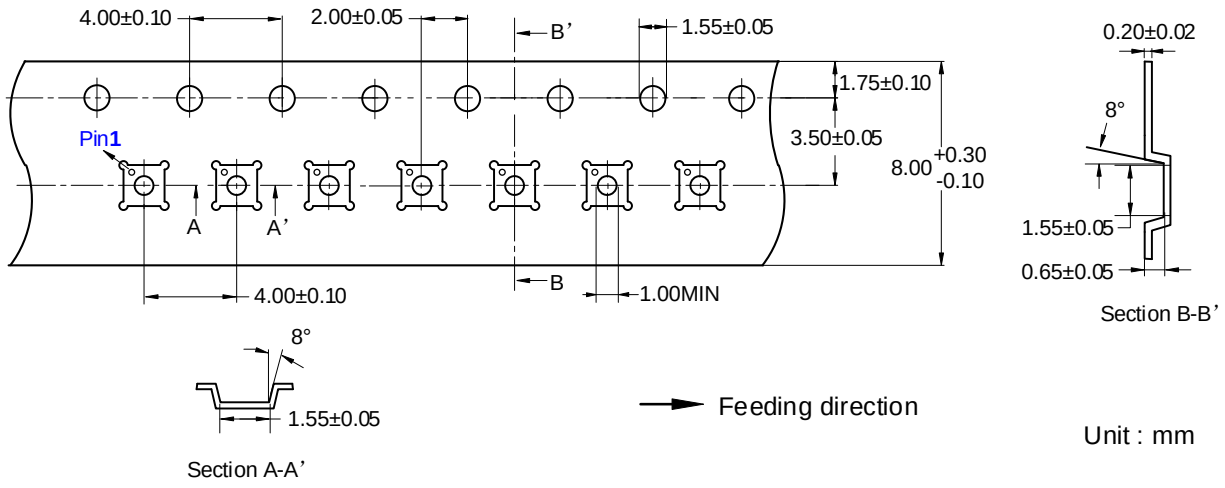


Dimensions Table (Units: mm)

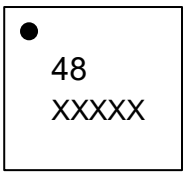
SYMBOL	MIN	NOM	MAX
A	0.425	0.455	0.485
A1	0.150	0.170	0.190
A2	0.2475	0.260	0.2725
b	0.205	0.225	0.245
D	1.360	1.380	1.400
E	1.360	1.380	1.400
e	0.350 BSC		

Tape Information

WLCSP16 (1.38mm × 1.38mm)



Marking Information



48 - Part Number

XXXXX - Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2026.01.16	Original Version	Tianqh	Niwt	Liujy
1.1	2026.06.12	Update the parameters of Level Translator	Tianqh	Niwt	Liujy
1.2	2026.07.27	Add Tape	Tianqh	Niwt	Liujy
1.3	2026.08.26	Add Marking	Tianqh	Niwt	Liujy
1.3.a	2026.09.15	Correct the erroneous description	Tianqh	Niwt	Liujy