ET6408 - 8 bit I²C-bus/SM bus I/O Expander

General description

The ET6408 is an 8-bit universal I/O port expansion IC. It provides up to 8 I/O port expansion functions for MCU through I²C-bus /SM bus interface. It also has level conversion function, which makes it flexible to be used in multi-voltage mixed signal communication environment.

The ET6408 has two supply voltages: VDDI and VDDP.VDDI provides the power supply voltage for the master terminal (MCU) interface, and VDDP provides the power supply voltage for the internal core circuit and 8-bit I/O port.

The ET6408 has four main sets of registers: configuration register, input register, output register and polarity reversal register.

During power-on, all I/O ports are configured as input by default.By configuring registers, the system can determine the input/output status of each I/O port.Each input or output data is stored in the corresponding input or output register.The polarity of the input register can be reversed by configuring the polarity reversal register to save external logic gates.

In addition, the ET6408 has other eight registers: adjust output drive strength register, input latch register, Pull-up/Pull-down enable resistor, Pull-up/Pull-down resistors type choice register, interrupt shielding register, interrupt status register, output state control register.By configuring the register, you can configure corresponding to various states.

When a timeout or error occurs, the host can $\overline{\text{RESET}}$ ET6408 by applying a low level on the $\overline{\text{RESET}}$ port. During power-on reset, all registers are restored to their default states and the I²C /SM bus state machine is initialized.

When any input state is different from the corresponding input register state, the ET6408 open missed interrupt ($\overline{\text{INT}}$) output is activated, indicating to the host that the input state has changed. $\overline{\text{INT}}$ can be connected to the interrupt input of the MCU by sending an interrupt signal to notify the MCU of data coming in on the port without going through the I²C-bus.

The ports P0 to P7 output of the ET6408 provide a maximum of 25mA of irrigation current, which can directly drive the LED.

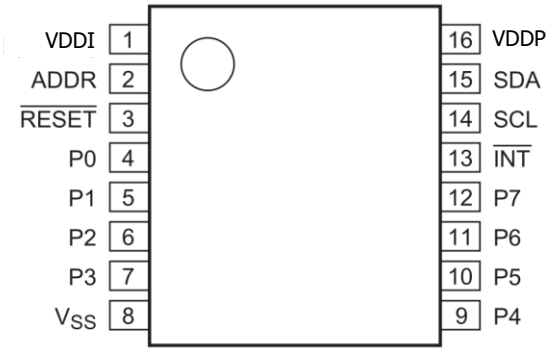
The I²C-bus address can be changed by connecting the ADDR pin to the VDDP or V_{SS}.

Features

- I^2C-bus to parallel port expander
- Operating power supply voltage range of 1.65 V to 5.5 V
- Allows bidirectional voltage-level translation and GPIO expansion between:
  - 1.8 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 2.5 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 3.3 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
  - 5 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
- Low standby current consumption:
  - 1.5 uA typical at V_{DDP} = 5 V
  - 1.0 uA typical at V_{DDP} = 3.3 V
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - V_{HYS} = 0.2 V (typical) at 1.8 V
  - V_{HYS} = 0.3 V (typical) at 2.5 V
  - V_{HYS} = 0.2 V (typical) at 3.3 V
  - V_{HYS} = 0.15 V (typical) at 5 V
- The minimum SDA/SCL input high level less than 1.2V
- Active LOW reset input ($\overline{RESET}$)
- Open-drain active LOW interrupt output ($\overline{INT}$)
- Input/Output Configuration register
- 400 kHz Fast-mode I^2C-bus
- Polarity Inversion register
- Internal power-on reset
- Output has Push-pull and Open-drain modes
- Pull-up resistors and Pull-down resistors can be configured
- Noise filter on SCL/SDA inputs
- Outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA
- ESD protection exceeds
  - ±2000 V Human-Body Model Pass
  - ±1000 V Charged-Device Model Pass
- Device Package:

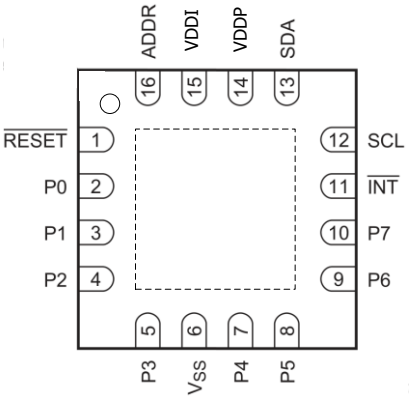
Part No.	Package	Size	Packing	MSL
ET6408V	TSSOP16	Width 4.4 mm	4.0K/Reel	3
ET6408Y	QFN16	3mm ×3mm×0.75 mm	3.0K/Reel	3
ET6408Y1	QFN16L	1.8mm ×2.6mm×0.55 mm	3.0K/Reel	1

Pin Assignments



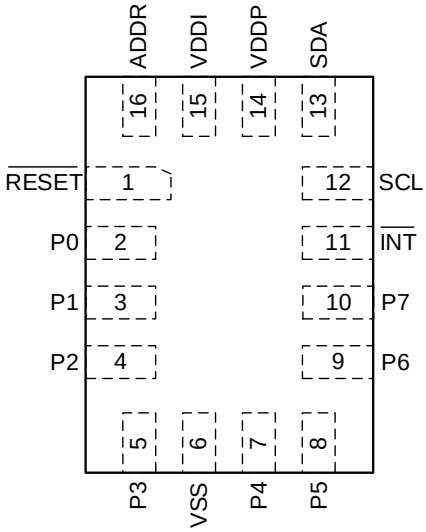
TSSOP16 (ET6408V)

Top View



QFN16 (ET6408Y)

Top View



QFN16L (ET6408Y1)

Top View

Figure 1. Pin Assignments

Pin. Function

Symbol	Pin No.		Description
	TSSOP16	QFN16/QFN16L	
VDDI	1	15	Supply voltage of I^2C-bus. Connect directly to the VDD of the external I^2C master. Provides voltage-level translation.
ADDR	2	16	Address input. Connect directly to VDDP or ground.
$\overline{RESET}$	3	1	Reset input, active low. Connect to VDDI through a Pull-up resistor.

Pin. Function(continued)

Symbol	Pin No.		Description
	TSSOP16	QFN16/QFN16L	
P0	4	2	Port 0 input/output 0.
P1	5	3	Port 0 input/output 1.
P2	6	4	Port 0 input/output 2.
P3	7	5	Port 0 input/output 3.
VSS	8	6	GND
P4	9	7	Port 0 input/output 4.
P5	10	8	Port 0 input/output 5.
P6	11	9	Port 0 input/output 6.
P7	12	10	Port 0 input/output 7.
$\overline{INT}$	13	11	Interrupt the output , connect to VDDI or VDDP through a Pull-up resistor
SCL	14	12	Serial clock bus. Connect to VDD(I2C-bus) through a Pull-up resistor.
SDA	15	13	Serial data bus. Connect to VDD(I2C-bus) through a Pull-up resistor.
VDDP	16	14	Supply voltage for Port P.

Block Diagram

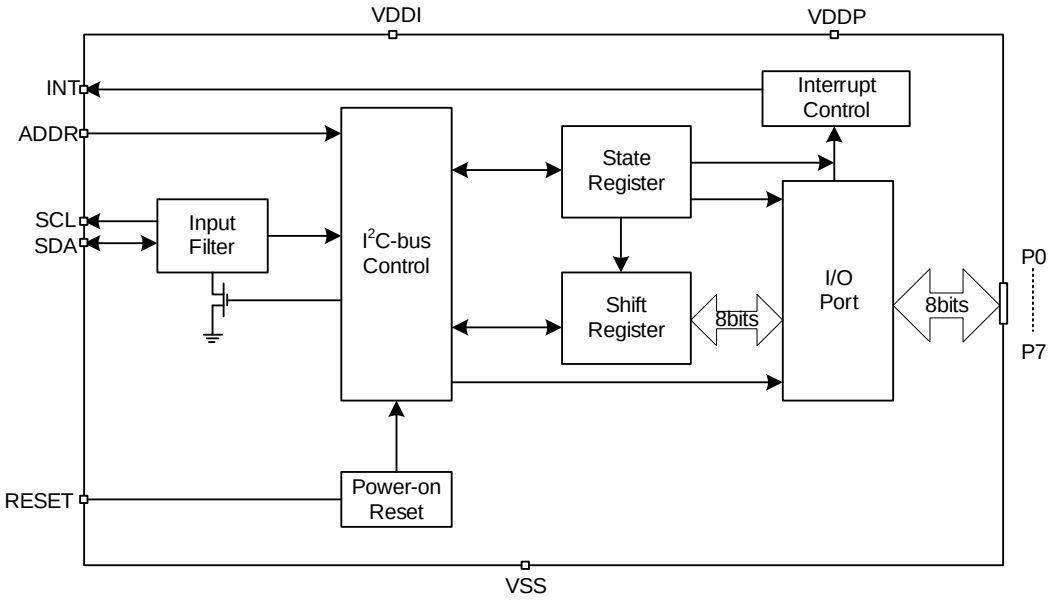


Figure 2. Block Diagram

Functions Description

Voltage Translation

V_{DDI} (SDA and SCL)	V_{DDP} (Port P)
1.8 V ~ 5.0V	1.8 V ~ 5.0V

Chip Address

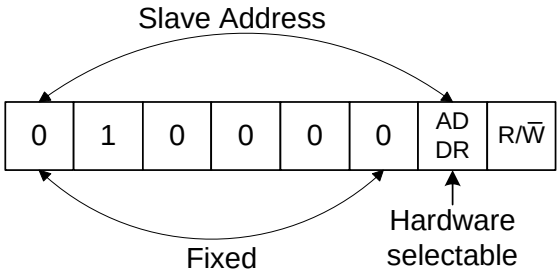


Figure 3. Chip address

ADDR is the hardware address package pin and is held to either HIGH (logic 1) or LOW (logic 0) to assign one of the two possible slave addresses. The last bit of the slave address (R/$\overline{W}$) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

Interface definition

Byte	Bit							
	7(MSB)	6	5	4	3	2	1	0(LSB)
I^2C-bus slave address	L	H	L	L	L	L	ADDR	R/W
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

Pointer register and Command byte

After the device address byte responds successfully, the bus controller sends a command byte, the pointer register, that can only write.

The command byte corresponds to the internal register that specifies the operation to be performed.When a new command byte is sent, the read instruction continues to access the last addressed register until the new command byte is written.

Register Map

Pointer Register Bits	Command byte	Register	Protocol	Default Value
0000 0000	00h	Input Register	Read only	xxxx xxxx
0000 0001	01h	Output Register	Read/Write	1111 1111
0000 0010	02h	Polarity inversion Register	Read/Write	0000 0000
0000 0011	03h	Configuration Register	Read/Write	1111 1111
0100 0000	40h	Output drive strength registers 0	Read/Write	1111 1111
0100 0001	41h	Output drive strength registers 1	Read/Write	1111 1111
0100 0010	42h	Input latched register	Read/Write	0000 0000
0100 0011	43h	Pull-up/Pull-down enable resistor	Read/Write	0000 0000
0100 0100	44h	Pull-up/Pull-down resistors type choice register	Read/Write	1111 1111
0100 0101	45h	Interrupt shielding register	Read/Write	1111 1111
0100 0110	46h	Interrupt status register	Read only	0000 0000
0100 1111	4Fh	Output state control register	Read/Write	0000 0000

Register descriptions

Register	Bit	7	6	5	4	3	2	1	0
00h	Symbol	I7	I6	I5	I4	I3	I2	I1	I0
	Default	X	X	X	X	X	X	X	X
01h	Symbol	O7	O6	O5	O4	O3	O2	O1	O0
	Default	1	1	1	1	1	1	1	1
02h	Symbol	N7	N6	N5	N4	N3	N2	N1	N0
	Default	0	0	0	0	0	0	0	0
03h	Symbol	C7	C6	C5	C4	C3	C2	C1	C0
	Default	1	1	1	1	1	1	1	1
40h	Symbol	CC3		CC2		CC1		CC0	
	Default	1	1	1	1	1	1	1	1
41h	Symbol	CC7		CC6		CC5		CC4	
	Default	1	1	1	1	1	1	1	1
42h	Symbol	L7	L6	L5	L4	L3	L2	L1	L0
	Default	0	0	0	0	0	0	0	0
43h	Symbol	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
	Default	0	0	0	0	0	0	0	0
44h	Symbol	PUD7	PUD6	PUD5	PUD4	PUD3	PUD2	PUD1	PUD0
	Default	1	1	1	1	1	1	1	1

Register descriptions(continued)

Register	Bit	7	6	5	4	3	2	1	0
45h	Symbol	M7	M6	M5	M4	M3	M2	M1	M0
	Default	1	1	1	1	1	1	1	1
46h	Symbol	S7	S6	S5	S4	S3	S2	S1	S0
	Default	0	0	0	0	0	0	0	0
4Fh	Symbol								ODEN
	Default	0	0	0	0	0	0	0	0

Input Registers(00h)

The Input registers (registers 0) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port registers are read only; writes to these registers have no effect.

The default value ‘X’ is determined by the externally applied logic level.

Note: Port P cannot be suspended when it is in the input state and is not configured to be pulled up or down.

Output Registers(01h)

The Output registers (registers 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, not the actual pin value.

Polarity Inversion Registers(02h)

The Polarity inversion registers (registers 2) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with ‘1’), the corresponding port pin’s polarity is inverted in the input register. If a bit in this register is cleared (written with a ‘0’), the corresponding port pin’s polarity is retained.

Configuration Registers(03h)

The Configuration registers (registers 3) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output.

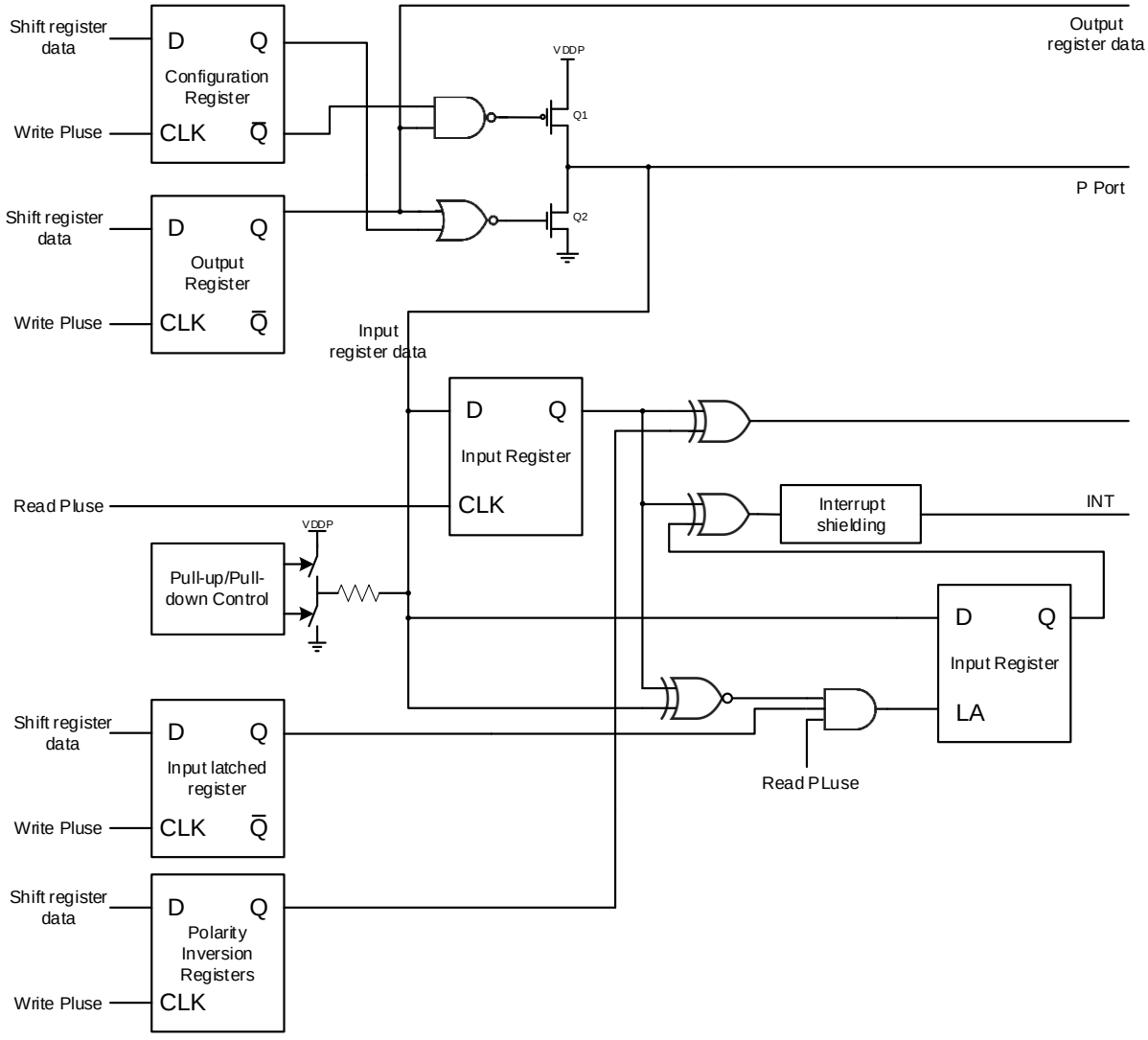


Figure 4. Logical function diagram

Output drive strength(40h,41h)

The output driver strength registers (registers 40 and 41) are used to configure the driving capacity of the GPIO port as the output. Each two bits corresponds to a P port, for example, CC7 corresponds to P7 port, CC6 corresponds to P6 port.The driver capability of data 00b/01b/10b is $\frac{1}{4}/\frac{1}{2}/\frac{3}{4}$ of the driver capability of data 11b.

Input latched register(42h)

Enter the latch register (register 42) and the GPIO port is valid in the input state.

When this register is configured as "0" :

If the state of the corresponding GPIO port on the input port changes, the $\overline{INT}$ port generates an interrupt signal.When the input register data is read, the interrupt signal is cleared.Or when the state of the port is

restored, the interrupt signal is cleared.

When this register is set to "1" :

The state of the corresponding GPIO port on the input port changes horizontally, then the $\overline{INT}$ port generates an interrupt signal.Only by reading the input register data, the interrupt signal can be cleared;And when the input register signal is not read, even if the port state is restored, the input register data is unchanged, and the interrupt is not cleared.

Pull-up/Pull-down enable resistor(43h)

The Pull-up/Pull-down enable resistor (register 43) is used to configure the Pull-up/Pull-down resistors function of the corresponding GPIO port (Pull-up/Pull-down resistors can be selected by Pull-up/Pull-down resistors type choice register).When the register is set to 0, the GPIO port does not have the Pull-up/Pull-down resistors function.When the register is set to 1, the GPIO port has the Pull-up/Pull-down resistors function.When the GPIO port is configured with open miss output, the Pull-up/Pull-down enable function is turned off.

Pull-up/Pull-down resistors type choice register(44h)

When the Pull-up/Pull-down enable register (register 43) is configured, the Pull-up/Pull-down select register (register 44) is configured to select the pull-up or pull-down function of the GPIO port.If the value is 1, the pull-up resistance is configured.If this parameter is set to 0, the pull-down resistance is configured.The typical resistance is 100KΩ.

Interrupt shielding register(45h)

The interrupt masking register (register 45) is used to mask the interrupt response function of the GPIO port.When the value is set to 0, the state of the corresponding port changes when it enters the state, and the $\overline{INT}$ port generates an interrupt signal.When the value is set to 1, the status of the corresponding port changes when it enters the status, and the $\overline{INT}$ port does not generate interrupt signals.

Interrupt status register(46h)

The interrupt status register is a read-only register. If a bit "1" is read, the port corresponding to the bit is the interrupt source. If the bit "0" is read, the port is not the interrupt source.

If the interrupt masking register is configured as "1", the corresponding bit data is read as "0".

Output state control register(4Fh)

Bit 0 of the output state configuration register (register 4F) is used to configure the port structure of the GPIO port in the output state:

This bit is "0", and THE GPIO output is push-pull structure (Q1 and Q2 in the structure block diagram are effective at output high level and low level respectively).When the bit is "1", the GPIO port in the output state is an open leakage structure, Q1 in the structure block diagram is always in the cut-off state, and Q2 is effective at low output current, while Q2 is cut-off at high output current.

I/O port

When an I/O is configured as an input port, MOS tubes Q1 and Q2 are turned off as a high-impedance input port.

When an I/O is configured as an output port, mostube Q1 or Q2 is turned on, depending on the state of the output register.In this case, there is a low impedance path between the I/O pin and the VDDP or VSS.

In addition, the GPIO port can be configured to have pull-up or pull-down resistors when it is in a non-open leakage output state (i.e. input or push-pull output).The output state can also be configured as an open leakage output structure.

Power-on reset

When the power supply (from 0V) is added to the VDDP and rises to VPOR, the internal power reset circuit keeps the chip in the reset state.When the power supply is higher than VPOR, the reset state is released, and the registers of ET6408 and the state machine of I²C-bus /SM bus are initialized to the default state.After that, the VDDP must drop below VPOR and return to the operating voltage for a new reset.

Reset input

In the VDDP operating voltage range, the $\overline{\text{RESET}}$ input can be used to initialize the system.You can $\overline{\text{RESET}}$ the $\overline{\text{RESET}}$ port by lowering the hold time TWRST.Once $\overline{\text{RESET}}$ is pulled low, the registers of ET6408 and the state machine of I²C-bus/SM bus are initialized to the default state.If $\overline{\text{RESET}}$ does not use an active connection, the input needs to be connected to a pull-up resistor to the VDDI.

Interrupt output ($\overline{\text{INT}}$)

After the interrupt masking register is configured, the bit corresponding to the GPIO port is set to 0. The port can activate the interrupt function only when it is in the input state.

Interrupts are generated by any rising or falling edge of the GPIO port input in input mode.After time t_{vINT}, $\overline{\text{INT}}$ signal is valid.The interrupt is reset when the data on the port changes to the original value or when the input register data corresponding to the port is read.In read mode, the $\overline{\text{INT}}$ output is reset for the ACK or NACK bit after the rising edge of the SCL.Because of the reset interrupt during this pulse, interrupts that occur during an ACK or NACK clock pulse may be lost (or very short).After a reset, any changes to the I/O port are detected and an $\overline{\text{INT}}$ interrupt is generated.

Pins configured for output do not generate interrupts.Changing I/O from output to input may cause false interrupts if the state of the pin does not match the contents of the input register.

$\overline{\text{INT}}$ is an open leakage output structure, connected to VDDP or VDDI by a pull-up resistor, depending on the application.The voltage source that needs to connect $\overline{\text{INT}}$ to the device that needs interrupt information.

In addition, the condition for interrupt reset can be changed by configuring the input latch register.

Bus protocol

ET6408 is an I²C-bus slave device.Data is exchanged between master and slave devices through read and write instructions of I2C-bus.The two communication lines are serial data line (SDA) and serial clock line (SCL).When connected to the output stage of the device, both lines must be connected to the power supply through a pull-up resistor.Data transfer can only be started when the bus is idle.

Write command

Data is transmitted to ET6408 by sending the device address and setting the least significant bit (LSB) to a logical 0.The command byte is sent after the device address to determine which register receives the data after the command byte.

The four sets of registers in ET6408 are: input register, output register, polarity reversal register and configuration register.After sending a data byte to one register, the next data byte is sent to another register in the pair.

There is no limit to the number of bytes of data that can be sent during a write transfer.In this way, the host can continuously update the register pair independently of the other registers.

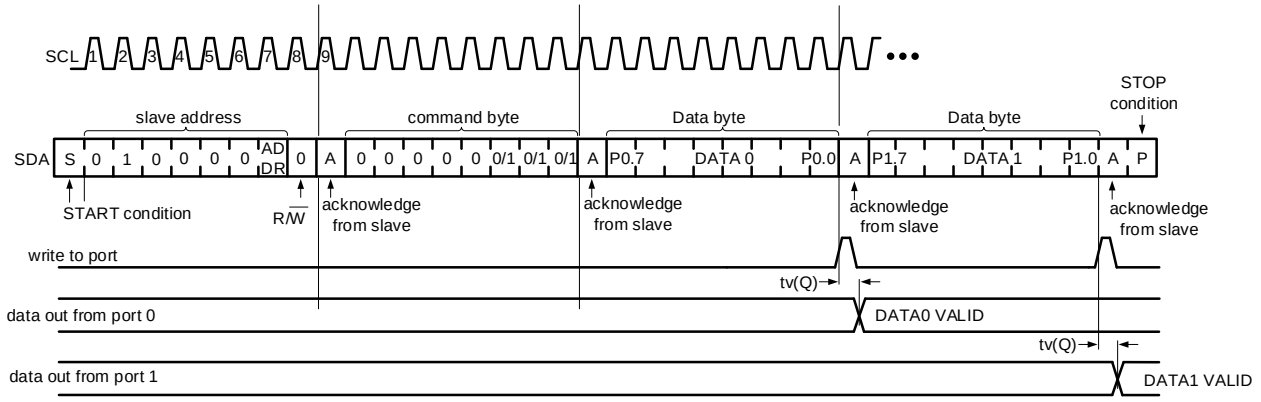


Figure 5. Write Commands

Read command

Data can be read from ET6408 by sending the device address and setting the least significant bit (LSB) to logical 1.The command byte is sent after the device address to determine which register to read.

Data in registers defined by command bytes is sent by ET6408.After the first byte is read, other bytes may be read, but it must be information in another register in the pair.

There is no limit to the number of bytes of data that can be read during a read transfer, but the master bus must be unresponsive after receiving the last byte of data.

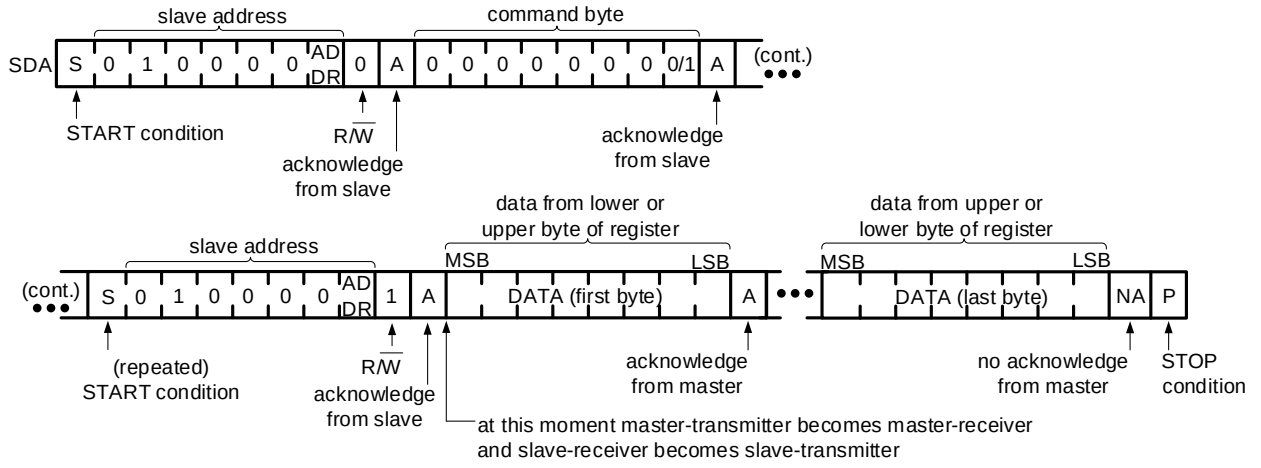


Figure 6. Read Commands

Absolute Maximum Ratings

Exceeding the values listed in the limit parameter table may damage the device.If any of these limits are exceeded, damage may occur and affect reliability.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDI}	I^2C-bus Supply Voltage		-0.5	+6.5	V
V_{DDP}	Supply Voltage Port P		-0.5	+6.5	V
V_I	Input Voltage		-0.5	+6.5	V
V_O	Output Voltage		-0.5	+6.5	V
I_{IK}	Input Clamping Current	ADDR, $\overline{RESET}$, SCL; V_I < 0V	-	-20	mA
I_{OK}	Output Clamping Current	$\overline{INT}$; V_O < 0V	-	-20	mA
I_{IOK}	Input/output Clamping Current	P port; V_O < 0V or V_O > V_{DDP}	-	±20	mA
		SDA; V_O < 0V or V_O > V_{DDI}	-	±20	mA
I_{OL}	LOW-level Output Current	P port; V_O = 0V to V_{DDP}	-	50	mA
		SDA, $\overline{INT}$; V_O = 0V to V_{DDI}	-	25	mA
I_{OH}	HIGH-level Output Current	P port; V_O = 0V to V_{DDP}	-	25	mA
I_{DD}	Supply Current	through V_{SS}	-	200	mA
I_{DDP}	Supply Current Port P	through V_{DDP}	-	160	mA
I_{DDI}	I2C-bus Supply Current	through V_{DDI}	-	10	mA
T_{STG}	Storage Temperature		-65	+150	°C
T_{JMAX}	Maximum Junction Temperature		-	150	°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDI}	I^2C-bus Supply Voltage		1.65	5.5	V
V_{DDP}	Supply Voltage Port P		1.65	5.5	V
V_{IH}	HIGH-level Input Voltage	SCL, SDA（V_{DDI}=1.8V）	0.96	5.5	V
		SCL, SDA（V_{DDI}≥2.5V）	1.2	5.5	V
		$\overline{RESET}$	0.7*V_{DDI}	5.5	V
		ADDR, P7 to P0	0.7*V_{DDP}	5.5	V
V_{IL}	LOW-level Input Voltage	SCL, SDA	-0.5	0.36	V
		$\overline{RESET}$	-0.5	0.3*V_{DDI}	V
		ADDR, P7 to P0	-0.5	0.3*V_{DDP}	V
I_{OH}	HIGH-level Output Current	P7 to P0	-	10	mA
I_{OL}	LOW-level Output Current	P7 to P0	-	23	mA
T_A	Ambient Temperature	Operating in free air	-40	+85	°C

Electrical Characteristics

D.C. Characteristics

T_A = 25°C;V_{DDI} = 1.65V to 5.5V; (Unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IK}	Input Clamping Voltage	I_I = -18mA	-1.2	-	-	V
V_{POR}	Power-on Reset Voltage	V_I = V_{DDP} or V_{SS}; I_O = 0mA; T_A=25°C	-	-	1.55	V
V_{OH}	HIGH-level Output Voltage	P port; I_{OH} = 8mA or 10mA,CCX = 11b				
		I_{OH} = -8mA; V_{DDP} = 1.65V	1.2	-	-	V
		I_{OH} = -10mA; V_{DDP} = 1.65V	1.1	-	-	V
		I_{OH} = -8mA; V_{DDP} = 2.3V	1.8	-	-	V
		I_{OH} = -10mA; V_{DDP} = 2.3V	1.7	-	-	V
		I_{OH} = -8mA; V_{DDP} = 3.0V	2.6	-	-	V
		I_{OH} = -10mA; V_{DDP} = 3.0V	2.5	-	-	V
		I_{OH} = -8mA; V_{DDP} = 4.5V	4.1	-	-	V
		I_{OH} = -10mA; V_{DDP} = 4.5V	4.0	-	-	V
V_{OL}	LOW-level Output Voltage	P port; I_{OL} = 8mA,CCX = 11b				
		V_{DDP} = 1.65V	-	-	0.45	V
		V_{DDP} = 2.3V	-	-	0.25	V
		V_{DDP} = 3.0V	-	-	0.25	V
		V_{DDP} = 4.5V	-	-	0.2	V
I_{OL}	LOW-level Output Current	V_{OL} = 0.4V; V_{DDP} = 1.65V to 5.5V				
		SDA	3	-	-	mA
		$\overline{INT}$	3	15	-	mA
		P port				
		V_{OL} = 0.5V; V_{DDP} = 1.65V	8	10	-	mA
		V_{OL} = 0.7V; V_{DDP} = 1.65V	10	13	-	mA
		V_{OL} = 0.5V; V_{DDP} = 2.3V	8	10	-	mA
		V_{OL} = 0.7V; V_{DDP} = 2.3V	10	13	-	mA
		V_{OL} = 0.5V; V_{DDP} = 3.0V	8	14	-	mA
		V_{OL} = 0.7V; V_{DDP} = 3.0V	10	19	-	mA
		V_{OL} = 0.5V; V_{DDP} = 4.5V	8	17	-	mA
		V_{OL} = 0.7V; V_{DDP} = 4.5V	10	24	-	mA

D.C. Characteristics (continued)

T_A = 25°C;V_{DDI} = 1.65V to 5.5V; (Unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input Current	V_{DDP} = 1.65V to 5.5V				
		SCL, SDA, $\overline{RESET}$; V_I = V_{DDI} or V_{SS}	-	-	±1	uA
		ADDR; VI = V_{DDP} or V_{SS}	-	-	±1	uA
I_{IH}	HIGH-level Input Current	P port; V_I=V_{DDP}; V_{DDP}=1.65V to 5.5V	-	-	1	uA
I_{IL}	LOW-level Input Current	P port; V_I =VSS; V_{DDP} =1.65V to 5.5V	-	-	1	uA
I_{DD}	Supply Current	IDDI + IDDP; SDA, P port, ADDR, $\overline{RESET}$; V_I on SDA and RESET = V_{DDI} or V_{SS}; V_I on P port and ADDR = V_{DDP}; I_O = 0mA; I/O = inputs; F_{SCL} = 400kHz				
		V_{DDP} = 3.6V to 5.5V	-	10	25	uA
		V_{DDP} = 2.3V to 3.6V	-	6.5	15	uA
		V_{DDP} = 1.65V to 2.3V	-	4	9	uA
		I_{DDI} + I_{DDP}; SCL, SDA, P port, ADDR, $\overline{RESET}$; V_I on SCL, SDA and $\overline{RESET}$ = V_{DDI} or V_{SS}; V_I on P port and ADDR = VDDP; I_O = 0mA; I/O = inputs; F_{SCL} = 0kHz				
		V_{DDP} = 3.6V to 5.5V	-	1.5	7	uA
		V_{DDP} = 2.3V to 3.6V	-	1	3.2	uA
		V_{DDP} = 1.65V to 2.3V	-	0.5	1.7	uA
		Active mode;I_{DDI} + I_{DDP}; P port, ADDR, $\overline{RESET}$; V_I on $\overline{RESET}$ = V_{DDI}; V_I on P port and ADDR = V_{DDP}; I_O = 0mA; I/O = inputs; F_{SCL} = 400kHz, continuous register read				
		V_{DDP} = 3.6V to 5.5V	-	60	125	uA
		V_{DDP} = 2.3V to 3.6V	-	40	75	uA
		V_{DDP} = 1.65V to 2.3V	-	20	45	uA

D. C. Characteristics (continued)

T_A = 25°C;V_{DDI} = 1.65V to 5.5V; (Unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔI_{DD}	Additional Quiescent Supply Current	SCL, SDA, $\overline{RESET}$; one input at V_{DDI} - 0.6V, other inputs at V_{DDI} or V_{SS}; V_{DDP} = 1.65V to 5.5V	-	-	25	uA
ΔI_{DD}	Additional Quiescent Supply Current	P port, ADDR; one input at V_{DDP} - 0.6V, other inputs at V_{DDP} or V_{SS}; V_{DDP} = 1.65V to 5.5V	-	-	80	uA
C_i	Input Capacitance	V_I = V_{DDI} or V_{SS} ; V_{DDP} = 1.65V to 5.5V	-	4.2	7	pF
C_{io}	Input/output Capacitance	V_{IO} = V_{DDI} or V_{SS} ; V_{DDP} = 1.65V to 5.5V	-	4.5	8	pF
		V_{IO} = V_{DDP} or V_{SS} ; V_{DDP} = 1.65V to 5.5V	-	4.5	8.5	pF

A.C. Characteristics

T_A = 25°C;VDDI = 1.65V to 5.5V; (Unless otherwise specified.)

Symbol	Parameter	Conditions	Standard-mode I^2C-bus		Fast-mode I^2C-bus		Unit
			Min	Max	Min	Max	kHz
f_{SCL}	SCL clock frequency		0	100	0	400	us
t_{HIGH}	HIGH period of the SCL clock		4	-	0.6	-	us
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	us
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		0	50	0	50	ns
$t_{SU;DAT}$	Data set-up time		250	-	100	-	ns
$t_{HD;DAT}$	Data hold time		0	-	0	-	ns
t_r	Rise time of both SDA and SCL signals		-	1000	-	300	ns

A. C. Characteristics(continued)

T_A = 25°C;VDDI = 1.65V to 5.5V; (Unless otherwise specified.)

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	kHz
t_f	Gall time of both SDA and SCL signals			300	-	300	ns
t_{BUF}	Bus free time between a STOP and START condition		4.7	-	1.3	-	us
$t_{SU;STA}$	Set-up time for a repeated START condition		4.7	-	0.6	-	us
$t_{HD;STA}$	Hold time (repeated) START condition		4	-	0.6	-	us
$t_{SU;STO}$	Set-up time for STOP condition		4	-	0.6	-	us
$t_{VD;DAT}$	Data valid time	SCL LOW to SDA output valid	-	3.45	-	0.9	us
$t_{VD;ACK}$	Data valid acknowledge time	ACK signal from SCL LOW to SDA (out) LOW	-	3.45	-	0.9	us
t_{wrst}	Reset pulse width		30	-	30	-	ns
t_{recrst}	Reset recovery time		200	-	200	-	ns
t_{rst}	Reset time		600	-	600	-	ns
t_{vINT}	Valid time on pin $\overline{INT}$	from P port to $\overline{INT}$	-	1	-	1	us
t_{rstINT}	Reset time on pin $\overline{INT}$	from SCL to $\overline{INT}$	-	1	-	1	us
t_{vQ}	Data output valid time	from SCL to P port	-	400	-	400	ns
t_{suD}	Data input set-up time	from P port to SCL	0	-	0	-	ns
t_{hD}	Data input hold time	from P port to SCL	300	-	300	-	ns

Load Configuration

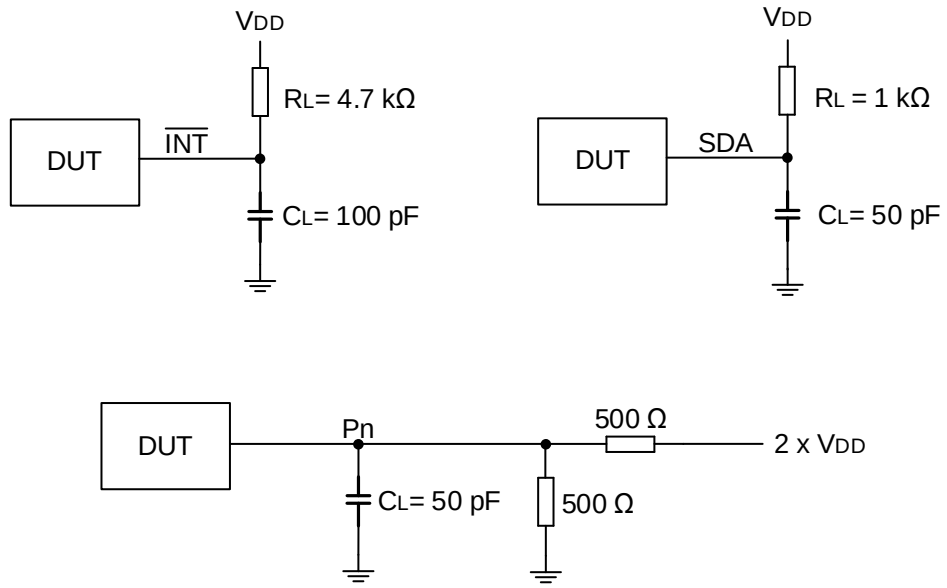


Figure7. $\overline{INT}$、SDA、Port P load configuration

***Note*:** C_L includes probe and clamp capacitance.

I²C Timing Waveform

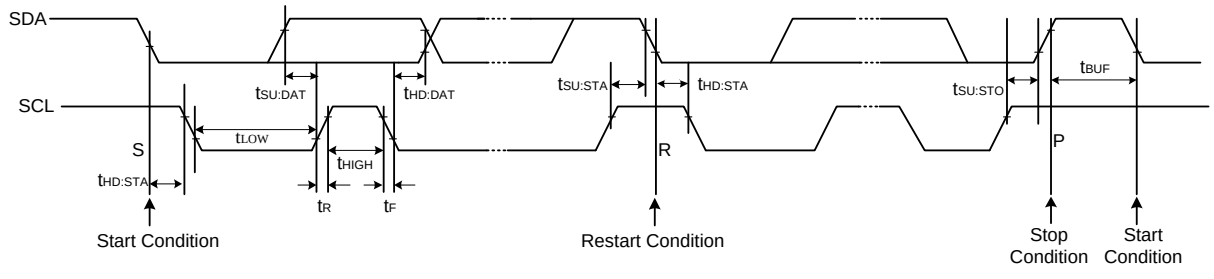


Figure 8. SDA Waveform

I²C Timing Waveform (Continued)

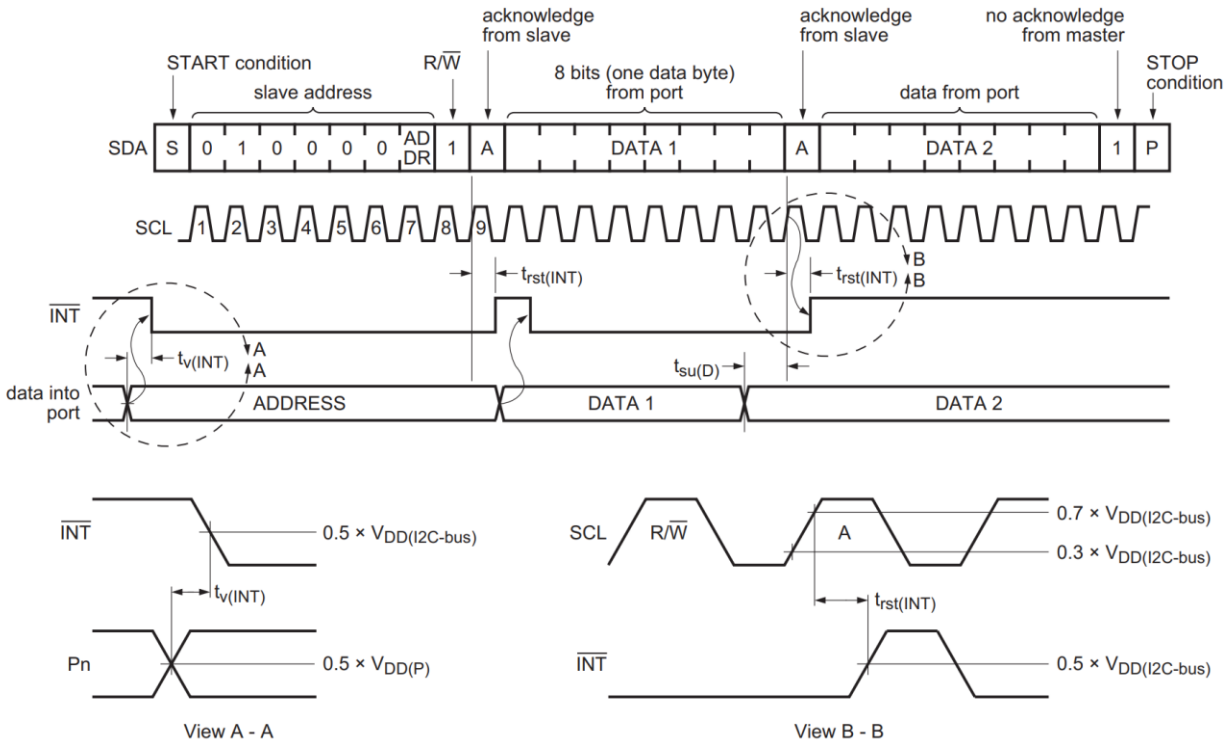


Figure 9. $\overline{INT}$、SDA、Port P Waveform

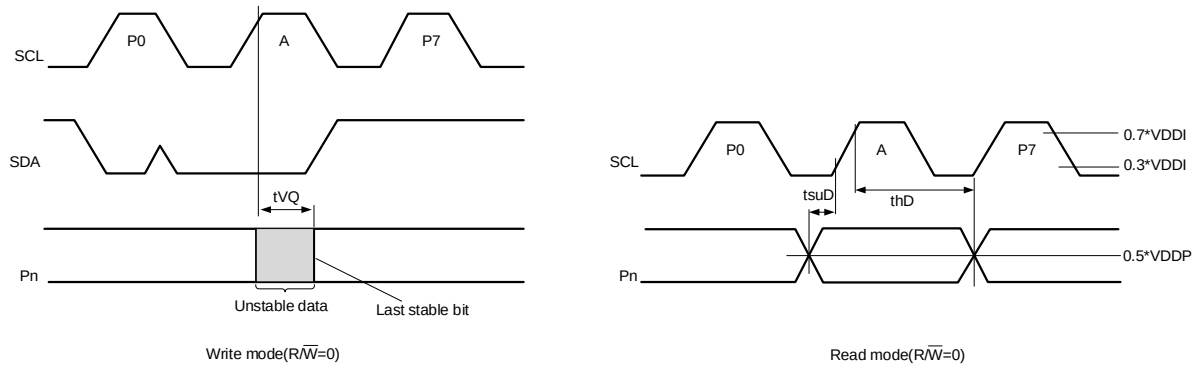


Figure 10. SDA Read/Write Mode Waveform

I²C Timing Waveform (Continued)

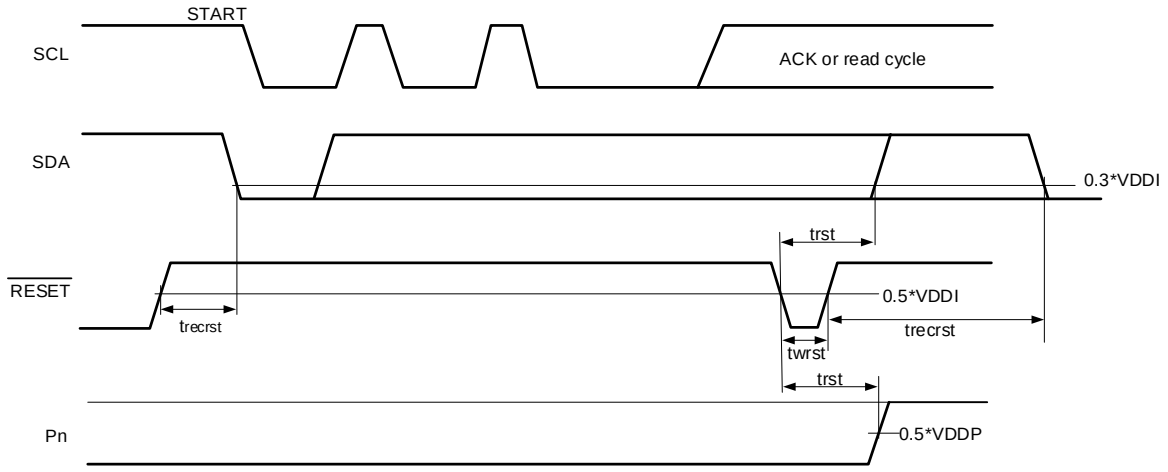


Figure 11. $\overline{\text{RESET}}$ waveform

Application Circuits

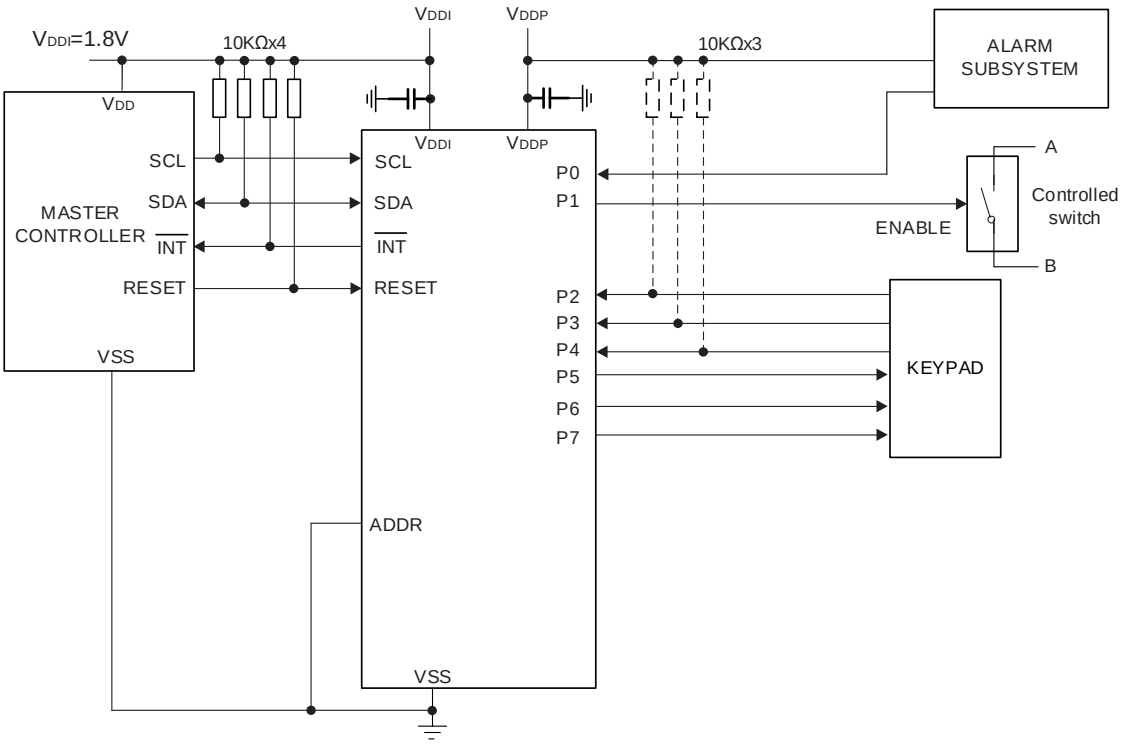


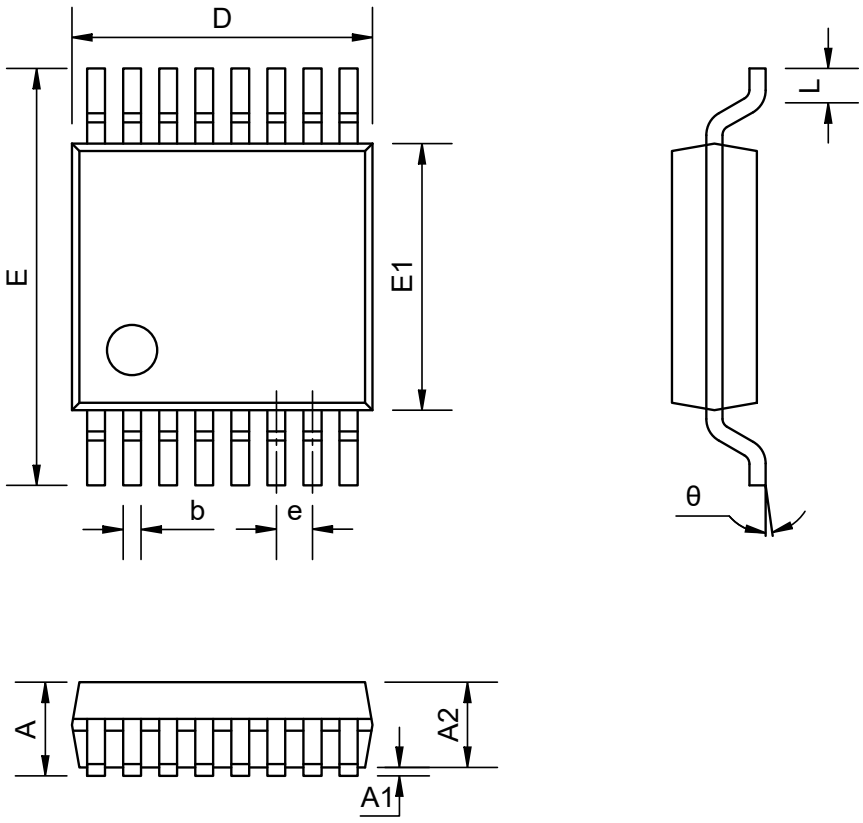
Figure 12. Application circuit (*)

***Note*：** * This application circuits is for reference only.

* When the P port is suspended, configure it to the output state please.

Package

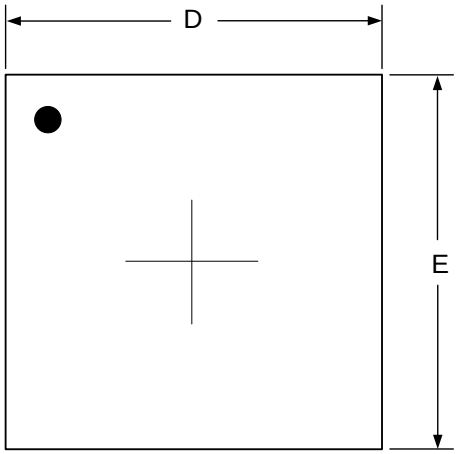
TSSOP16 (ET6408V)



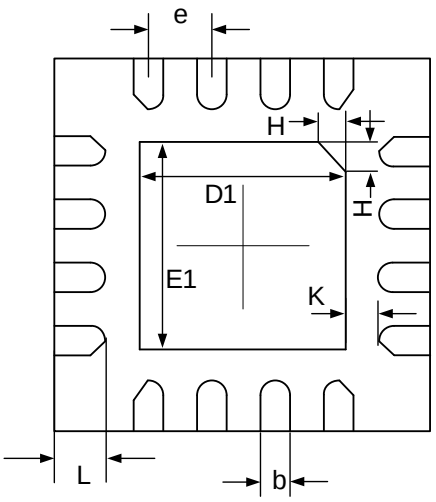
Dimensions Table (Units:mm)

Symbol	Min	Non	Max
A	--	--	1.20
A1	0.05	--	0.15
A2	0.90	--	1.05
b	0.20	--	0.28
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
θ	0°	--	8°

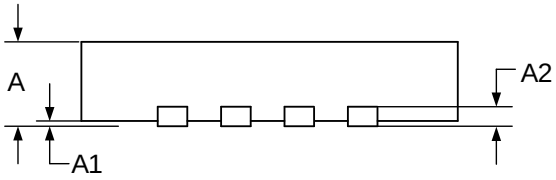
QFN16 (ET6408Y)



TOP VIEW



BOTTOM VIEW

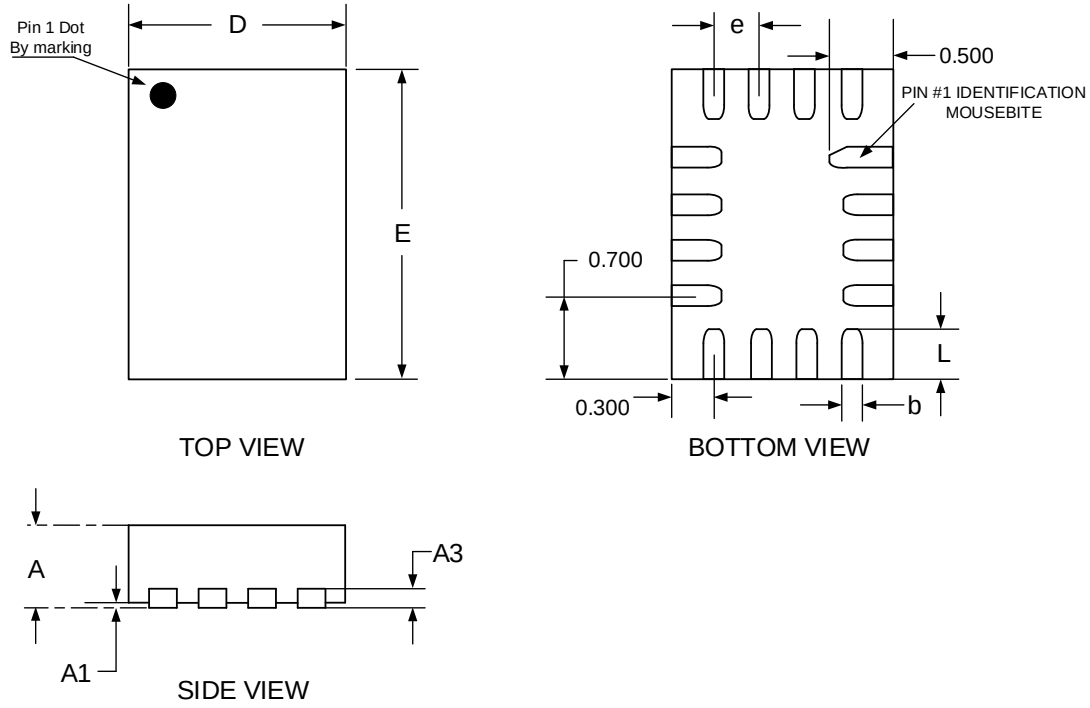


SIDE VIEW

Dimensions Table (Units:mm)

Symbol	Min	Non	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.20REF	
b	0.20	0.25	0.30
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.60	1.70	1.75
E1	1.60	1.70	1.75
e	0.40	0.50	0.60
H		0.30REF	
K	0.15	-	-
L	0.35	0.40	0.45

QFN16L (ET6408Y1)

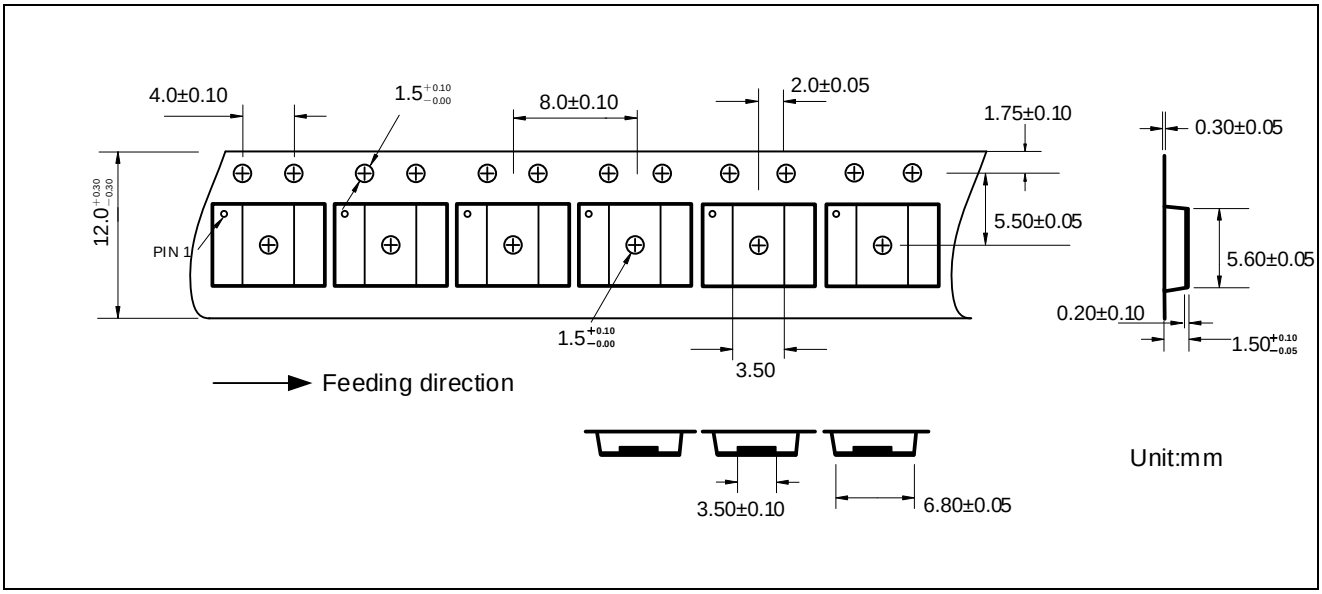


Dimensions Table (Units: mm)

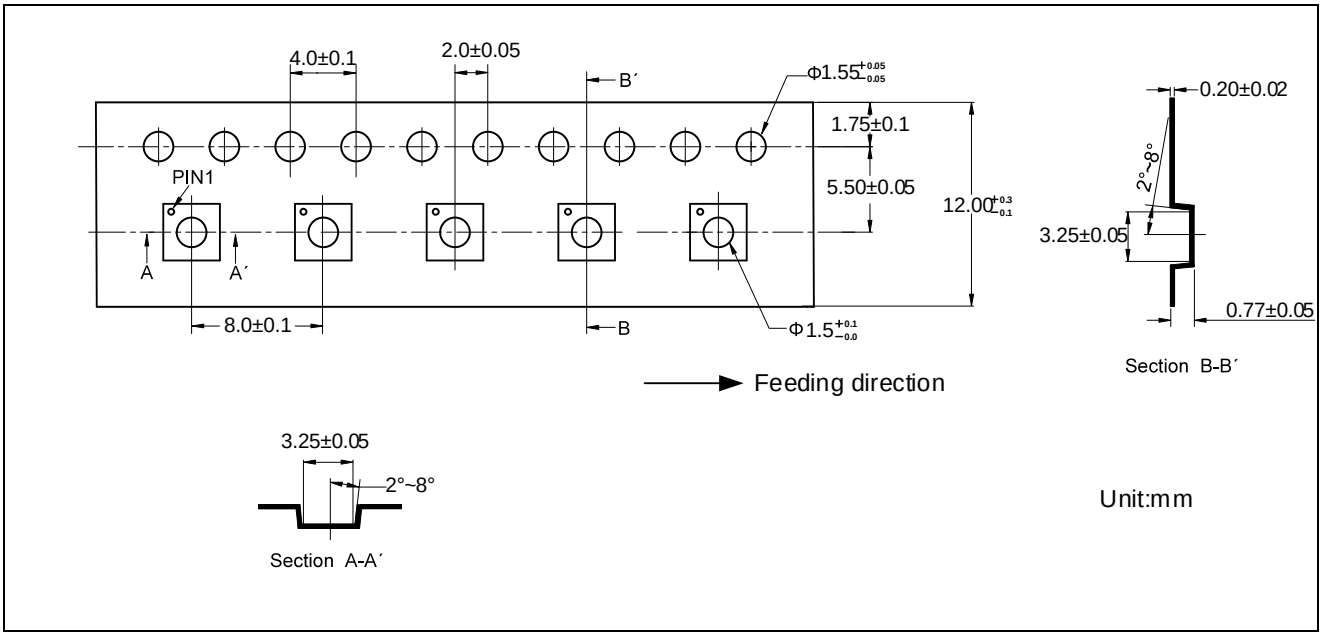
SYMBOL	MIN	NOM	MAX
A	>0.50	0.55	0.60
A1	0.00	-	0.05
A3	0.15REF		
D	1.75	1.80	1.85
E	2.55	2.60	2.65
L	0.30	0.40	0.50
b	0.15	0.20	0.25
e	0.40BSC		

Tape Information

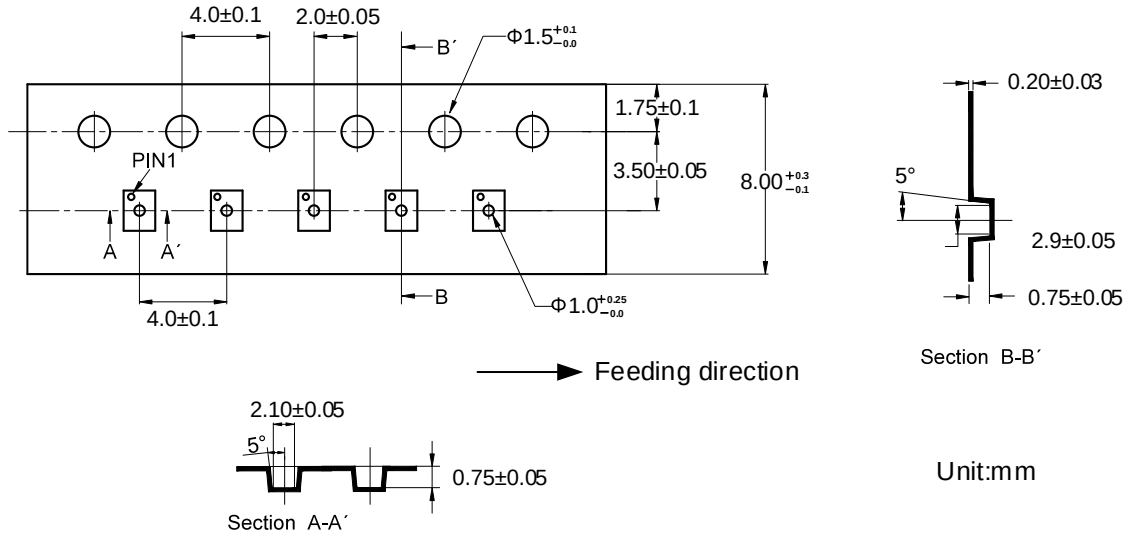
TSSOP16



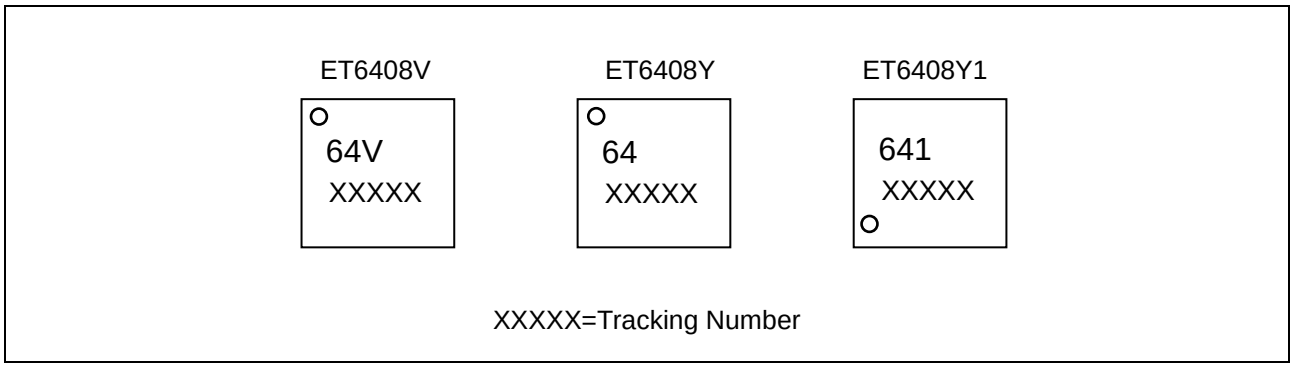
QFN16



QFN16L



Marking



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2022-02-17	Preliminary Version	Shilj	Shilj	Liujy
1.0	2022-08-12	Offered Version	Zhuzq Shibo	Shilj	Zhujl
1.1	2026-07-07	Add QFN16L package	Tianqh	Geh	Liujy
1.2	2026-07-23	Update V_{OH},V_{OL} test condition	Tianqh	Geh	Liujy
1.3	2026-09-15	Add Packing,MSL,Marking,Tape	Tianqh	Geh	Liujy