ET80101 - Low Iq Buck-Boost Converter

General Description

The ET80101 is high efficiency and Low Iq buck-boost converters. Depending on the input voltage, they automatically operate in boost, buck or in a novel buck-boost mode when the input voltage is approximately equal to the output voltage.The transitions between modes happen at defined thresholds and avoid unwanted toggling within the modes to reduce output voltage ripple.

The ET80101 can be controlled by an I²C compatible interface that supports High-speed Plus mode(1MHz). These features include: Output voltage programmed, Auto PFM or FPWM mode select, Software startup or shutdown, State Flag,PG function, etc. The output voltage is also controlled by an external VSEL pin. The output voltage default to 3.5V when VSEL pin is logic high, and it default to 3.3V when VSEL pin is logic low.

The ET80101 is available in small WLCSP9 (1.28×1.28-0.4mm Pitch) Package .

Features

- Input voltage range: 2.2V to 5.0V
- Output voltage range:
  - Default 3.5V when VSEL=H, default 3.3V when VSEL=L
  - Programmed by I²C, range is 2.025V to 5.2V, 25mV per step
- Address select by VSEL
  - 7bit address=1110101,VSEL=H
  - 7bit address=1110110,VSEL=L
- High efficiency over entire load range
- Less than 5μA operating quiescent current
- Automatic PFM and FPWM mode
- Defined transitions between buck, buck-boost and boost operation
- Forward and reverse current operation
- Safety and robust operation features
- Integrated soft start
- Over-temperature,Short,current limit protection
- Forward and backward current limit
- True load disconnect during shutdown
- I²C interface supporting 1 MHz rate

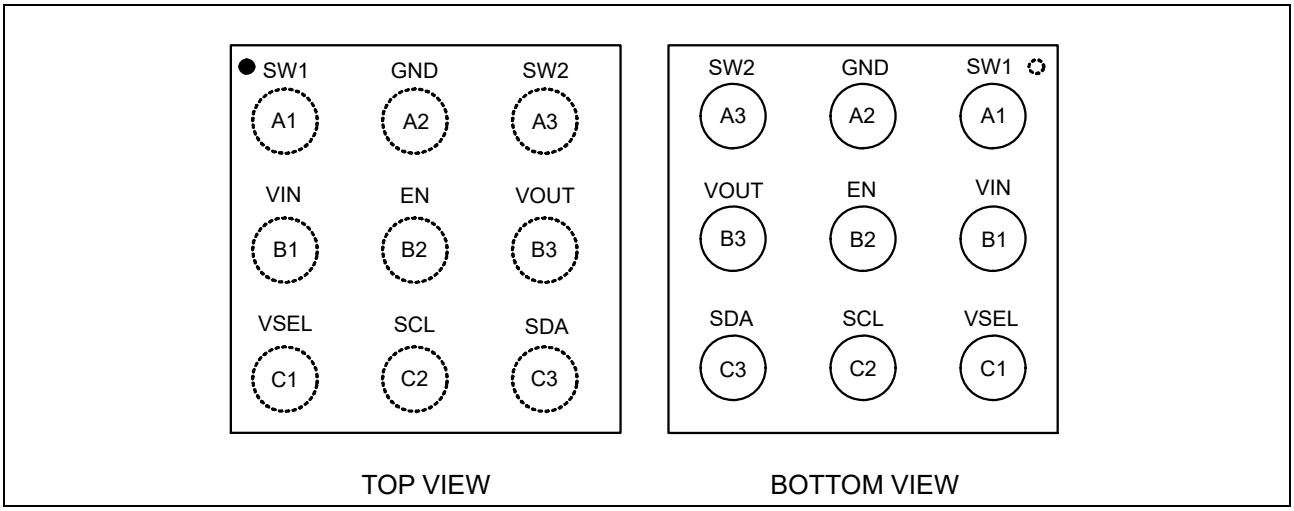
Device Information

Part No.	Package	MSL
ET80101	WLCSP9(1.28×1.28-0.4mm Pitch)	1

Applications

- Voltage stabilizer (datacom, optical modules, cooling/heating)
- System pre-regulator (smartphone, tablet, terminal, telematics)
- Point-of-load regulation (wired sensor, port/cable adapter, and dongle)
- Fingerprint, camera sensors (electronic smart lock, IP network camera)

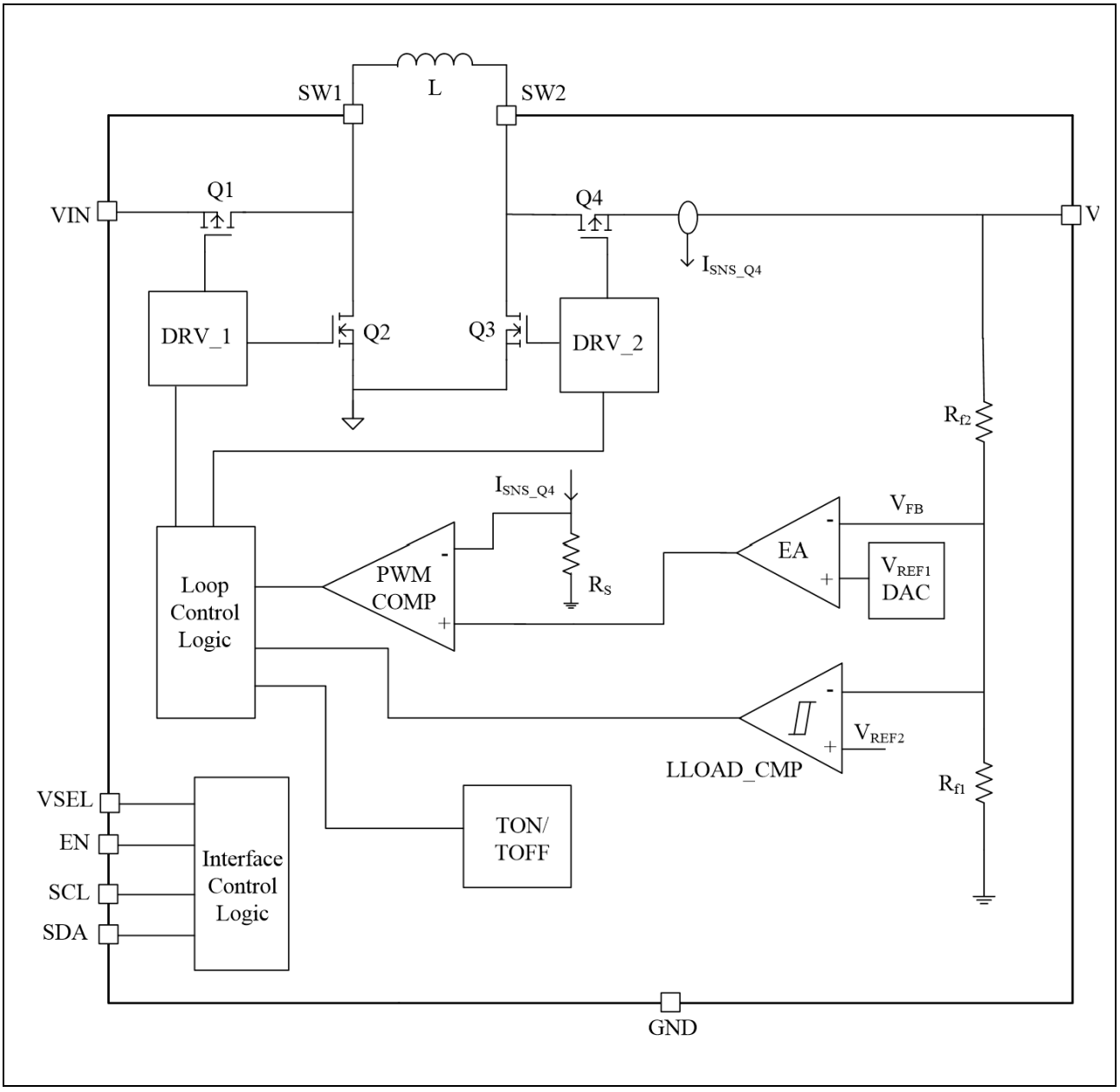
Pin Configuration



Pin Function

Pin No.	Pin Name	I/O	Description
A1	SW1	-	Converter switch pin1, connect to inductor.
A2	GND	-	Power ground.
A3	SW2	-	Converter switch pin2, connect to inductor.
B1	VIN	-	Input Power supply.
B2	EN	I	Enable. When this pin is high, the circuit is enabled.
B3	VOUT	-	Output voltage pin.
C1	VSEL	I	Output voltage and I^2C address selection pin.When VSEL=H,output voltage default to 3.5V and 7bit address=1110101.When VSEL=L,output voltage default to 3.3V and 7bit address=1110110.
C2	SCL	I	I^2C Serial Clock.
C3	SDA	I/O	I^2C Serial Data.

Block Diagram



Functional Description

The ET80101 is high-efficiency buck-boost converters. Each device uses four switches to maintain synchronous power conversion under all operating conditions, so that the device achieves high efficiency power conversion over a wide range of input voltages and output currents. The device automatically switches between buck, boost, and buck-boost operation as required by the operating conditions. The device operates as a true buck converter when $V_{IN} > V_{OUT}$ and as a true boost converter when $V_{IN} < V_{OUT}$. When $V_{IN} \approx V_{OUT}$, the device operates in a 3-cycle buck-boost mode. The RMS current through the switches and the inductor is thus kept to a minimum, minimizing switching and conduction losses. Controlling the switches this way lets the converter achieve high efficiency over the whole input voltage range.

Control Scheme

The device automatically selects the best switching scheme for the operating conditions. To make sure of stable operation, the selection logic includes hysteresis (see Figure 1)

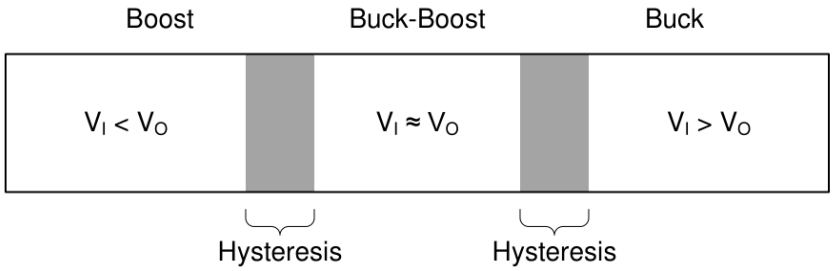


Figure 1. Switching Scheme Selection

Buck Operation

When $V_I > V_O$, the device switches like a buck converter:

Q1 is the switch.

Q2 is the rectifier.

Q3 is permanently off.

Q4 is permanently on.

See Figure 2. During buck operation, one switching cycle comprises two phases: on–off.

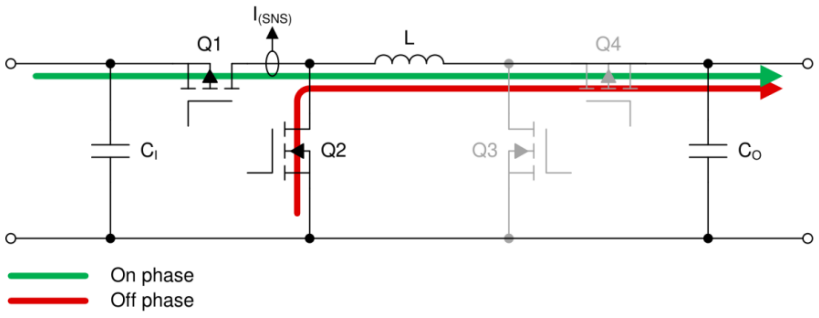


Figure 2. Buck Switch Configuration

Boost Operation

When $V_I < V_O$, the device switches like a boost converter:

Q1 is permanently on.

Q2 is permanently off.

Q3 is the switch.

Q4 is the rectifier

See Figure 3. During boost operation, one switching cycle comprises two phases: on–off.

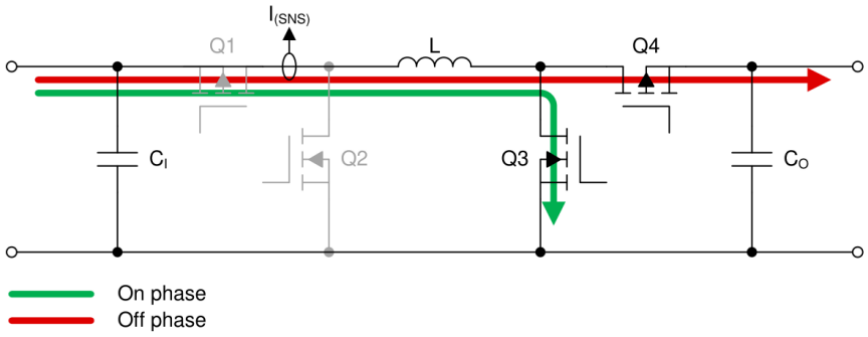


Figure 3. Boost Switch Configuration

Buck-Boost Operation

When $V_I \approx V_O$, all four transistors switch continuously (see Figure 4). During buck-boost operation, one switching cycle comprises three phases.

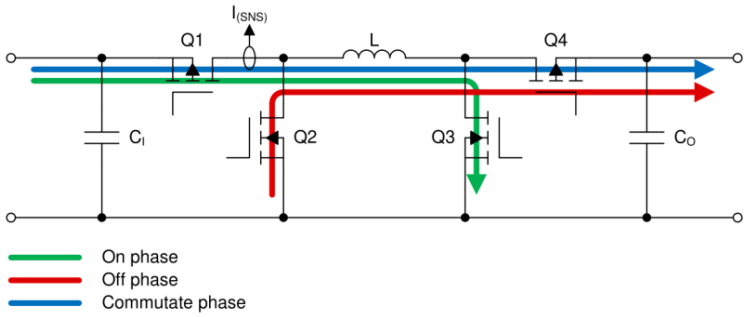


Figure 4. Buck-Boost Switch Configuration

Control Scheme

The device uses quasi fixed frequency, valley-current-mode control scheme where an outer voltage control loop generates the demand signal for an inner current control loop. When one cycle starts, the converter begins to store energy in the conductor. When the on time ends, the off phase begin. During the off state, the current of inductor decreases. When the inductor current equals the demand signal from the error amplifier, the off phase will be ended, and it begins the next cycle.

During PWM operation, current can flow in the reverse direction (from output to input). In this case, the error amplifier provides a negative valley current target. So the average current of input is close to zero.

Power-Save Mode Operation (PSM)

To increase efficiency across a wide range of operating conditions, the device automatically changes from pulse- width modulation (PWM) at medium and high output currents to pulse-frequency modulation (PFM) at low output currents.

During PWM operation, the device switches continuously and adjusts the duty cycle of each switching cycle to regulate the output voltage.

During PFM operation, the device switches in bursts of a few switching cycles, separated by periods when the device does not switch. PFM operation increases efficiency at low output currents because when the device does not switch, there are no switching losses and most of the internal circuitry is disabled, which reduces quiescent power consumption. A comparator with hysteresis compares the output voltage of the error amplifier to a predefined PFM threshold voltage. When the output voltage of the error amplifier is greater than the burst threshold voltage, the device starts switching. When the output voltage of the error amplifier is less than the burst threshold voltage, the device stops switching. This scheme automatically adjusts the frequency and the duration of the switching bursts to regulate the output voltage. During PFM operation, the output voltage ripple can be higher and the transient response is not as good as during PWM operation (see Table 1).

To enable power-save mode, clear the FPWM bit in the Control register to 0.

Table 1. Forced-PWM versus Power-Save Mode Performance Comparison

PERFORMANCE PARAMETER	BEST OPERATING MODE
Low-power efficiency	Power-Save Mode (PSM)
Medium- and high-power efficiency	No difference
DC Output voltage accuracy	Forced-PWM
Transient response	Forced-PWM
Output voltage ripple	Forced-PWM

Forced-PWM Operation (FPWM)

During Forced-PWM operation, the device uses PWM for all operating conditions. Forced-PWM operation has lower output voltage ripple and better transient response than power-save mode operation, but lower efficiency at low output current.

Note that the device inhibits Forced-PWM operation during start-up (that is, until the converter output has reached power-good for the first time.

Device Enable (EN)

The EN pin enables and disables the device.When the EN pin is high, the device is enabled. When the EN pin is low, the device is disabled.

Under-voltage Lockout (UVLO)

The device has an under-voltage lockout function that disables the device when the supply voltage is too low for correct operation.

Soft Start

To minimize inrush current and output voltage overshoot during start-up, the device has a soft-start function.

At turn on, the switch current limit ramps gradually to its maximum value and the device starts up in a controlled way. The gradual increase of the current limit generates the smallest inrush current for no-load conditions. It is also possible to start into a high load as long as the load does not exceed device current limit.

The rise time of the output voltage changes with the application circuit and the operating conditions. The output voltage rise time increases if the following occurs:the output capacitance is large,the load current is large,the device operates in boost mode.

See the Application and Implementation section for output voltage rise times in a typical application.

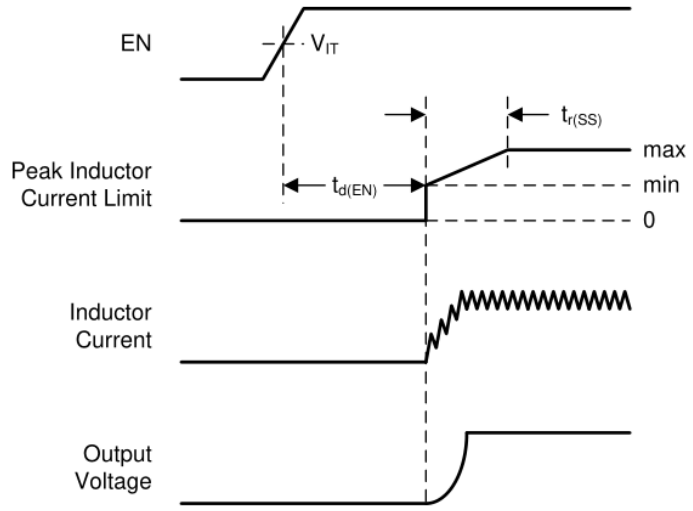


Figure 5. Device Start-Up

Output Voltage Control

The default output voltage is controlled by the VSEL pin. The output voltage default to 3.5V when VSEL pin is logic high, and it default to 3.3V when VSEL pin is logic low. When the EN=H and Reg_ENABLE=1, the device can programmer output voltages from 2.025V to 5.2V by I²C interface. From 2.025V to 5.2V, the output voltage step is 25mV. The following is an example of programmer output voltages by I²C interface.

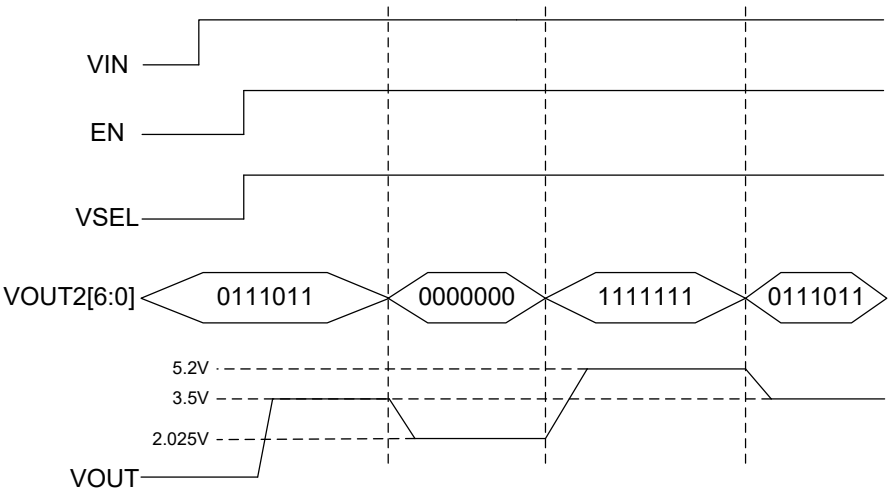


Figure 6. V_{OUT} Voltage programmed by I²C

Thermal Shutdown

The device has a thermal shutdown function which turns off the converter if the junction temperature is greater than 150°C. The device automatically turns on the converter again when the junction temperature is less than 120°C. You can still use the I^2C interface to read and write to the registers when the device is in an over-temperature condition.

When the device detects an over-temperature condition, it sets the TSD_STATUS bit in the Status register to 1. The device clears the TSD_STATUS bit to 0 when the junction temperature of the device is less than 120°C.

Load Disconnect

During device shutdown, the input is disconnected from the output. This prevents any current flow from the output to the input or from the input to the output.

Device Functional Modes

The device has two functional modes: off and on. The device enters the on mode when the voltage on the VIN pin is higher than the UVLO threshold and a high logic level is applied to the EN pin. The device enters the off mode when the voltage on the VIN pin is lower than the UVLO threshold or a low logic level is applied to the

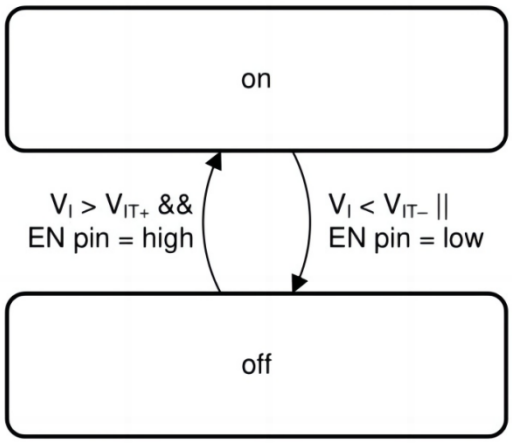


Figure 7. Device Functional Modes

EN pin

Programming

Serial Interface Description

Bus Interface

Base band Processor can transmit data with ET80101 each other through SDA and SCL port. SDA and SCL composite bus interface, and a pull-up resistor to the power supply should be connected.

Data Validity

When the SCL signal is high, the data of SDA port is valid and stable. Only when the SCL signal is low, the level on the SDA port can be changed.

Start (Re-start) and Stop Working Conditions

When the SCL signal is high, SDA signal from high to low represents start or re-start working conditions, while the SCL signal is high, SDA signal from low to high represents stop working conditions.

Byte format

Each byte of data line contains 8 bits, which contains an acknowledge bit. The first data is transmitted MSB.

Acknowledge

During the writing mode, ET80101 will send a low level response signal with one period width to the SDA port. During the reading mode, ET80101 will not send response signal and the host will send a high response signal one period width to the SDA.

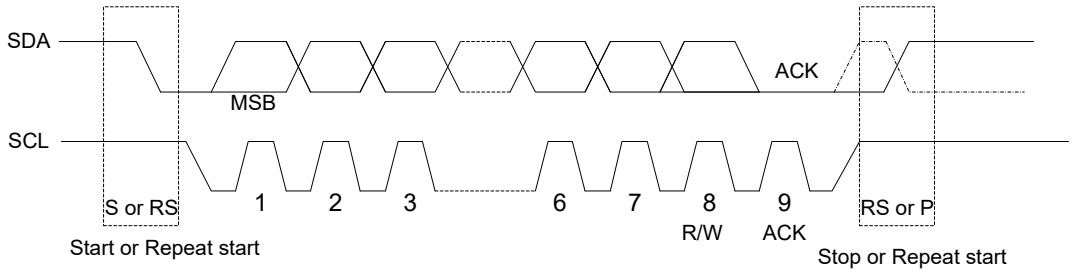


Figure 8. I²C write mode

- ACK=Acknowledge
- MSB=Most Significant Bit
- S=Start Conditions
- RS=Restart Conditions
- P=Stop Conditions
- Fastest Transmission Speed =1MHz
- Restart: SDA-level turnover as expressed by the dashed line waveform

Chip Address:

- 7bit address=1110101,VSEL=H
- 7bit address=1110110,VSEL=L

I²C Writing Command Register Interface Protocol (single):

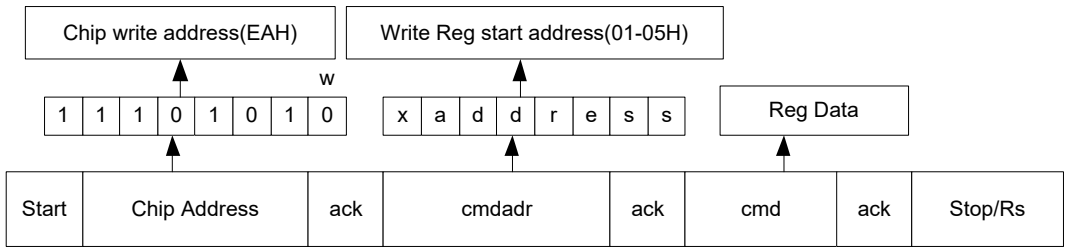


Figure 9. I²C Writing Command Register (single)

- Start=Start Conditions
- Chip address=Write register address =1110101+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr(0+REG's 7bit address)
- ack=Acknowledge
- Reg data = cmd(Command data)
- ack=Acknowledge
- Stop/Rs=Stop Condition/Restart Condition

I²C Writing Command Register Interface Protocol (continuous):

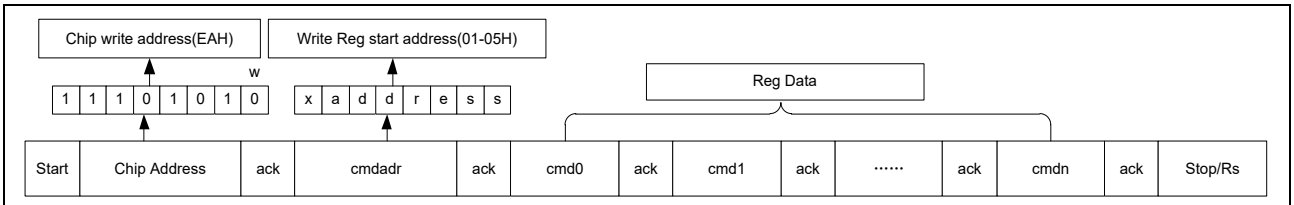


Figure 10. I²C Writing Command Register (continuous)

- Start=Start Conditions
- Chip address=Write register address =1110101+0(w)b
- ack=Acknowledge
- Write Reg start address byte = cmdadr(0+REG's 7bit address)
- ack=Acknowledge
- Reg data 0 = cmd0(Command data0)
- ack=Acknowledge
- ·····
- Reg data n =cmdn(Command datan)
- ack=Acknowledge
- Stop/Rs=Stop Condition/Restart Condition

I²C Reading Command Register Interface Protocol (single):

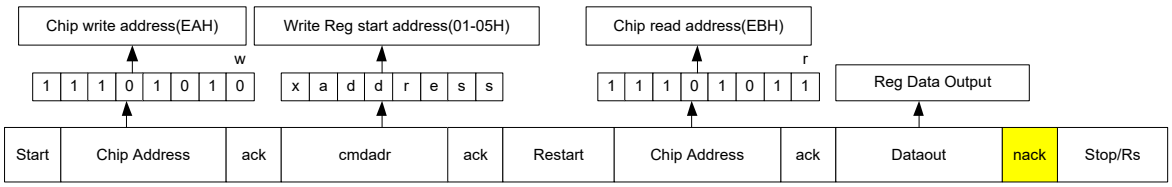


Figure 11. I²C Reading Command Register (single)

- Start=Start Conditions
- Chip address =Write register address=1110101+0(w)b
- ack=Acknowledge from ET80101
- Write Reg start address byte = cmdadr(0 + REG's 7bit address)
- ack=Acknowledge from ET80101
- Restart=Restart condition
- Chip address Read register address=1110101+1(r)b
- ack=Acknowledge from ET80101
- Dataout=Register data output
- nack=No Acknowledge from Host
- Stop/Rs=Stop Condition/Restart Condition

I²C Reading Command Register Interface Protocol (continuous):

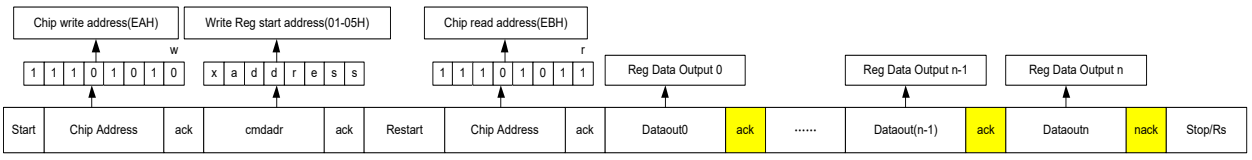


Figure 12. I²C Reading Command Register (continuous)

- Start=Start Conditions
- Chip address =Write register address=1110101+0(w)b
- ack=Acknowledge from ET80101
- Write Reg start address byte = cmdadr(0 + REG's 7bit address)
- ack=Acknowledge from ET80101
- Restart=Restart condition
- Chip address Read register address=1110101+1(r)b
- ack=Acknowledge from ET80101
- Dataout0=Register data output 0
- ack=Acknowledge from Host
- ……
- Dataoutn=Register data output n
- nack=No Acknowledge from Host
- Stop/Rs=Stop Condition/Restart Condition

Register Description

CONTROL_REGISTER Address:0x01 (Default:0010 0000b)

Bit	Symbol	Description	Read/Wirte	Default
Bit 7	RESERVED	Reserved.	R/W	0
Bit 6	RESERVED	Reserved.	R/W	0
Bit 5	ENABLE	Control Operation of the Converter. 0: Converter operation disabled. 1: Converter operation enabled.	R/W	1
Bit 4	RESERVED	Reserved.	R/W	0
Bit 3	FPWM	Set Forced PWM Operation. 0: Disable. 1: Enable.	R/W	0
Bit 2	RPWM	Set Ramp PWM Operation. 0: Disable. 1: Enable.	R/W	0
Bit 1	SLEW[1:0]	Set the Slew Rate. Set the slew rate of the output voltage change to a new value. 00: 1V/ms. 01: 2.5V/ms. 10: 5V/ms. 11: 10V/ms.	R/W	00
Bit 0				

STATUS_REGISTER Address: 0x02 (Default: 0000 0001b)

Bit	Symbol	Description	Read/Wirte	Default
Bit 7	RESERVED	Reserved.	R	0
Bit 6	SCP_STATUS	The status of the short circurt Function. 0: Normal operation. 1: An short circurt event is occurring.	R	0
Bit 5	OCP_STATUS	The status of the Over-Current Function. 0: Normal operation. 1: An over-current event is occurring.	R	0
Bit 4	TSD_STATUS	The status of the over-temperature Function. 0: Normal operation. 1: An over-temperature event is occurring.	R	0
Bit 3	SCP_FLAG	The status of the short circurt Function. It is cleared only if this register is read. 0: Normal operation. 1: An short circurt event was detected.	R	0
Bit 2	OCP_FLAG	The flag of the Over-Current Function. It is cleared only if this register is read. 0: Normal operation (default). 1: An over-current event was detected.	R	0
Bit 1	TSD_FLAG	The flag of the over-temperature Function. It is cleared only if this register is read. 0: Normal operation. 1: An over-temperature event was detected.	R	0
Bit 0	PG	Output Power-Good. if the power-not-good condition no longer exists. 0: A power-not-good event was detected. 1: Power-good.	R	1

DEVICE_IDENTITY_REGISTER Address: 0x03 (Default: 0101 0000b)

Bit	Symbol	Description	Read/Wirte	Default
Bit 7	DEVICE[3:0]	Device ID.	R	0
Bit 6			R	1
Bit 5			R	0
Bit 4			R	1
Bit 3	Manufacture ID	Device VERSION.	R	0
Bit 2			R	0
Bit 1			R	0
Bit 0			R	0

VOUT1_REGISTER Address: 0x04 (Default: 0011 0011b)

Bit	Symbol	Description	Read/Wirte	Default
Bit 7	RESERVED	Reserved.	R/W	0
Bit 6	VOUT1[6:0]	VOUT1 register determines the device output voltage if the VSEL pin is logic low. VOUT = 2.025 + (VOUT1[6:0] × 0.025)V (default 3.3V)	R/W	0
Bit 5			R/W	1
Bit 4			R/W	1
Bit 3			R/W	0
Bit 2			R/W	0
Bit 1			R/W	1
Bit 0			R/W	1

VOUT2_REGISTER Address: 0x05 (Default: 0011 1011b)

Bit	Symbol	Description	Read/Wirte	Default
Bit 7	RESERVED	Reserved.	R/W	0
Bit 6	VOUT2[6:0]	VOUT2 register determines the device output voltage if the VSEL pin is logic high. VOUT = 2.025 + (VOUT2[6:0] × 0.025)V (default 3.5V)	R/W	0
Bit 5			R/W	1
Bit 4			R/W	1
Bit 3			R/W	1
Bit 2			R/W	0
Bit 1			R/W	1
Bit 0			R/W	1

Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted)(1)

Parameters		Min	Max	Unit
V_{IO}	VIN, VOUT to AGND	-0.3	6	V
	EN, SDA, SCL to AGND	-0.2	6	V
	SW1,SW2 to PGND	-0.3	6.5	V
V_{ESD}	Human Body Model (JEDEC JS-001)	-2000	+2000	V
	Charged Device Model (JESD22-C101)	-500	+500	V
T_J	Junction Temperature	-40	+150	°C
T_{STG}	Storage Temperature	-65	+150	°C

Notes:

(1) tresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal, unless otherwise noted.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(3)

Symbol	Parameters		Min		Max	Unit
V_{IN}	Supply voltage		2.2		5.0	V
V_O	VSEL=H, Default Output voltage			3.5		V
	VSEL=L, Default Output voltage			3.3		V
	Programmed Output voltage by I^2C		2.025		5.2	V
V_{IH}	High-level input voltage	SCL, SDA, VSEL	0.9		V_{IN}	V
V_{IL}	Low-level input voltage	SCL, SDA, VSEL	0		0.4	V
V_{EN}	EN input voltage		0		V_{IN}	V
C_{IN}	Input capacitance(4)			10		μF
C_O	Output capacitance (4)			22		μF
L	Inductance			0.47		μH
T_A	Operating free-air temperature range		-40		85	°C
T_J	Operating junction temperature range		-40		125	°C

Notes:

(3) The device can sustain the maximum recommended output current only for short durations before its junction temperature gets too hot. Users must verify that the thermal performance of the end application can support the maximum output current.

(4) Effective capacitance after DC bias effects have been considered.

Electrical Characteristics

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted). Typical values are at V_I = 3.8V, V_O = 3.5V and T_J = 25°C (unless otherwise noted).

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN_RANGE}	Input voltage range		2.2		5.0	V
I_{Q_VIN}	Supply current into VIN	V_I = 3.8V, V_O = 3.5V, $V_{(EN)}$ = 3.8V, switching, T_J = 25°C		2	5	μA
I_{SD}	Shutdown current into VIN	V_I = 3.8V, $V_{(EN)}$ = 0V or ENABLE=0, T_J = 25°C		0.35	1	μA
$V_{I_UVLO_H}$	UVLO threshold voltage	Rising,T_J = 25°C	1.95	2.05	2.15	V
$V_{I_UVLO_L}$	UVLO threshold voltage	Falling,T_J = 25°C	1.75	1.85	1.95	V
V_{OUT_RANGE}	Output voltage range	VSEL=L	2.025	3.3	5.2	V
		VSEL=H	2.025	3.5	5.2	
V_{STEP}	Step of output voltage			25		mV
V_{O_ACC}	Output voltage accuracy	PWM operation	-1		1	%
		PSM operation	-1		3	%
V_{O_RIPPLE}	Output voltage Ripple	V_I=3.5V, V_O=3.5V, PWM Mode		35	50	mV
		V_I=4V, V_O=3.5V, PWM Mode		10	20	mV
		V_I=4V, V_O=3.5V, PFM Mode		50	100	mV
V_{O_Tran}	Output voltage transient Ripple	V_I=3.8V, V_O=3.5V, Buck Mode, I_O=0~0.3A, 1us edge		80	100	mV
I_{OUT_Max}	Output max current	V_I=2.2V, V_O=3.5V	0.7	0.9		A
		V_I=2.2V~2.5V, V_O=3.5V	0.8	1		A
		V_I > 2.5V, V_O=3.5V	1	1.2		A
Efficiency	V_I=3.8V, V_O=3.5V, Buck Mode	I_O = 100uA	85	95		%
		I_O = 5mA	90	95		%
		I_O = 100mA	93	95		%
	V_I=3.0V, V_O=3.5V, Boost Mode	I_O = 100uA	84	90		%
		I_O = 5mA	88	92		%
		I_O = 100mA	90	93		%

Electrical Characteristics(Continued)

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted). Typical values are at V_I = 3.8V, V_O = 3.5V and T_J = 25°C (unless otherwise noted).

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{DS_ON(SW1_HS)}$[(1)]			V_I=3.8V, T_J = 25°C		48		mΩ
$R_{DS_ON(SW1_LS)}$[(1)]			V_I=3.8V, T_J = 25°C		40		mΩ
$R_{DS_ON(SW2_HS)}$[(1)]			V_I=3.8V, T_J = 25°C		53		mΩ
$R_{DS_ON(SW2_LS)}$[(1)]			V_I=3.8V, T_J = 25°C		45		mΩ
F_{SW}	Operation frequency in current continuous mode		V_I = 3.8V, V_O = 5V, T_J = 25°C,Boost Mode	1.4	1.8	2.2	MHz
			V_I = 3.5V, V_O = 3.5V, T_J = 25°C, Buck-Boost Mode	1.1	1.4	1.7	MHz
			V_I = 5V, V_O = 3.5V, T_J = 25°C,Buck Mode	1.65	2.1	2.55	MHz
I_{LIM}	Valley current Limit of inductor		V_I = 3.8V, V_O = 5V, T_J = 25°C,Boost Mode	1.6	2.0		A
			V_I = 3.5V, V_O = 3.5V, T_J = 25°C, Buck-Boost Mode	0.8	1.0		A
			V_I = 5V, V_O = 3.5V, T_J = 25°C,Buck Mode	0.95	1.20		A
t_{SS}[(1)]	Soft Start Time		Internal soft-start time		0.5	1	ms
V_{PG_H}	Output power good rising threshold		VOUT rising,T_J = 25°C	92	95	98	%V_{OUT}
V_{PG_L}	Output power good falling threshold		VOUT falling,T_J = 25°C	81	84	87	%V_{OUT}
V_{IT+}	Positive-going input threshold voltage	SCL SDA		0.9			V
		VSEL EN		0.9			
V_{IT-}	Negative-going input threshold voltage	SCL SDA				0.4	V
		VSEL EN				0.4	

Notes:

(1) Not production tested, design assurance

Electrical Characteristics(Continued)

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted). Typical values are at V_I = 3.8V, V_O = 3.5V and T_J = 25°C (unless otherwise noted).

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
I_{IH}	High-level input current	SCL, SDA, VSEL	$V_{(SCL)}$ = $V_{(SDA)}$ = $V_{(VSEL)}$ = 3.3V, no pull-up resistor		±0.01	±0.1	μA
I_{IL}	Low-level input current	SCL, SDA, VSEL	$V_{(SCL)}$ = $V_{(SDA)}$ = $V_{(VSEL)}$ = 0V,no pull-up resistor		±0.01	±0.1	μA
V_{OL}	Low-level output current	SCL, SDA	I_{OL} = 10mA			0.4	V
I_{IB}	Input bias current	EN	$V_{(EN)}$ = 0V to 5.0V		0.01	0.1	μA
T_{SD}	Thermal shutdown threshold temperature		T_J rising		150		°C
T_{HSY}	Thermal shutdown hysteresis				30		°C

Timing Requirements

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

I^2C Timing

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCL}	SCL Clock Frequency	0	-	1000	KHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	1.3	-	-	μs
$t_{HD:STA}$	Hold Time(Repeated) START Condition	0.6	-	-	μs
t_{LOW}	Low Period of SCL Clock	1.3	-	-	μs
t_{HIGH}	HIGH Period of SCL Clock	0.6	-	-	μs
$t_{SU:STA}$	Setup Time for a Repeated START Condition	0.6	-	-	μs
$t_{HD:DAT}$	Data Hold Time	-	-	0.9	μs
$t_{SU:DAT}$	Data Setup Time	100	-	-	ns
t_R	Data Hold Time2	-	$20+0.1C_b$ (6)	300	ns
t_F	Data Hold Time2	-	$20+0.1C_b$ (6)	300	ns
$t_{SU:STO}$	Setup Time for STOP Condition	0.6	-	-	μs

Note6: C_b=total capacitance of one bus line in PF.

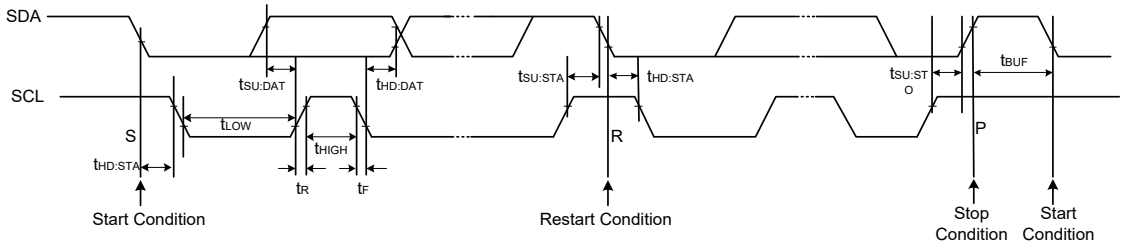
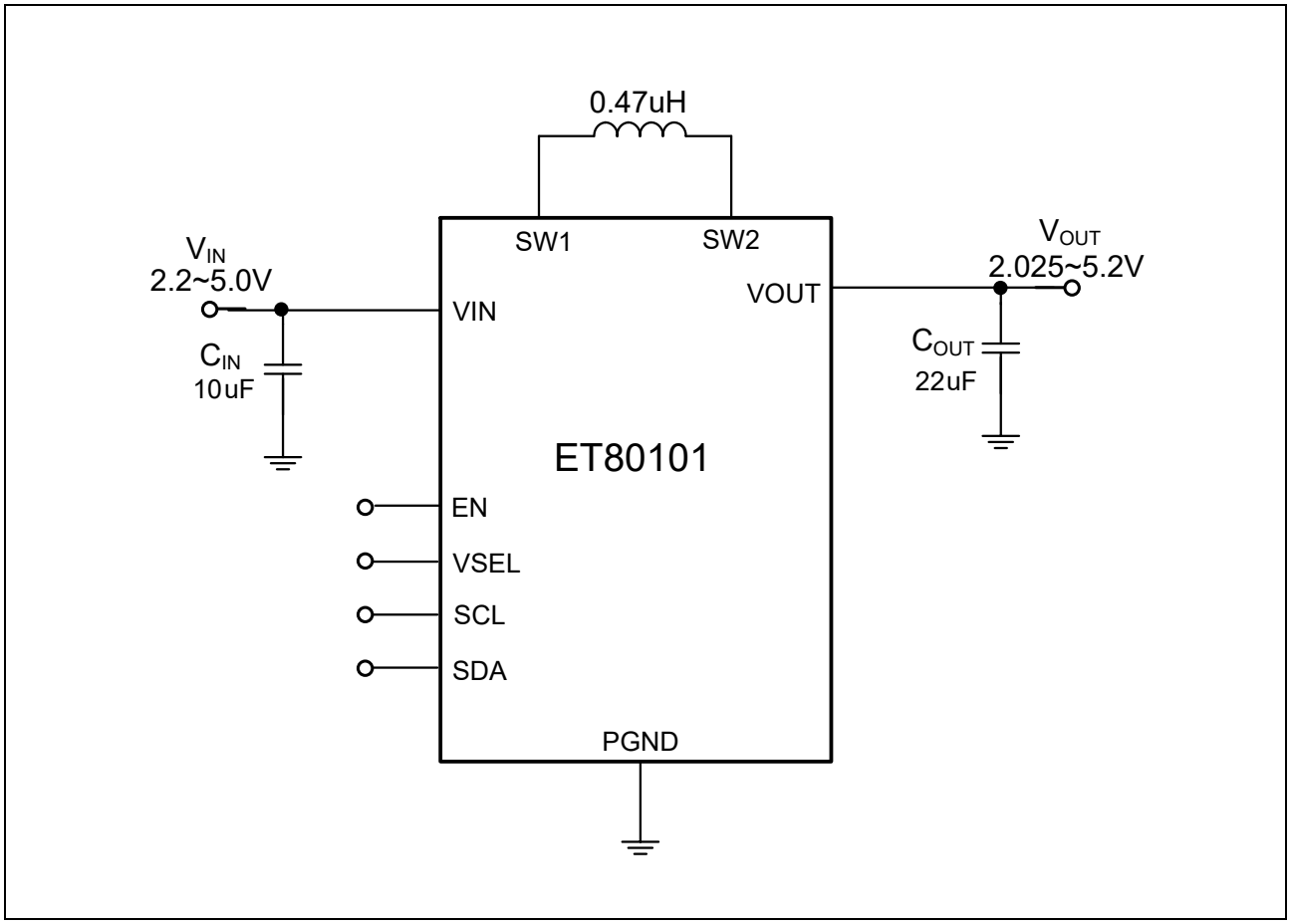


Figure 13. I^2C Timing Waveform

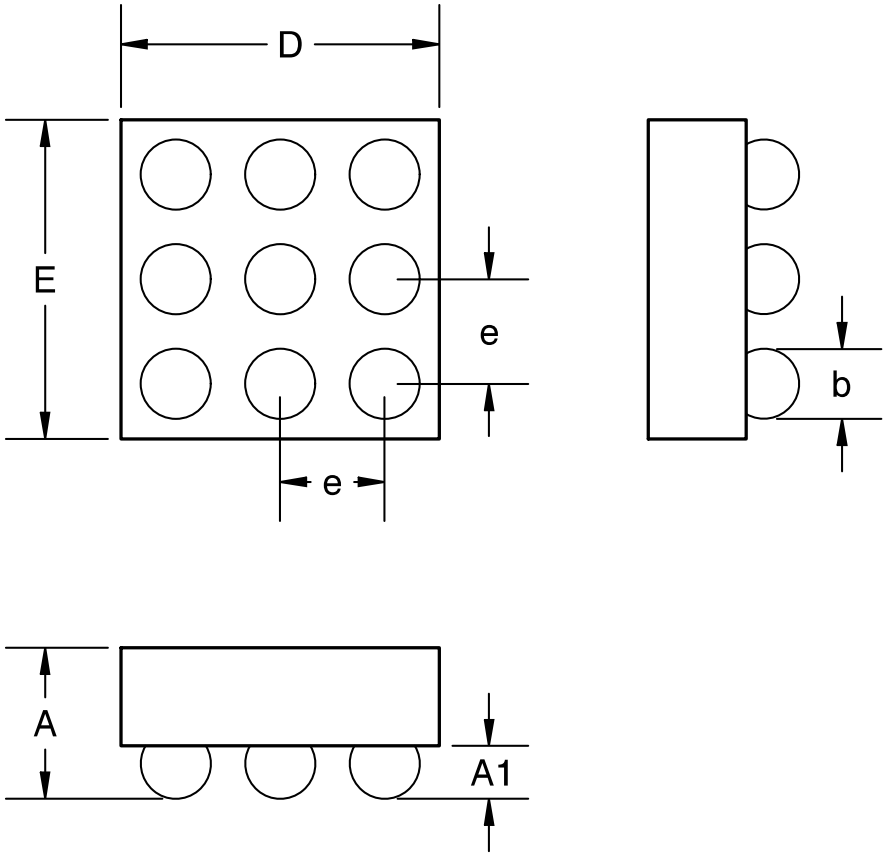
Typical Application Circuits



Note*: The circuit diagram is for reference only.

Package Dimension

WLCSP9



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.487	0.540	0.593
A1	0.170	0.195	0.220
b	0.245	0.270	0.295
D	1.250	1.280	1.310
E	1.250	1.280	1.310
e	0.400 BSC		

Revision History and Checking Table

Version	Date	RevisionItem	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2024-07-19	Preliminary Version	Liuc	Xielh	Liujy
0.1	2025-11-26	Update Electrical Characteristics and Package Dimension	Liuc	Xielh	Liujy
0.2	2026-3-17	Update Electrical Characteristics &Functional Description	Liuc	Xielh	Liujy
0.3	2026-5-13	Update Electrical Characteristics	Liuc	Xielh	Liujy
0.4	2026-5-29	Update Voltage Control	Liuc	Xielh	Liujy
0.5	2026-6-15	Update Electrical Characteristics	Liuc	Xielh	Liujy
1.0	2026-7-8	Official Version	Liuc	Xielh	Liujy